Impact of Transistor Aging on RF Low Noise Amplifier Performance of 28nm Technology : Reliability Assessment

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***Abstract*— Transistor reliability has become one of the major concerns in reliable circuit design in advanced CMOS nanometer technology. Transistor aging can have a significant impact on the performance of the RF frontend circuits. In this paper, the impacts of transistor aging on a RF low noise amplifier (LNA) are studied. In this work, single-ended cascode LNA with source inductive degeneration and LC folded-cascode LNA test circuits are used to study the transistor aging effect. The noise figure (NF) and the gain, critical performance parameters of a LNA are shown to be degradation-sensitive. It is shown that the noise figure of the LNA is significantly increased and the gain of the LNA is decreased by the aging effect using a 28nm technology. The optimum gate bias point and the cascode structure have been shown as design guidelines to make the LNA more reliable.**

I. INTRODUCTION

Technology scaling toward nanometer CMOS technologies accelerates transistor degradation. It is becoming hard to solve the degradation effects at the technology level. Hence, circuit designer needs to take this as a serious issue to be solved at design level [1]. In recent years, circuit-level aging resilience has become one of the main focuses of research in reliability domain. At circuit level, the emphasis has mainly been on the monitoring digital circuits and digital building blocks, which have been shown to be very susceptible to BTI degradation [2-4]. However, some significant work also addresses analog circuit performance degradation. A very little attention, however, has been paid to radio-frequency circuits [5-8]. However, no dedicated study has been done on the performance degradation of a LNA in an advanced technology node such as 28nm. In communications, noise is a very important parameter, which is an important specification for the circuit designer. For noise, the low noise amplifier (LNA) is the heart of the receiver section. The lifetime of good noise performance of the LNA will decide whether the whole receiver can work normally for a long period or not. This paper aims to provide RF circuit designers a detail analytical analysis of performance degradation of a LNA under the device aging effect. The focus is on discussing the performance degradation of different LNA topologies to identify if any topology dependency exists. The analysis shows the optimum gate bias point and the cascode structure can be used as design guidelines to make LNA more reliable.

In this paper, section II briefly reviews the transistor aging. In section III, the investigated LNA topology and the analysis of the degradation effects are described. Next, section IV discusses the background of the reliability simulation framework. The simulation results are presented in Section V. Section VI discusses the results. Finally, conclusions are drawn in Section VII.

II. TRANSISTOR AGING

Transistor aging phenomena were first observed during the early eighties. Regarding aging mechanisms of a transistor, we account for the Bias Temperature Instability (BTI) effect, Hot Carrier Insertion (HCI) and Time-Dependent Dielectric Breakdown (TDDB) induced degradation. This section reviews these important transistor aging phenomena.

A. Bias Temperature Instability

When subject to operating bias voltage and temperature, a transistor exhibits changes in its characteristics over time; this effect is termed as bias temperature instability (BTI). BTI is typically observed as a threshold voltage shift. Extensive efforts have been placed to understand and model the BTI. It has been found that during AC stress the BTI damage has a permanent (P) as well as a recovery component (R) [9] [10]:

$$\Delta V_{TH} \sim \underbrace{\exp(\alpha_1 V_{GS}) t^{n_p}}_{\text{P}} + \underbrace{V_{GS}^{\alpha_1}(C_R + n_R \log_{10}(t))}_{\text{R}} \quad (1)$$

Here, α_1 and α_2 are voltage scaling factors. n_p and n_R are time exponents. All these coefficients along with C_R are process dependent. The recovery component (R) characterizes the so called relaxation or recovery of the BTI degradation immediately after the stress voltage has been removed.

B. Hot Carrier Injection

Hot Carrier (HC) stress consists of a large lateral electric field near the drain end of a transistor in saturation and results in a change of the transistor characteristics such as the threshold voltage V_{TH}, the carrier mobility β and the output conductance g_o [11]. Here in this work we used the HCI degradation model described in [11]:

$$\Delta V_{TH} \sim \frac{1}{\sqrt{L}} \exp(\alpha_3 V_{GS}) \exp(\alpha_4 V_{DS}) t^{n_{HC}} \quad (2)$$

where $n_{HC} \approx 0.5$ represents the time exponent. α_3 and α_4 are technology-dependent voltage scaling parameters.

C. Time-Dependent Dielectric Breakdown

The strong electric fields across the gate-oxide can cause oxide damage, subsequent to Time-Dependent Dielectric Breakdown (TDDB) in nanometer CMOS devices. Soft breakdown (SBD)

is more prominent than hard breakdown (HBD) for sub-180nm CMOS devices, which is observed as a partial loss of the dielectric properties and results in an increase of the magnitude and the noise of the gate current [1]. The voltage at which TDDB happens are typically not used for analog circuits in 28 nm technology so TDDB may not have significant impact on RF circuit in nominal operating conditions.

III. RF LOW NOISE AMPLIFIER

A. Circuit Topologies

A cascode LNA with inductive source degeneration structure is widely used in RF receiver design. A single-ended cascode LNA with source inductive degeneration is depicted in Fig.1. MN1 and MN2 are same-size transistors, giving a better noise isolation.

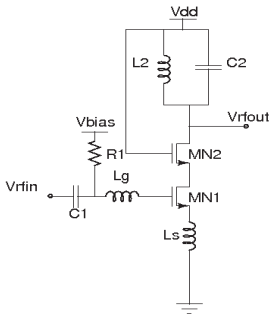

Fig. 1: Cascode LNA with inductive source degeneration

Fig.2 sketches the folded-cascode LNA topology. The common-gate transistor MP2 of the cascode LNA is folded to another biasing path. This topology provides the possibility to increase the bias voltage which will increase the g_m of MN1. An increase in g_m will consequently increase the cutoff frequency $\omega_T \simeq g_m/C_{gs}$. This will result in an overall noise figure (NF) reduction.

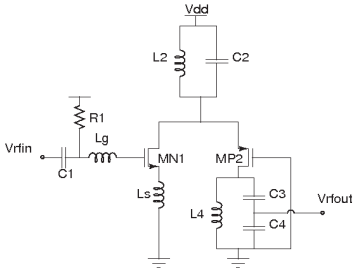

Fig. 2: Folded-cascode LNA topology

This topology has been chosen because it contains NMOS and PMOS transistors in the same structure. Especially MP2 (PMOS) transistor is placed between the supply and ground rails. So, it can have the full supply voltage to accelerate the degradation and therefore, more likely to suffer from NBTI and HCI degradations. These LNAs have been designed in a 28nm CMOS technology with the targeted NF of <2dB and the gain of >10dB at 20GHz operating frequency.

B. LNA Noise Figure and Gain Aging

In principle, all MOSFETs in the LNA are affected by described degradation mechanisms. The folded-cascode LNA has common-source (CS) stage with inductive source degeneration and it works like a traditional cascode LNA

The noise figure of the LNA with inductive source degeneration can be estimated as [12]:

$$NF_{LNA} = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha}\frac{\chi}{Q_L}\left(\frac{\omega_0}{\omega_T}\right) \quad (3)$$

$$NF_{LNA} = A + K\left(\frac{\omega_0}{\omega_T}\right) \quad (4)$$

where, $A = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s}$ and $K = \frac{\gamma}{\alpha}\frac{\chi}{Q_{L\,s}}$

R_l is the parasitic resistance of the inductor (L_g) at the input, R_s is the internal resistance of the signal source, R_g is the gate resistance of the input MOSFET (MN1), γ, α and χ are technology dependent constants, Q_L is the quality factor which is constant for fixed ω_0, ω_0 is the operating frequency of the LNA, ω_T is the cut-off frequency of the input MOSFET (MN1):

$$\omega_T \approx \frac{g_m}{C_{gs}} \quad (5)$$

From (4), $NF_{LNA} = A + K\omega_0\left(\frac{C_{gs}}{g_m}\right)$ (6)

Then, $\Delta NF_{LNA}\big|_{aging} \approx \frac{\partial NF_{LNA}}{\partial C_{gs}}\Delta C_{gs} + \frac{\partial NF_{LNA}}{\partial g_m}\Delta g_m$ (7)

$$\Delta NF_{LNA}\big|_{aging} \approx \frac{\Delta C_{gs}}{C_{gs}}.K\omega_0\left(\frac{C_{gs}}{g_m}\right) - \frac{\Delta g_m}{g_m}.K\omega_0\left(\frac{C_{gs}}{g_m}\right) \quad (8)$$

From (6) & (8), we get, $\frac{\Delta NF_{LNA}\big|_{aging}}{NF_{LNA} - A} \approx -\frac{\Delta g_m}{g_m} + \frac{\Delta C_{gs}}{C_{gs}}$ (9)

Similarly from (5), $\frac{\Delta\omega_T}{\omega_T} = \frac{\Delta g_m}{g_m} - \frac{\Delta C_{gs}}{C_{gs}}$ (10)

where g_m is the transconductance of the input MOSFET MN1, C_{gs} is the gate capacitance of MN1.

BTI and HCI both decrease the g_m of the MOSFET. From the above equations (9) and (10), we find that the decrease in g_m will increase the NF of the LNA and decrease the cut off frequency (ω_T) of the input transistor.

The gain of the cascode LNA is given by [12]:

$$G = \left(\frac{\omega_T}{\omega_0}\right)\frac{R_L}{2R_S} \quad (11)$$

Then, $\left.\frac{\Delta G}{G}\right|_{aging} = \frac{\Delta\omega_T}{\omega_T}$ (12)

From (10), we get,

$$\left.\frac{\Delta G}{G}\right|_{aging} = \frac{\Delta g_m}{g_m} - \frac{\Delta C_{gs}}{C_{gs}} \quad (13)$$

where, R_L is the load resistance of the LNA. From the above equations (13), we find that the decrease in g_m will decrease the gain of the LNA.

Numerical Calculation (folded-cascode LNA):

When the supply voltage is 1.25V and the gate bias voltage of the input transistor MN1 is 0.5V, we get the total Vth-shift after the 5year lifetime is ~20% from the models, described in the section II. From the first order transistor equation, the transconductance of the input MOSFET MN1is defined as:

$$g_m = \beta(V_{gs} - V_{th}), \text{ then, } \frac{\Delta g_m}{g_m} = \frac{\Delta\beta}{\beta} - \frac{\Delta V_{th}}{(V_{gs} - V_{th})} \quad (14)$$

Where, β presents a term which includes the transistor size (W/L), the oxide capacitance (C_{ox}) and the carrier mobility (μ).

From (14), $\frac{\Delta g_m}{g_m} \simeq -0.28$, when Vth-shift is ~ 20%. We get $\frac{\Delta C_{gs}}{C_{gs}} \simeq -0.11$ by extracting the value of C_{gs} of the input transistor MN1 once for the fresh LNA (without any degradation effect) and again with ~20% Vth-shift. Now, from (9) we get the predicted normalized noise figure shift as:

$$\frac{\Delta NF_{LNA}\big|_{aging}}{NF_{LNA} - A} \approx 18\%$$

Similarly from (13) we get gain-shift, $\frac{\Delta G}{G}\Big|_{aging} \approx -18\%$

From the above calculations, we can observe that the gain of the LNA will decrease and the noise figure will increase when g_m decreases by transistor aging. Since the noise figure as well as the gain of the LNA plays a decisive role in the noise performance of the entire receiver system, the aging of the LNA will have a significant impact on the receiver performance.

IV. RELIABILY SIMULATION FRAMEWORK

To perform circuit level degradation analysis, an extended SPICE simulator can be used as is described in [14]. In our MICAS laboratory, a custom reliability simulator has been developed [14], which incorporates aging models to the SPICE models. For advanced sub-45nm CMOS technology node aging effects, especially BTI, become stochastic in nature [13]. Our simulation tool is capable to perform both deterministic and stochastic simulation of the aging effects in circuits.

In this work, the LNA circuit has been simulated with this custom reliability simulator. Simulation results are presented in the next section.

V. LNA RELIABILITY SIMULATION RESULTS

The two LNAs are designed in a 28nm CMOS technology and simulated with the custom reliability simulator mentioned in the previous section. This simulator uses ELDO as the underlying circuit solver. The circuits are evaluated, over a lifetime of 5 years[1]. Table I shows the experimental results. Both the average performance shift Δμ(P) and the shift of standard deviation Δσ(P) were recorded over time.

Cascode LNA:

For the cascaded LNA topology (Fig.1), it is observed from the simulation results in the Table I that after 5years the NF is increased by ~0.6% and the gain of the LNA has decreased by ~1% due to stress, which are not very significant.

TABLE I

RELIABILITY ANALYSIS OF LNA FOR 28nm CMOS TECHNOLOGY

LNA Topology	Performance Spec (P)	Nominal Value	Avg. Shift (%) Δμ(P)	SD Shift (%) Δσ(P)
Cascode LNA	NF (dB)	1.1925	+0.6	+2.3
	NF_{MIN} (dB)	1.0190	+0.7	+5.7
	Gain (dB)	11.905	-1	+5.3
Folded LNA	NF (dB)	1.6198	+13	+64.5
	NF_{MIN} (dB)	1.0424	+13.7	+84
	Gain (dB)	12.453	-8.6	-30

Folded-cascode LNA:

The NF and the gain of the folded-cascode LNA over a 5year lifetime are depicted in Fig.5. This result is the combined effect of NBTI and PBTI along with HCI and SBD on the performance of the folded-cascode LNA (Fig. 2).

If we see the Noise figure and the gain degradation curves in Fig.3, the noise figure (in dB) is increased significantly with ~13% and the gain (in dB) is decreased by ~8.6%, which is also a significant deviation due to transistor aging. If we convert the simulated value of the noise figure and the gain from dB to magnitude then we get,

$$\frac{\Delta NF_{LNA}\big|_{aging}}{NF_{LNA} - A} \approx 16\% \text{ and } \frac{\Delta G}{G}\Big|_{aging} = -12\%$$

which are well fit with numerical prediction from analysis in section III. Both degradations are significantly worse than for the single-ended cascode LNA.

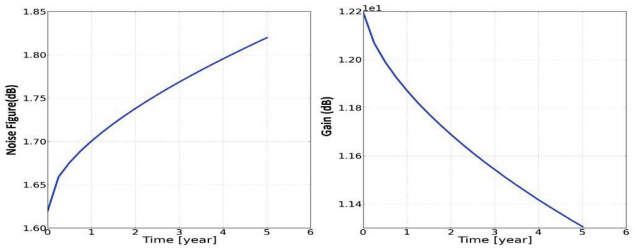

Fig. 3: Evolution of the NF and the gain of the folded LNA over a 5year lifetime

This result shows the expected degradation according to the analytical analysis from section III which concludes that the NF will increase and the gain of the LNA will decrease by the aging of the input device. In Fig. 4, the simulated noise figure (NF) of the folded-cascode LNA (Fig.2) is plotted as a function of the frequency.

[1]Due to the logarithmic lifetime dependence of both HCI and BTI effects (Section II), reliability simulations over the first 5 years of the product lifetime yield relevant conclusions for a complete lifetime (7–10 years or more) in commercial use. Therefore, a 5-year lifespan is used for LNA circuit evaluation.

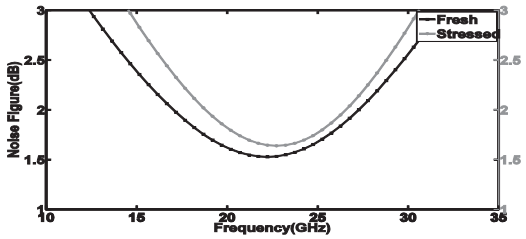

Fig. 4: NF of the folded LNA as a function of frequency before and after a 5year lifetime

The gain of the LNA as a function of the frequency before and after stress is shown in fig.5.

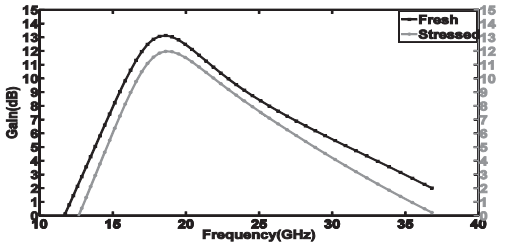

Fig. 5: Gain of the folded LNA as a function of frequency before and after a 5year lifetime

VI. DISCUSSION

From the above simulation results, it is observed that the NF and the gain of a cascode LNA are not very sensitive to the aging effects, whereas these two performance parameters are significantly degraded for the folded-cascode LNA. In the cascode LNA the supply voltage is shared by two transistors MN1 and MN2. So, the drain-to-source voltage stressing the input transistor MN1 is reduced. Therefore, aging effects are also lower because of the low voltage stress.

Whereas in case of folded-cascode LNA (Fig. 2), as both transistors are placed between the supply and the ground rail, they suffer more from the aging effects due to this higher voltage stress. So, it is concluded that the cascode LNA topology is more reliable than the folded-cascode LNA for the device aging effects in 28nm technology.

As can be seen in Fig. 5, the absolute value of gm-shift (after 5year lifetime) of the input transistor MN1 of the folded LNA due to device aging varies with the gate bias voltage.

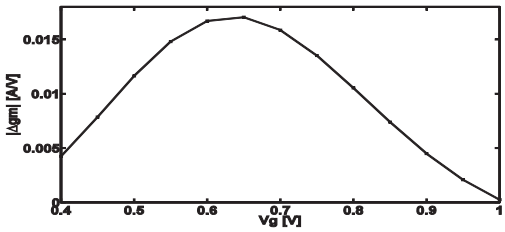

Fig. 5: Absolute value of gm-shift (after 5yera lifetime) of the input transistor MN1 of the folded LNA due to device aging varies with the gate bias voltage.

According to this plot, gm-shift due to aging will significantly decrease with high gate voltage when transistor MN1 is in saturation. When the folded LNA has been simulated with input dc bias voltage 0.8V, we found the noise figure (in dB) shift as well as the gain (in dB) degradation is <1%. This analysis shows that the optimum input gate bias voltage and the cascode structure can be used as design guidelines to make LNA more reliable.

VII. CONCLUSION

In this paper the aging-induced performance degradation of two different state-of-the-arts LNA topologies have been evaluated. The degradation of two critical parameters, the noise figure (NF) and the gain of the LNAs, have been demonstrated in 28nm technology. It is concluded that device-aging-induced degradation of the NF and the gain of the LNA is topology dependent and is higher for the folded-cascoded than the single-ended topology. It is also shown that the optimum input gate bias voltage reduces the NF and the gain degradation of the LNA. This work will help to find more aging-resilient topologies for RF circuits.

ACKNOWLEDGMENT

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