27.6 A 1.7mW 11b 1-1-1 MASH ΔΣ Time-to-Digital Converter

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Recently, high resolution TDCs have gained more and more interest due to their increasing implementation in digital PLLs, ADCs, jitter measurement and time-of-flight measurement units. Similar to ADCs, existing architectures of TDCs can be divided into several categories: flash TDCs [1,3], pipeline TDCs [2], and SAR TDCs [4]. The highest achievable time resolution of a TDC is mainly limited by the CMOS gate delay. In order to get sub-gate-delay resolution, the Vernier method is commonly used. However, the mismatch problem caused by process variation limits its effectiveness, and the same holds for the time amplification method. The gated-ring-oscillator (GRO) method [5] is introduced to achieve sub-ps time resolution, but it still requires an equivalent CMOS gate delay as low as 6ps. Upcoming applications in 4th generation nuclear reactors, space and high energy physics like the Large Hadron Collider (LHC), require the TDC to achieve a high time resolution in harsh environments with high temperature and radiation, where the threshold voltage, transconductance, and delay of a transistor undergo dramatic changes. In these cases, the high accuracy and robustness of the TDC need to be inherent to the design rather than by employing a fast CMOS technology.

The noise-shaping technique is widely used in design of ADCs, which can improve the effective resolution of a coarse quantizer, but requires no precisely matching analog components. The same concept can principally be ported to the design of TDCs. The commonly used ΔΣ structure which consists of integrators can not be directly adopted by a TDC, due to the difficulty of realizing a time integrator. In this work, however, the first MASH ΔΣ TDC is reported. A first-order noise-shaping TDC has been built in an error-feedback manner, as shown in Fig. 27.6.1. The error-feedback structure is impractical for a ΔΣ ADC since its performance is limited by the inaccuracy of the analog subtractors. However, time subtraction can be easily realized by nand/nor operation, and moreover, the error-feedback structure does not require an explicit integrator in the loop.

Directly preserving the quantization error in the time regime is still impossible with current technologies: the time information has to be converted into another intermediate physical quantity such as voltage or charge. A relaxation oscillator can generate a clock by alternatively charging and discharging two capacitors. The phase of the clock corresponds to the voltage on each capacitor. The time can be measured by enabling the oscillator during the measurement interval and counting the number of periods of the generated clock. When the oscillation stops, the phase of the clock, which refers to the quantization error, can be stored on the capacitor as a residue voltage. Principally, it is similar with the GRO [5], but the skew error caused by charge redistribution during the start and stop of the oscillator is negligible here due to the large capacitance. In a GRO based TDC it can significantly deteriorate the performance.

By cascading several error-feedback stages, a higher order noise-shaping can be obtained. A third-order MASH TDC is shown in Fig. 27.6.1. All stages have the same architecture and are followed by digital processing blocks. It is algebraically equivalent to a conventional 1-1-1 MASH ΔΣM. The MASH TDC works as follows: In each stage, the time signal *tin* controls a current to charge two capacitors. When it is active high, one of the two capacitors starts charging. For instance, *vinp1* starts rising when *vinn1* stays at *vlow*, as illustrated in Fig. 27.6.2. When *vinp1* reaches *vhigh*, the comparator output becomes '1'. This reverses the state of the SR-latch, and triggers the oscillation. After the stop signal arrives, the phase of the clock is preserved; the counter is first read out and then reset to 0. Due to the fact that the counter is only driven by the rising edge of the clock, a time which equals the quantization error *q[1]* will be subtracted from the next input. The overall quantization error can then be described as *q[2]-q[1]*. The time signal which feeds into the following stage is generated by taking the first rising edge of the counting clock as a start signal, and keeping the same falling edge as the TDC's input.

The frequency of the relaxation oscillator can be expressed as *IREF/(VREF·2C)*. By correlating *VREF* and *IREF* as *VREF* = *IREF·R*, its frequency becomes only depending on passive components, which is *1/(2·RC)*. Thus, it exhibits inherent PVT variation tolerance and the matching between stages is better than for its MASH ADC counterparts.

Fig. 27.6.3 shows the schematics in the 1-1-1 MASH TDC. The main origin of noise in the TDC is the comparator delay. When the oscillator is disabled, the comparator state may not be perfectly preserved due to the hysteresis. This will introduce extra noise into the preserved quantization error, and it can only be suppressed by oversampling. A four-stage threshold detection comparator is adopted in this design. Each of the first three stages has a gain of 10dB and consumes 40μA current. The last stage provides a higher gain of 20dB with a power consumption of 80μA. This comparator has a delay of 0.8ns. Two comparators in each stage are turned off alternately to save power, when its connected capacitor is not being charged. Charge injection when turning on/off input switches and kT/C noise also contribute to the overall noise level. In the conversion to time noise the local noise voltage is divided by the charging slope of the capacitor. Thus, a larger slope is mostly desirable. In this design, *IREF* = 50μA, *VREF* = 650mV, and *C* = 0.64pF, which gives a charging slope of 80μV/ps.

A PWM signal, modulated by a sine wave, is employed to evaluate the performance of the TDC, and the bandwidth is set to 100kHz. An 18kHz -3dBFS signal is used for large signal measurements. The full scale input range is 100ns, when the OSR is 25, and the carrier frequency is 5MHz. The output spectrum and waveform are shown in Fig. 27.6.4a. It shows an SNDR of 60.3dB. Fig. 27.6.4b shows the results of a small signal measurement, when the full scale input range is 10ns, and a 22kHz -40dBFS signal is applied. The carrier frequency is 50MHz and the OSR is 250. An SNDR of 28dB and a resolution of 5.6ps are achieved. The system is also compatible with other OSR values, such as 50 and 100. Fig. 27.6.5 shows the DR of the TDC, which is 68dB. Note that, there is no apparent drop on SNDR when the input level is close to full scale, since in a TDC system, the input dynamic range is only limited by the depth of the counter, which can be easily extended to avoid any overloading of the system.

A radiation assessment with a dose rate of 30kGy/h has been performed, as shown in Fig. 27.6.6, proving the TDC's robustness. The current consumption is almost not affected and even after an extremely high radiation dose of 3.4MGy, the ENOB drops only 1 bit and, for an OSR of 250, a 10.5ps time resolution is still achieved.

This first reported 1-1-1 MASH ΔΣ TDC is implemented in 0.13μm CMOS. It consumes only 1.7mW from a 1.2V supply and achieves an ENOB of 11b. The SNDR is mainly limited by the comparator delay. It can principally be reduced by adding more power to the comparator or applying calibration. The developed MASH TDC architecture gives full flexibility to design high resolution low power TDCs even for extreme environments.

References:

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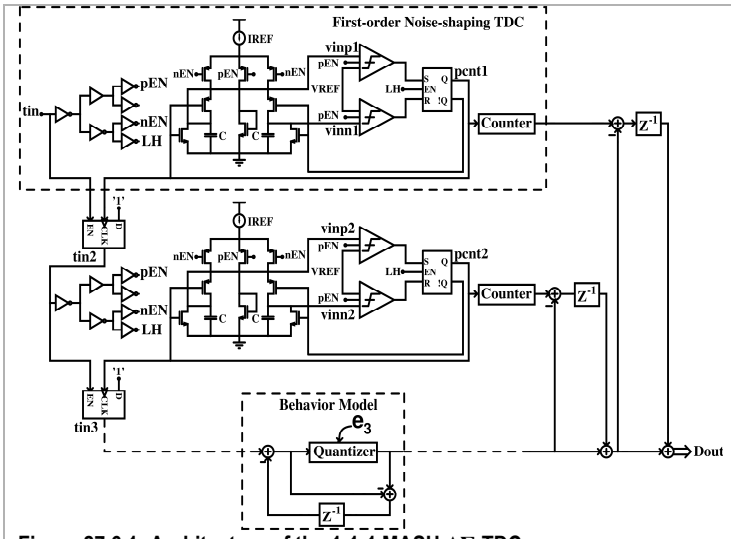

Figure 27.6.1: Architecture of the 1-1-1 MASH ΔΣ TDC.

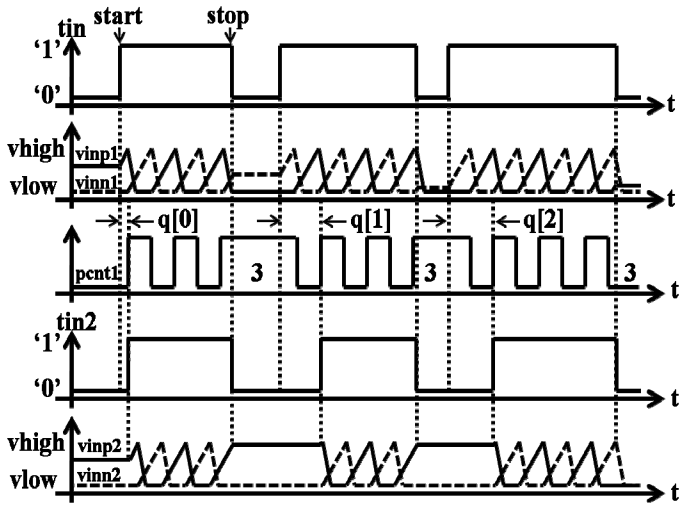

Figure 27.6.2: Timing diagram of the 1-1-1 MASH ΔΣ TDC.

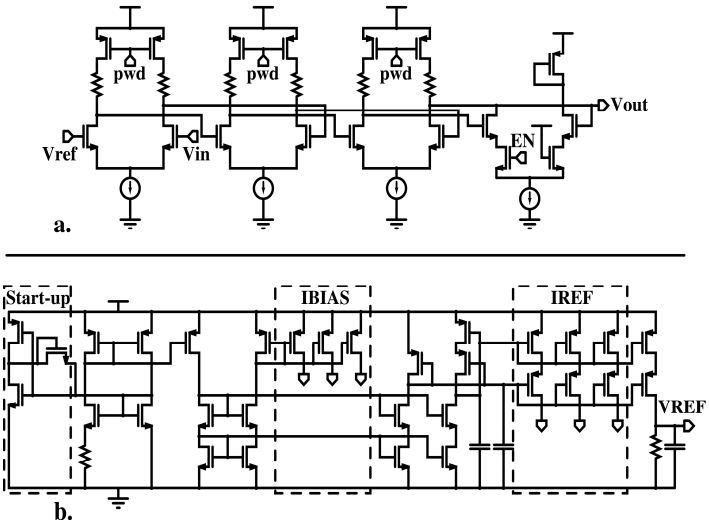

Figure 27.6.3: (a) Schematic of the comparator, (b) the reference voltage/current generator.

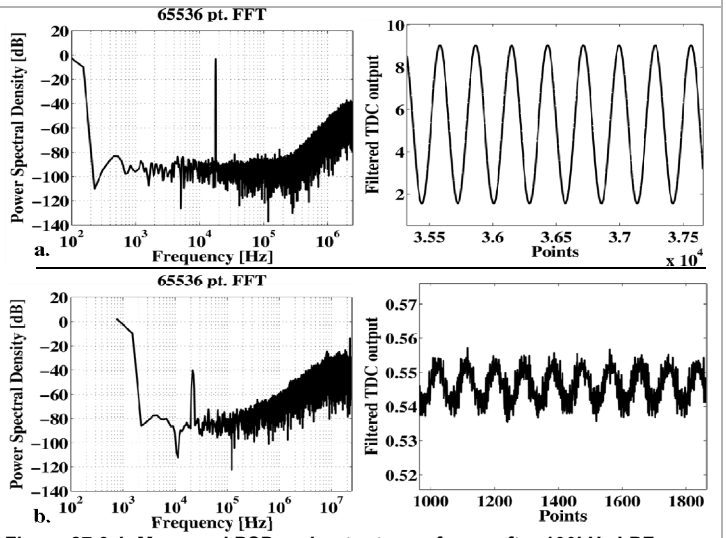

Figure 27.6.4: Measured PSD and output waveforms after 100kHz LPF.

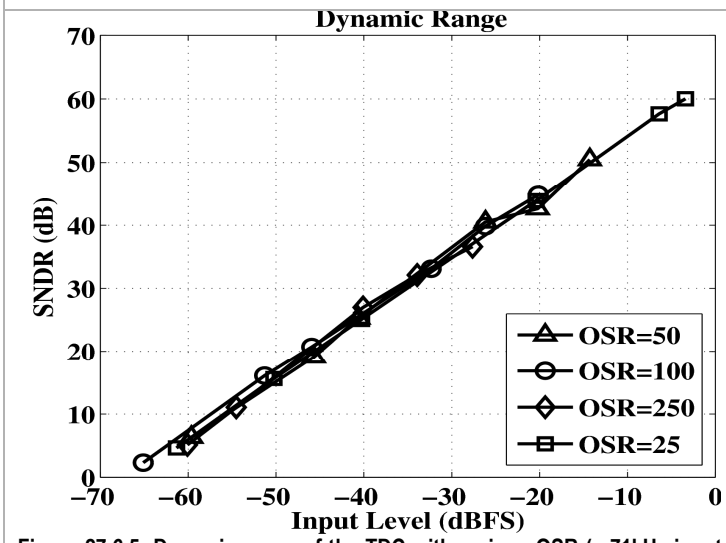

Figure 27.6.5: Dynamic range of the TDC with various OSR (a 71kHz input signal is applied).

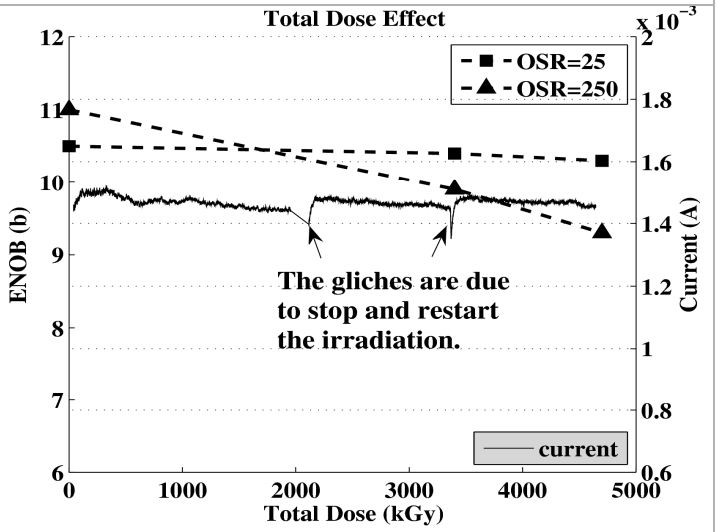

Figure 27.6.6: Total dose effect on the MASH ΔΣ TDC.