Low-Power Electronic Technologies for Harsh Radiation Environments

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Abstract

Electronic technologies that can operate in harsh radiation environments are important in space, nuclear, and avionic applications. However, radiation-hardened (rad-hard) integrated circuits often require additional processing and more complex configurations than conventional systems. Here, we review the development of low-power rad-hard electronics, examining the underlying phenomena of radiation-induced electronic failure and the design methodologies available with conventional complementary metal–oxide–semiconductor (CMOS) technologies to mitigate the problem. We also explore the potential of various emerging memory technologies in the creation of rad-hard electronics. Finally, we consider the potential rad-had applications of emerging memory technologies.

1 Introduction

Electronic technologies can now be deployed almost anywhere. This includes harsh and inaccessible environments that require technology that operates under high pressures and temperatures, and in high concentrations of toxic/corrosive gases and levels of radiation. The use of appropriate packaging schemes allows electronics to operate under most of these conditions. However, exposure to radiation often leads to an invasive process that causes irreversible damage to the packaged semiconductor devices due to ionization and collision phenomena generated by high-energy photons and particles. In such circumstances, packaging and shielding are often ineffective and can even exacerbate the impact of radiation owing to nuclear reactions induced in the packaging materials.

The source of these high-energy photons and particles are either natural (extra-terrestrial and terrestrial) or generated artificially in facilities like nuclear power plants or particle accelerators (Fig. 1). The impact of radiation on electronics depends on the characteristics of the radiation environment, and thus the requirements of a system will depend on where the electronics will be deployed. For example, the Curiosity probe, which was sent to the surface of Mars, required high resilience towards cosmic radiation, especially p^+ radiation from solar activities, since Mars has a low-density atmosphere and no global magnetic field to shield its surface.[1] A future destination for interplanetary exploration missions is Europa, one of Jupiter's moons, and the probes will face even more extreme β, p^+ radiation, as well as energetic oxygen and sulfur ions originating from Europa's plasma conditions and the strong magnetosphere of Jupiter.[2]

Furthermore, the orbital infrastructures located near the Van Allen belts — such as geostationary (GEO) and global positioning system (GPS) satellites, and the International Space Station (ISS) (at high, medium, and low earth orbits, respectively) — are irradiated by trapped β and p^+ radiation that could damage their electronic systems.[3–5] Maintenance and replacement in such inaccessible environments involve high cost and risk. For example, sending a replacement unit to the ISS costs US$ 10,000 for each pound of payload.[6] Radiation-hardened (rad-hard) technologies thus have a crucial role to play in space exploration and long-distance communications.

Radiation-induced electronic failure is also an increasing concern in avionics and even ground systems. The n^0 and p^+ particles coming from the atmosphere have been found to be responsible for autopilot upsets that occur on average once in every 200 flight hours, as well as electrical upsets in automotive electronics and data centers.[3,7] In addition, the intense particles and X-rays of solar flares can ionize and increase the density of the low layers of the

ionosphere, respectively, and interact with electromagnetic waves leading to disturbances in high-frequency radio communication systems.[3] These problems affect the stability of flight systems, traffic operations, and navigations both in airspace and on the ground, where safety is of primary importance. Similarly, the operation of nuclear facilities in a safety-critical manner is essential, and rad-hard technologies are commonly employed to enhance the overall safety margins.[8] Moreover, radiation effects are a concern in medical and industrial equipment, where X-ray and β radiations are used for therapy and diagnostic purposes. In high-energy physics facilities, various particles and photons are also generated by collisions in particle accelerators, creating challenges for the accelerator instrumentation and radiation detection, data acquisition, and communication.[9]

Rad-hard integrated circuit technologies often require additional processing and more complex configurations than standard fabrication flow. This makes rad-hard electronics, particularly low-power electronic technologies, difficult to keep pace with the International Technology Roadmap for Semiconductors (ITRS).[10] In this Review, we examine the latest logic and memory design techniques for radiation effect mitigation and explore the future development of rad-hard technologies.

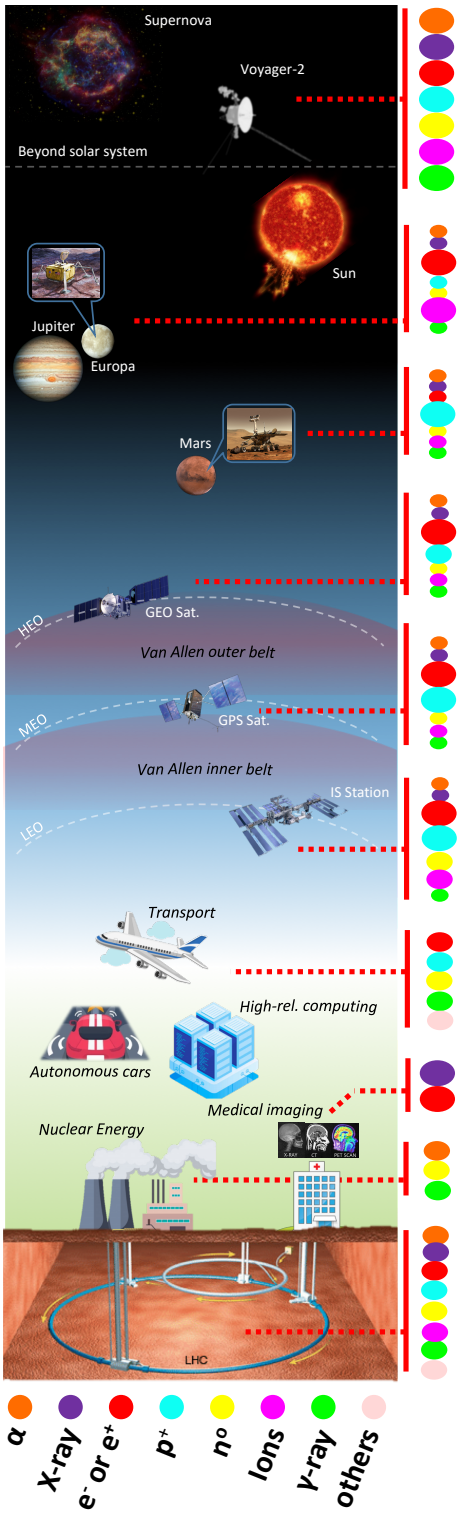

Figure 1: Energetic radiation environment. (a) Cosmic galactic radiation is the result of galactic events, such as supernova explosions and pulsars that emit γ-ray and high energy particles (83.3% p^+, 13.72% α, 2% β, 0.98% heavy ions). (b) Another source at deep space is the cosmic solar radiation where it emits p^+, β, X-ray, and γ-ray; the concentration and energy of these components vary depending on the solar activities (solar wind, solar flare, and coronal mass ejections) that occur randomly.(c) The earth's magnetic field and atmosphere play a significant role in limiting some of these particles reaching the surface of the earth where they are trapped inside the Van Allen outer magnetic belt (it consists mainly of β), whereas the other cosmic particles interact with atmospheric particles producing β, p^+, and a small portion of heavy ions and trapped inside the inner belt. Thus, the Van Allen belts can be classified as a radiation environment located at the earth's orbital region. (d) Nevertheless, some of the cosmic radiation can still pass through these belts and react with the earth's atmospheric molecules (such as oxygen and nitrogen) producing n^0, p^+, and pions (π); the π eventually produces β pairs (e^--e^+)and neutrinos. In addition to these particles, γ-rays are also emitted from the atmosphere during thunderstorms. (e) Radioactive materials, such as uranium, thorium, and their derivatives, are another terrestrial radiation source which emit α, β, and γ-ray. Radiation can also be intentionally generated using radiation generators for medical and industrial purposes (X-ray and β) or particle accelerators (various photons and particles) and some are unwanted byproducts of nuclear reaction (α, β, n^0, and γ-ray) that are produced by power plant facilities. The contribution of each type of radiation varies depending on the location where the electronic is deployed as depicted in each zone, see supplementary Tables 1 and 2 for details. β represents e^- or e^+ particles

2 Physics of radiation-induced electronic failures

High-energy photons (X-ray, and γ-ray) and particles (n^o,β, p^+, α, and heavy ions) interact with their environment and may deposit energy into material along their path. This energy deposition may result in temporary or permanent effects in this material. The severity depends on the impact of the radiation on the physical or chemical properties of the material. For semiconductor devices, the impact predominantly occurs in the semiconductor and insulator materials, rather than in the metals. Radiation can result in both temporary and permanent damages which are classified into three classes: total ionization dose (TID), displacement damage (DD), and single event effects (SEEs), as depicted in Fig. 2.

Both photons and particles can ionize materials in semiconductor devices. The cumulative dose is quantified by the amount of absorbed ionizing energy per mass, having an SI unit of Gray (Gy; 1 Gy = 1 J/kg = 100 rad).[11] Current semiconductor circuits and systems suffer electrical degradation after several tens of Gy up to several tens of kGy for space certified components. A limited number of custom radiation-hardened components can sustain up to hundreds of kGy.[12] Fig. 2(a) shows a band diagram of a Metal-Oxide Semiconductor (MOS) device and the schematic of the TID degradation mechanism due to trapped charges in the surrounding oxide layers. The mechanism is started with the ionization of atoms resulting in electron-hole (e-h) pairs in the SiO_2 material (Fig. 2(b)); this process occurs in a few femtoseconds and requires approximately 17 eV per e-h pair.[11] Since the electron mobility is higher than the hole mobility, the electrons can easily escape the oxide material through the positively biased gate within a few picoseconds. A fraction of electrons recombines with the holes (Fig. 2(c)). Note that high-energy photons have a high charge yield and may generate a higher number of un-recombined holes compared to high-energy particles.[13] Hereafter, the holes drift toward the interface through localized states in the bulk Silicon where they may release protons (H^+) which are embedded as impurities in the crystal. The holes can be trapped in bulk defects or at the Si-SiO_2 interface (Fig. 2(d). The H^+, that also migrate to the interface, are known to cause depassivation of the Si-H bonds at the interface thus forming additional interface traps. The trapped charges are responsible for a degraded current gain and an increased recombination rate in bipolar transistors, reduced mobility, threshold voltage shifts, an increase of 1/f noise, mismatch and leakage current in MOS transistors.[11,12,14] From a circuit perspective, device TID effects deteriorate circuit behaviour and may lead to a

reduced performance to even complete failure in CMOS circuits and systems.

DD is a non-ionizing mechanism that is initiated by the collision of particles with the atoms of the semiconductor and may result in physical damage in the lattice. Photons can indirectly induce DD by producing secondary electrons having high kinetic energy.[11] The affected atoms may be displaced from their initial position, creating vacancy and interstitial defects in the lattice which may interact further to form cluster defects (Fig. 2(e)). The concentration of these defects may become significant upon continuous or repeated radiation exposure. The severity of the damage not only depends on the total radiation exposure time but also on the type of particles. A 1 MeV n^{o} can induce multiple collisions in the lattice (damage cascade) from a single incidence while a high atomic mass incident ion, such as 15 keV As (74.9 Da), may locally deposit a considerable amount of energy and melt the material forming amorphous clusters; the cluster size can be up to 5 nm.[15] These defects create deep-level traps within the bandgap and are responsible for the increase of recombination rates and the reduction of charge carrier lifetime (Fig. 2(f)).[15] As a result, DD increases the saturation voltage and a reduction of the current gain in a bipolar transistor.[14] Bipolar transistors start to degrade typically at neutron fluxes of 10^{10}-10^{11} while MOSFETs do not tend to degrade till 10^{15} n^{o}/cm^{2}; this indicates that bipolar transistor are more sensitive to DD than MOSFETs (CMOS) since the latter are surface devices which suffer less impact from bulk defects.[14] Also photovoltaic devices tend to degrade due to DD, which is a problematic issue in space where they are being used as the primary power source.[15] In addition, opto-electronic devices such as photodiodes used for instance in optical communication, but also in camera chips, degrade from the reduced charge carrier life-time as well.[16]

A one-time ionization event from an energetic particle hitting a semiconductor device can also induce severe temporary or permanent electronic failures. The mechanism of the SEE starts with the creation of e^{-}h pairs along the track of the impinging particle in the semiconductor material (Si), known as a charge funnel. The incidence angle, mass, and energy of the particle determine the density of the e^{-}h pairs in the funneling region (Fig. 2(g)).[17] The excess e^{-}h pairs will either recombine or be transported through drift or diffusion.[11] The actual SEEs are predominantly caused by the charges generated in the vicinity of the doped regions like the source and drain junctions of a MOS device. There, self-recombination cannot be the dominant response when the device is under bias and electric fields are present and most carriers will be transported. The transport of electrons follows a two-step process. A high number of electrons drift to the opposite polarity bias due to a strong electric field near the device's source and drain junctions (Fig. 2(h)), fol-

lowed by the diffusion of the remaining scattered electrons (Fig. 2(i)). This results in a parasitic current pulse in nanoseconds interval (Fig. 2(j)) with a steep edge (fast drift) followed by a long tail (slow diffusion). This charge spike may induce temporary (non-destructive) soft-errors (such as upsets and transients) or permanent destructive errors (such as latch-up, burnt-out, gate rupture, and snap-back) in the circuit.

The concurrent effect of TID and SEEs in CMOS devices has changed over time with technology scaling. Threshold voltage degradation in MOS devices is proportional with the square of the gate-oxide thickness $t_{ox}{}^2$.[18] Therefore, scaled devices are generally more resilient to long term degradation induced by trapped charges in the gate-oxide. However, the present deep sub-micrometer technologies have very thin gate oxides which cause minimal impact and the remaining effects are mostly dominated by trapped charges and interface traps in the surrounding oxides like STI and SiN spacers or fin oxides[19] and are far from negligible, especially at MGy dose levels. The actual TID impact on the devices can be very different between technologies and even between foundries and are highly dependent on sizing, bias conditions and even temperature. For SEEs the general tendency is opposite meaning that they become worse in deep sub-micron devices due to shrinking node capacitances and reduced supply voltages. The amount of radiation induced charges becomes larger relative to the functional charge in the devices increasing the amplitude of the transients and the amount of upsets. The smaller device sizes also result in a higher probability of single particle strikes affecting multiple devices increasing the number of multi-bit upsets.

The radiation levels on earth are considerably lower than those in space and it would take many decades for TID or DD to become an issue. However, even at a very low dose rate, every single energetic particle (especially α and n^o) can potentially induce an SEE in high-altitude and on-ground systems.[11] Therefore, SEE is the most challenging issue in the terrestrial environment. Radiation hardening techniques are commonly used to mitigate upsets and latch-up in memory cells and logic devices, respectively.[11] Notwithstanding, TID may still be a concern for medical and industrial electronics where high-energy photons and particles are often used for therapy, sterilization, and inspection and definitely for instrumentation in nuclear energy facilities and high-energy physics experiments where dose levels can go up to several MGy.

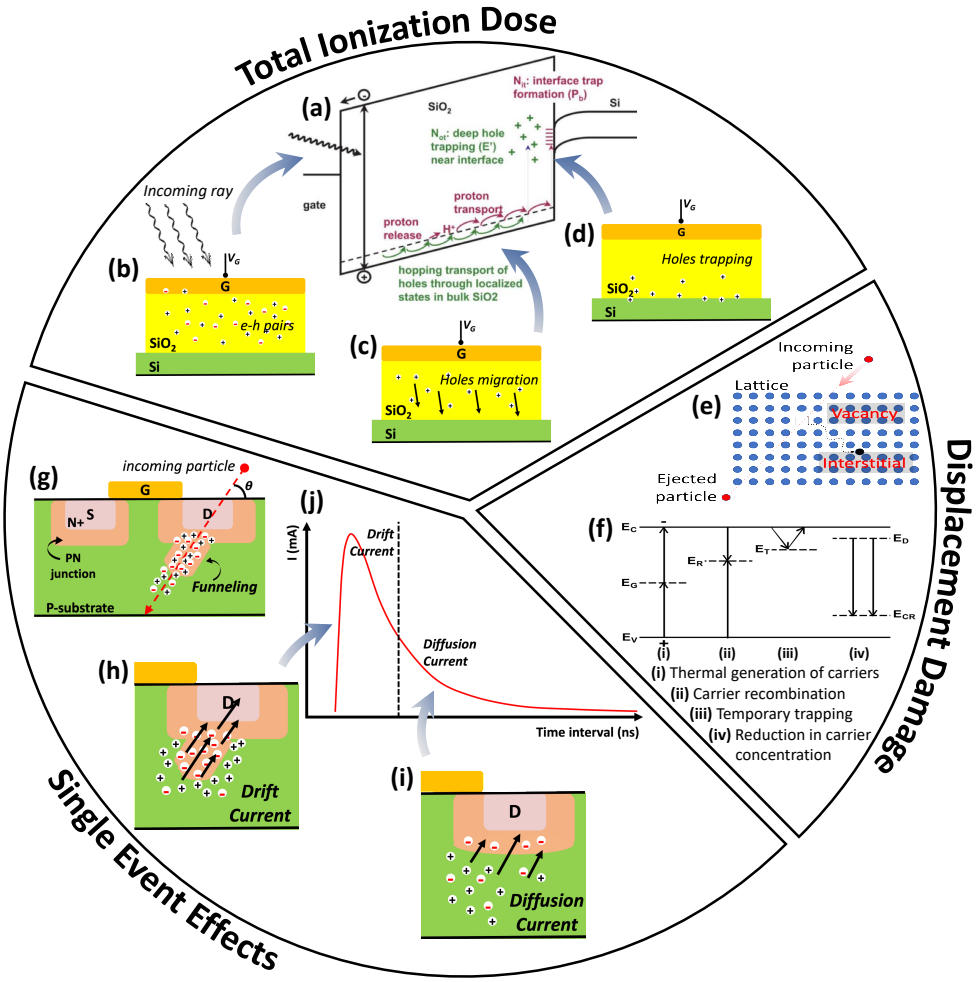

Figure 2: The routes of radiation damage in electronics. Total ionization dose (TID), displacement damage (DD), and single event effects (SEE) could lead to damages in semiconductor devices. (a) TID is a cumulative charge incidence phenomenon contributed by (b) e-h pairs generated in the oxide, (c) low mobility holes that slowly migrate through localized states and (d) holes trapped at the interface region. (e) DD is a cumulative collision phenomenon where particles alter the position of atoms in the semiconductor lattice affecting (f) carrier recombination, trapping, and concentration. (g) SEE is a single charge incidence phenomenon induced by particles hitting the device creating e-h pairs along its trajectory and generates (h) drift and (i) diffusion currents, (j) despite the current spike occurs in a few nanoseconds it can lead to either temporary or permanent failure. Schematic in (a) is (© [1969] IEEE. Reprinted, with permission, from [Radiation Effects in MOS Oxides, Schwank, James R., Shaneyfelt, Marty R., Fleetwood, Daniel M. et al, IEEE Transactions on Nuclear Science Vol 55 Issue 4 Pages 1833-1853, DOI:10.1109/TNS.2008.2001040]).[13] Schematics in (b-d) and (g-j) are adapted by permission from [Springer Nature Service Centre GmbH]: [Springer] [Proceedings of the 3rd Brazilian Technology Symposium][17](Overview About Radiation–Matter Interaction Mechanisms and Mitigation Techniques, R. N. S. Raphael, L. E. Seixas, Agord M. Pinto et al), [Springer International Publishing AG, part of Springer Nature 2019] (2019). Schematics in (f) is © [2013] IEEE. Reprinted, with permission, from [Displacement Damage Effects in Irradiated Semiconductor Devices, Srour, J. R. and Palko, J. W., IEEE Transactions on Nuclear Science Vol 60 Issue 3 Pages 1740-1766, DOI: 10.1109/TNS.2013.2261316][15]

3 Radiation Hardening by Design

Integrated circuits and systems can be protected from radiation effects using a variety of techniques across distinct design levels, taking into account: (i) Layout, (ii) Circuit techniques and (iii) System level mitigation techniques.[20] Since SEEs and TID effects differ in terms of timescale and device impact, their mitigation methods are different too. Layout techniques are more generic and can be applied broadly.[18] Circuit and system level mitigation approaches are, however, more specific and generally distinct strategies exist for digital and analog circuits,[21] with an exception at layout level. Fig. 3 shows various radiation hardening techniques for CMOS implementations. Note that radiation hardened processes are an alternative strategy but they come with significantly higher development cost and often a lower performance.

Long term radiation exposure may result in positive trapped oxide charges. Following Moore's scaling trend, the gate oxide thickness has shrunk dramatically and secondary oxides, mainly SiN spacers and Shallow Trench Isolation (STI) became primary hotspots.[19] Trapped charges in the SiN spacers influence the local potential in lightly doped LDD (Local Drain Diffusion) regions (Fig. 3(a)).[22] For PMOS transistors, p-doped LDDs become highly resistive, rendering an overall increase of the channel resistance. For NMOS transistors, n-doped LDDs become more negative making LDD less effective for hot carrier degradation; the reason why LDD is used. For long channels, the effect is relatively less dominant than short channels due to an unaffected central region. Charges trapped in the STI regions affect the local threshold voltage in the channel edge, as is shown on Fig. 3(b), similarly to trapped charges in the gate oxide.[23,24] This results in an increased leakage current for NMOS devices.[25] Since trapped STI charges only affect the channel edge, wide devices suffer relatively less than narrow devices.

A generally effective technique for mitigating long term degradation in deep-submicron technologies is using long and wide devices. Large widths are often unfavorable due to power consumption and area constraints. To overcome STI edge effects, an edgeless transistor can efficiently mitigate these effects, as shown on Fig. 3(c). The Enclosed Layout Transistor (ELT) has its drain in the middle, enclosed by the channel and no STI touching the channel.[26,27] However, design rule compliance and matching becomes more challenging. Mitigating SEEs at layout level can also be done by adding reverse biased guard rings nearby sensitive nodes, as depicted on Fig. 3(d).[28] Large reverse bias voltages and depletion regions enhance charge collection capabilities so electron-hole pairs in the substrate are diverted towards the guard rings. Alternative structures like dummy junctions are often used to

save area.[29] These techniques can be applied for different circuits, which makes layout techniques the preferred option for rad-hardening.

At circuit level, many mitigation methods exist for different circuits. The most popular technique for SEE mitigation is employing the concept of Triple Modular Redundancy (TMR), shown on Fig. 3(e). Digital logic, consisting of sequential and combinational logic, is implemented thrice such that single logical errors can be corrected. Voters select the majority of the inputs and implement single error correction.[30,31] In nanoscale technologies, single particle strikes can affect multiple gates simultaneously, hence gate spacing becomes mandatory to prevent multi-cell upsets.[32] Unfortunately, TMR results in a more than 3x power, area and speed penalty due to the voters and long interconnects. To alleviate these drawbacks, several alternatives are possible[33,34]

Instead of logic level triplication, these individual gates can be hardened by design too. The DICE (Dual Interlocked Cell) latch, shown on Fig. 3(f),[35] is an example of a radiation hardened latch. Instead of using two storage nodes, an additional pair is added. The latching positive feedback runs in both directions in the circuit but if an SEE occurs at any node A-D, the SEE can never propagate through the entire loop and will be blocked by an inactive device.

For analog circuits, SEE mitigation is less trivial. Redundancy can be used here, for instance in current mirrors, where each gate finger of the input device is connected to each individual finger of the output device resulting in a reduction of a single finger transient by the amount of fingers used. This requires higher bias currents and thus comes at the expense of the overall area and power needed. Another commonly used technique is to increase the sensitive node capacitance to reduce voltage disturbances. This however comes at the cost of speed or power. However, for DC circuits like bandgaps and biasing circuitry, capacitive decoupling, capacitive negative feedback or intermediate low pass filtering are simple and efficient.[36,37] For fast signaling, Differential Charge Cancellation (DCC) mitigates SEEs in analog differential circuits.[38] Two closely spaced junctions can share the charge of a particle strike, as shown on Fig. 3(g). If those drain junctions operate differentially, as shown on Fig 3(h), the shared charge acts as a common mode signal to the circuit and can thus be easily suppressed.

At system level less generic and more specific mitigation is used. For instance, processors can use software level mitigation like signatures or tightly coupled cores, executing the same program.[39] For memories, several generic techniques exists, like error correcting codes (ECC),[40] data scrambling[41,42] and memory scrubbing.[41,43] ECC uses coding schemes with redundant bits for error correction. Depending on the ECC, single or even multiple errors

can be detected and corrected. Hamming codes are frequently used with single bit correcting capability although multiple errors in a single word are non-correctable unless more complex codes are used. As shown on Fig. 3(i), standard physical word placement can be susceptible to multi-bit upsets in adjacent cells. Data scrambling is an effective technique to distribute same word bits physically such that multi-cell upset clusters do not affect multiple bits in a word.[41,42] Hence, each affected bit is correctable. If bits become corrupted in the memory, they remain faulty until corrected. A methodology for on-line Error Detection and Correction (EDAC) is shown in Fig. 3(j). A dual port memory has both a memory scrubbing interface to continuously scan through the memory to correct erroneous words and an application interface. Memory scrubbing should be fast enough to prevent 2 different particles hitting the same word between ECC checks.[41,43]

As previously noted, the CMOS process itself has an important impact on the radiation hardness. Aside from bespoke radiation hardened technologies, a variety of alternative, commercially available, CMOS technologies exist: bulk CMOS, Silicon-on-Insulator (SOI) and FinFets with varying radiation responses.[44–46] The above mentioned effects apply specifically to conventional planar CMOS devices on a bulk Si substrate, shown in Fig. 4(a). SOI transistors, alike the ones shown in Fig. 4(b), are intrinsically less susceptibility to SEEs due to the buried oxide (BOX) layer that isolates the channel from the substrate.[47] In a similar fashion to bulk-CMOS, particles create an ionization track deep in the substrate, yet, deep substrate charges cannot migrate towards the junctions since they are isolated by the BOX. Hence, only a fraction of the total generated charge is collected. However, the additional BOX layer comes at the cost of a thick oxide facing the entire channel area where charges can be trapped, similarly to the gate oxide, resulting in threshold voltage shifts.[44] State-of-the-art ultra-thin SOI processes employ BOX thicknesses in the range of 7-15 nm[48] and their TID radiation hardness compares to 0.35 μm - 1 μm bulk CMOS technologies. The improved SEE sensitivity and moderate TID degradation explains the success of SOI technology for many space applications, where the total doses are rather limited. As BOX thicknesses have shrunk over time, they have become useful as secondary gates to adjust the threshold voltage of the devices offering the ability to cancel threshold voltage shifts.[49]

In contrast to planar CMOS technologies, FinFets are 3D structures with surface conductivity at different edges of the fin. As illustrated in Fig. 4(c), thick oxides are not in direct contact with the active regions and improved TID sensitivity is therefore expected. However, since the devices have become extremely small in terms of volume, trapped charges in surrounding oxides can indirectly impact the channel region.[50] For SEEs, if particles

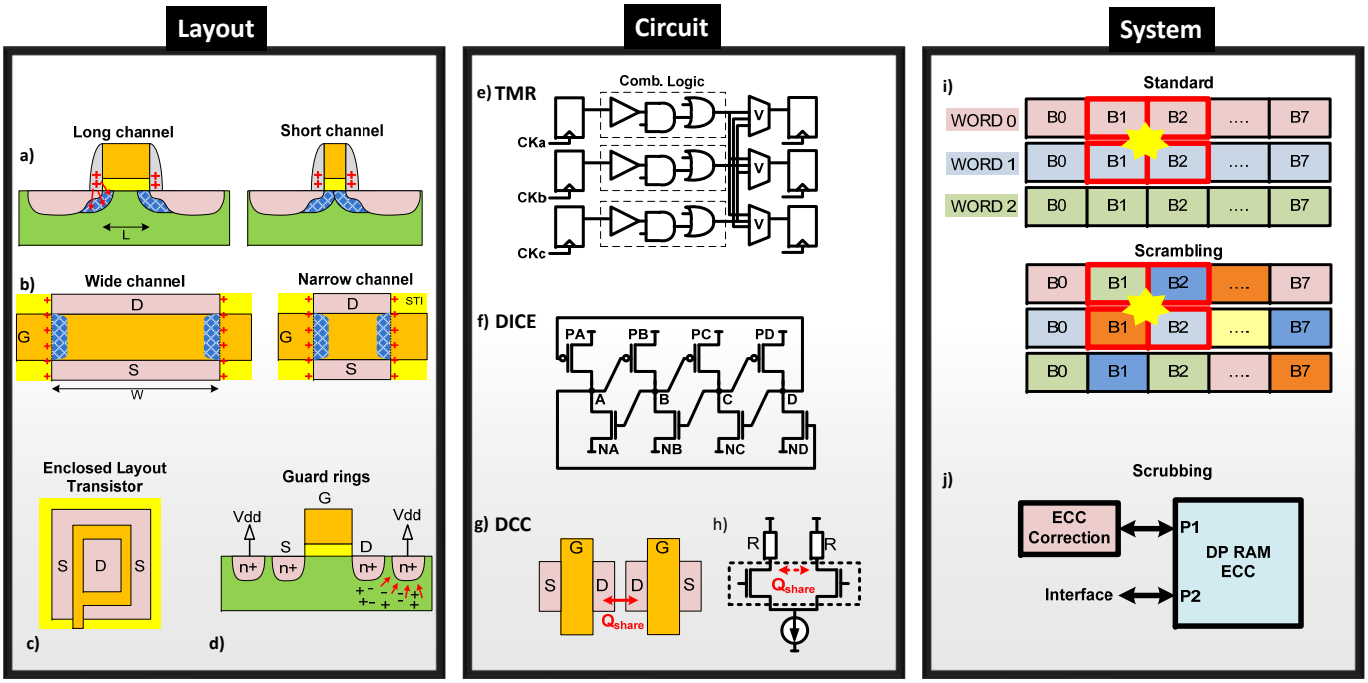

Figure 3: Radiation Hardening by Design (a) Short channel effects from trapped charges in the SiN spacers. (b) Narrow channel effects from trapped charges in the STI. (c) Enclosed layout transistor (ELT) layout to avoid STI contact with the channel. (d) Reverse biased guard rings near the sensitive nodes to divert charges. (e) Triple Modular Redundancy (TMR): Logic cells are triplicated. Both sequential cells and combinational cells can be redundant. Voters are inserted for single error correction. (f) Dual Interlocked Cell (DICE): Radiation hardened latch with an additional storage pair and interlocked connectivity. (g) Differential charge cancellation (DCC): Charge sharing by closely spacing differential nodes to convert disturbances to a common mode signal. (i) Multi-Bit Upsets (MBUs) in memories can be mitigated by distributing common bits spatially such that a single particle cannot affect multiple bits of the same word. (j) Continuous read and correction of a memory to correct for single accumulated errors.

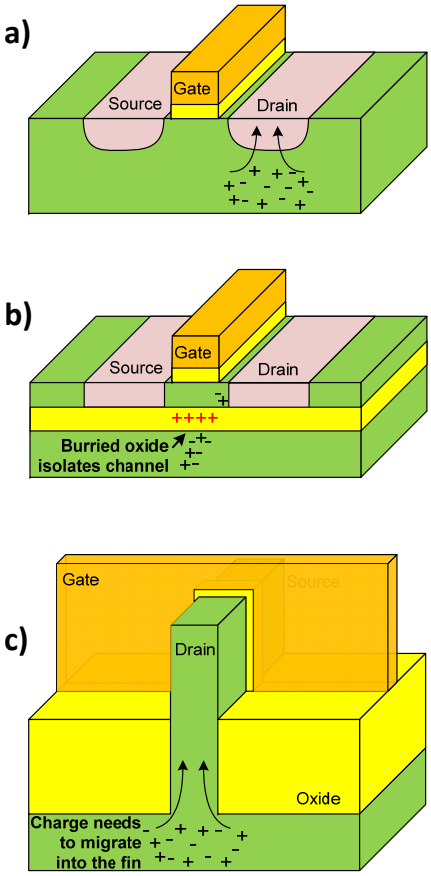

Figure 4: Radiation effects in advanced CMOS devices (a) In Bulk CMOS, charges in the substrate can migrate towards the S/D junctions. (b) In SOI devices, the buried oxide isolates the channel and junctions from the substrate and only a fraction of the charge is collected. Charges can however be trapped in the relatively thick oxide. (c) In FinFets, the active region is on the top of the fin. Charges need to diffuse in the fin which is less efficient.

hit the fin directly, these charges can be captured by the junctions. This probability is however relatively low and due to the limited volume, a small amount of charge can be generated in the fin. The remainder of the charge is typically deposited in the substrate and overall charge diffusion into the fin is limited.[51,52]

4 Radiation Effects in Integrated Memories

Memories are often tailored to achieve high density (bits/area) with specific device structures, each having radiation assurance concerns. Different memory technologies like SRAM, DRAM, flash, MRAM and ReRAM have different performance trade-offs such as volatility, access time, power consumption and compatibility with CMOS platforms.[53] Bi-stable Static Random Access Memories (SRAM; Fig. 5(a)) are widely used as local on-chip memories due to their fast operation and integration with CMOS processes. Information is retained on two complementary circuit nodes through positive feedback, however, SEEs can result in a bit flip if sufficient charge is injected. This charge is known as the critical charge, Q_{crit}, which depends on the node capacitance, device strength (or feedback) and supply voltage.[54,55] Reducing any of these parameters reduces the radiation resilience, which explains why nanoscale technologies have become more sensitive to SEEs.[55] Circuit hardening techniques like capacitive and resistive decoupling[56–59] and system level mitigation, discussed in Section 3, improve robustness significantly. Dynamic Random Access Memories (DRAMs) rely on charges stored on capacitors (Fig. 5(b)). SEEs result from charge deposition on the storage capacitor, corrupting the stored (multi-level) information, although errors in surrounding logic contribute too.[60,61] Smaller capacitances and multi-level schemes make DRAMs more sensitive to upsets.[62]

Flash memories are non-volatile elements with charges stored on a floating gate, shown in Fig. 5(c). The device is read by measuring the threshold voltage of the MOS structure which depends on the floating gate charge. Similarly to DRAMs, multi-level flash memories are used today. Due to TID, positive charges may accumulate in both oxides and will neutralize electrons in the floating gate resulting in a threshold voltage shift over time.[63] Therefore, memory cells will become corrupted as the ionizing dose increases and in contrast to general CMOS scaling, the tunneling oxide thickness of floating gate devices is not shrinking significantly beyond 7 nm.[64] Multi-bit storage makes flash memories more susceptible due to smaller margins.[65] . Since the floating gate is isolated from active regions, SEEs cannot corrupt information directly but can occur due to configuration upsets or readout errors.[66]

DRAM, SRAM, and flash technologies are all suffering from scaling issues and struggle to keep up with Moore's Law.[10] Various emerging non-volatile memory technologies are being proposed to replace them, such as ferroelectric-RAM (FeRAM), phase change-RAM (PCRAM), magnetic-RAM (MRAM), and Resistive-RAM (ReRAM). Here we ruled out FeRAM and PCRAM due to several challenges that hinder their potential as future rad-

hard memory. Specifically FeRAM is sensitive to contamination during the back-end-process integration, while PCRAM is temperature-sensitive which makes it ill-suited for space and nuclear applications.[67] MRAM and ReRAM are considered as the forerunners due to their excellent performance, CMOS compatibility, and radiation tolerance.

The discovery of room temperature-giant magnetoresistance in 1988 had led to the rapid development of spintronic devices, particularly MRAM.[68] The MRAM device structure is based on metal/magnetic material/insulator/magnetic material/metal stack (Fig. 5(d)) and the tunneling conductance between this stack is controlled by the magnetization of the two magnetic materials, denoted as tunneling magnetoresistance (T-MR). The polarization of one of the magnetic materials is fixed (reference layer) while the other's polarization can be flipped (free layer) by a spin-polarized current inducing spin torque effect, and the device can be turned On and Off when the magnetic polarization of both materials are in anti-parallel and parallel, respectively.[68] In principle, the overall size of an MRAM cell can be miniaturized down to single nanometre scale, demonstrating MRAM's excellent scalability prospects. Moreover, the underlying mechanism relies on the current density rather than the absolute current which scales with the cell size.[68] In practice, however, scaling such technologies can be limited by the thermal stability factor (Δ) where decreasing the anisotropy of the magnetic material decreases Δ. Δ lower than 60 may result in an unstable magnetic moment and thus lead into poor memory retention at elevated temperatures.[69] SEEs can potentially induce bit flip soft-errors in the MRAM cell. Nevertheless, the occurrence probability is significantly lower compared to charge-based memories.[70] DD, however, can cause an issue when scaling down the MRAM cell, where the interfacial quality between the ultra-thin multilayers is difficult to maintain.[68] The energetic particles damage the interfacial structures forming an intermixing phase in the insulator degrading the T-MR effect.[68]

The ReRAM, that is part of memristor (memory-resistor) technologies, has a simple metal/insulator (storage layer)/metal sandwich device structure (Fig. 5(e)). Various materials can serve as the insulator (oxide, chalcogenide, nitride, or polymer), and it can be designed in such a way as to exhibit digital or analog behaviour.[71] The switching mechanism of such memristor cells is controlled by the movement of anions and cations under an electric field. This ionic movement induces the formation and rupture of a conducting filament/region (consisting of donor defects (valence-change type), or metallic ions (electrochemical type)) that controls the electron flows in the cell. This phenomenon can be traced back to 1962,[72] and yet it had not gained enough attention until the HP Labs showcased its potential for the next-generation high-density data storage in 2008.[73] The memristor shows the potential of

scalability towards 10 nm node[74] and the insulator can be thinning down to sub-10 nm.[75,76] Such a thin insulator will only absorb very little energy from the radiation, which makes memristor an intrinsically rad-hard element.[77] Memristor cells are sufficiently high resistant to SEEs (bit flips only occur due to the transient photocurrent effect originating from the nearest neighbor transistors not from the memristor cell itself)[78,79] and a very high fluence (above 10^{18} 1-MeV-equivalent-neutrons/cm^2)[80] or dose (tens to hundreds of kGy)[81,82] is required to show noticeable effects on the cells due to DD and TID, respectively. Such a high dose is above the minimum requirement for space electronics.[83] The radiation could induce defects generation[84,85] and, in some cases, phase transformation in chalcogenide[86] and oxide[81] materials. Hence, comparison studies between the switching mechanism of valence-change and electrochemical types performing in radiation rich environments should be further explored.[86] Any of these radiation-induced defect/phase changes may lead to an increase in leakage current, a decrease of the memory window and switching instability, and overall variation of switching parameters. Nevertheless, this form of degradation does not significantly affect any digital functionality.[87,88] The defects generation could become a problematic issue when it degrades the synaptic functions[79,89] (such as dynamic range and linearity properties, (Fig. 5(e)) of the analog memristors where these metrics are particularly crucial for the realization of in-memory computing and bio-inspired computing applications.[90]

SRAM, DRAM, and flash are commercially available memory technologies in the market. SRAM and DRAM serve as the primary (system) storage since they can perform high-speed switching and robust endurance while flash serves as the secondary storage due to its non-volatility characteristic. MRAM and ReRAM are non-volatile memories and their performance is much better than flash and almost as good as SRAM and DRAM.[53] Henceforth, these two emerging technologies could serve as universal memories for both primary and secondary data storage (Fig. 5(f)). The use of non-volatile memories as the primary storage is beneficial for achieving disaster-resilient computing where the system can retain the computation result after a sudden loss of power, which can be caused by cosmic radiation.[3,70] MRAM, however, still can suffer from SEE and DD while ReRAM appears to be susceptible to DD. Whilst both technologies appear to be appealing for rad-hard electronics applications, additional efforts are needed for benchmarking their resilience to DD and SEE. Nevertheless, MRAM cells are used in series with a transistor as the selector element in an array configuration (1T1MTJ).[53] Hence, the array is prone to the three types of radiation damage. Meanwhile, for ReRAM, the transistor can be replaced with a Zener diode (1D1R). The Zener diode has the same sandwich architecture as ReRAM which could have

high resiliency in highly radiative environments as ReRAM does. Moreover, this diode's architecture is advantageous to retain the maximum achievable scalability in the array configuration. This makes ReRAM more appealing for rad-hard electronics than MRAM.

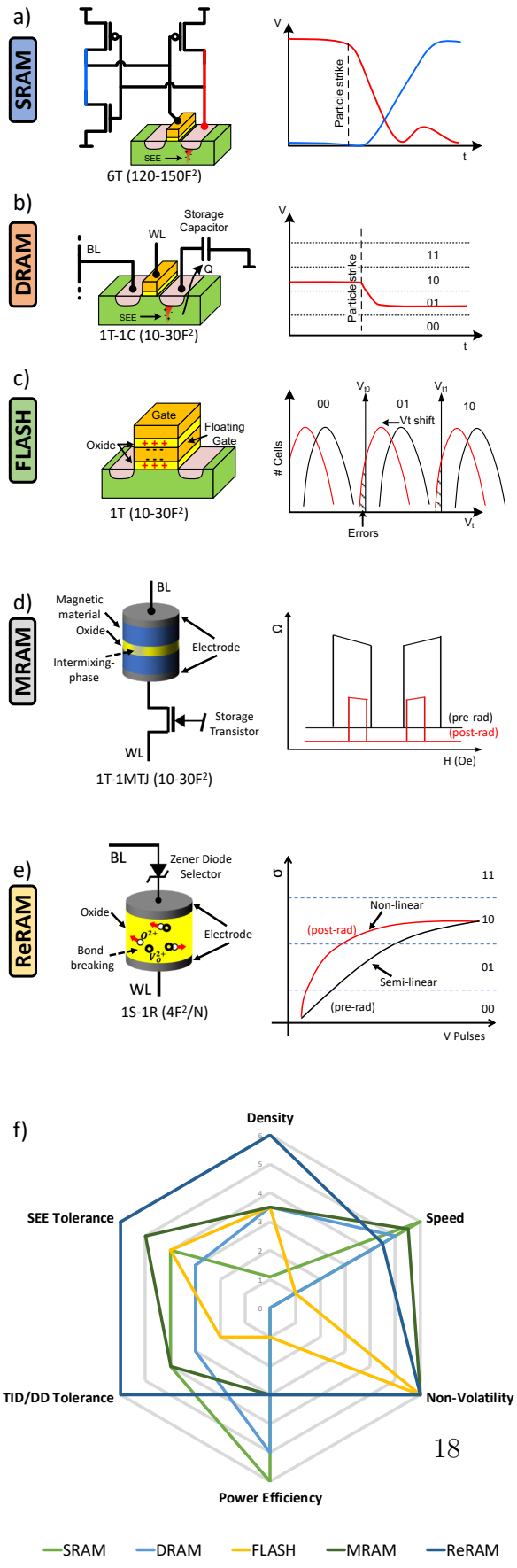

Figure 5: Radiation effects in memory technologies. (a) SRAM devices store information on two complementary nodes. An SEE on each node can flip the state of the cell. With sufficient charge and due to positive feedback, the other node will also flip. (b) DRAM devices can store multiple bits on a single capacitor. SEEs on the switch transistor inject charges on the storage capacitor and the resulting voltage error can result in erroneous information. (c) Flash memories are non-volatile devices that rely on fixed charges in a floating gate which are measured through threshold voltage shifts. Long term TID effects result in trapped charges in both oxides shifting the threshold voltage which results in faulty bits accumulated over time. (d) MRAM uses magnetization direction to store information through an ultra-thin barrier layer sandwiched between two magnetic layers. Radiation results in the formation of an intermixing phase in the barrier layer and deteriorates the tunneling magnetoresistance effect. (e) ReRAM is based on ionic movement and the defects concentration inside the switching layer controls this movement. Radiation induced defects generation can occur after a huge dose of radiation and increases the leakage current. (f) Performance comparison of the different memory technologies.[53,61,66,70,78,91–95]

5 Outlook

CMOS technology scaling has led to a massive increase in system complexity and performance. Logic gate delays have shrunk to less than 10 ps enabling multi-GHz operation with up to a billion transistors on a single chip. In addition, the overall memory capacity and bandwidth have increased in modern systems. These improvements have fuelled a series of disruptive developments in areas such as machine learning, artificial intelligence (AI), computer vision, and autonomous decision making.

Total dose and displacement resilience generally improve with device scaling, allowing circuits to survive higher radiation doses. Therefore, it should be easier for new CMOS platforms to find their way into avionic, space, and nuclear applications. This could lead to a variety of developments: AI in space; consumer electronics in cubesat missions; intelligent computer vision algorithms in nuclear fusion and fission reactors; and self-exploring unmanned vehicles for nuclear accident intervention and dismantling. Improved radiation hardening techniques can also enhance the lifetime of a system in these environments, and could lead to additional uses in high-dose applications like particle accelerator and detector instrumentation. On the other hand, as small technological nodes become more sensitive to SEEs, transport applications like airplane autopilot systems, railway systems, and the emerging field of autonomous cars (which strongly rely on advanced signal processing and AI) will require fault mitigation strategies at circuit, system or software level. Resilient implementation of next-generation electronic technologies with little overhead (performance, power, and cost) is thus the key to unlocking these future applications.

MRAM and ReRAM technologies show potential for replacing SRAM and DRAM as primary storage due to their non-volatility, which can support a variety of fault mitigation strategies and allow disaster-resilient computing to be more easily implemented. The drive for commercial space flights also requires the development and use of reliable and compact electronics that can help reduce launch and maintenance costs. MRAM and ReRAM technologies are a good fit for such requirements due to their excellent rad-hard performance, low-power consumption, high density, and independence to auxiliary components (in contrast to SRAM and DRAM, which should be backed by battery and capacitor cells, respectively).

The potential role of emerging non-volatile memories becomes more significant in applications that rely on functions beyond storage (Fig.6). ReRAM, as an adjustable resistor, can replace the conventional resistor in passive circuits to make them tuneable and, likewise, may minimize the use of tuning transistor in active circuits; this technique could reduce the power dissipa-

tion and increase the density of the circuits due to its non-volatility and small feature size, respectively, leading to lower costs of deployment. ReRAM offers the flexibility to implement programmable logic. Flash-based FPGAs can benefit from the radiation hardness of ReRAM, making them a suitable alternative to implement configuration memory for non-volatile FPGAs. It could also be exploited for non-volatile circuit applications, such as physical unclonable functions (PUFs). PUFs are unique, uncontrollable, and unpredictable fingerprints used in crypto-graphic challenge-response authentication, where they rely on semiconductor variability in oxides, which tend to be sensitive to radiation. To resolve this issue, PUFs could exploit the analogous variability of ReRAM, providing alternative architectures with increased robustness.

Recently, ReRAMs are also being explored in various sensors due to their ability to respond to external stimuli. Furthermore, SRAM memories have started to be implemented as a radiation detector where the number of bit errors gives an estimation on the radiation intensity; the sensitivity of the cells is adjustable by altering their supply voltage.[96] Recent works on SRAMs have proposed to use both single-bit and multi-bit upset data to even estimate the energy levels of the environment. A similar methodology can be applied to ReRAM too. Moreover, emerging memory technologies have been considered for brain-inspired (neuromorphic) computing to overcome the bottleneck of von Neumann's computer architecture and making in-memory computation possible. Although MRAM has superior performance than other emerging memory technologies, it requires complex circuit designs due to its small dynamic range.[97] ReRAM is thus the most feasible choice for enabling AI machines in space and nuclear environments.

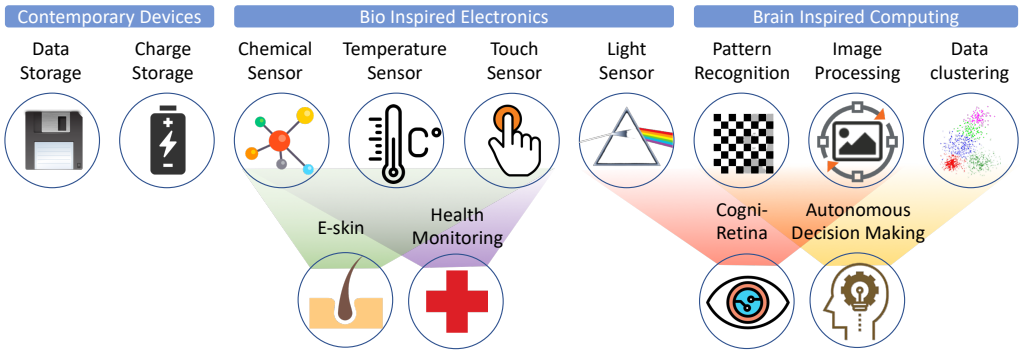

Figure 6: Prospective rad-had applications of emerging memory technologies. Memristor technologies are based on electrochemical phenomena which offer broad applications beyond data storage. A non-zero-crossing I-V characteristic was observed in memristor cells due to the excess concentrations of charged species, inducing electromotive force in the cells that indicate nanobattery behavior.[98] The I-V characteristics can also be modulated by external stimuli such as chemical (liquid and gas),[99,100] temperature,[101] touch,[102] and light[103] which shows the potential for sensory applications. The integration of these sensors could make up artificial skins[104] useful for health monitoring systems.[105] Furthermore, the electrochemical process in memristors can mimic the synaptic plasticity of the biological synapses. This neuromorphic capability opens the potential for in-memory computing and could revolutionize the traditional von Neumann's computer architecture.[106] Several neuromorphic computing applications have been explored, such as pattern recognition,[90] image processing,[107] and data clustering[108] where these functions push the computation capability in more complex machines, for example, cogni-retina for bionics/robotics,[109] and autonomous machines.[90]

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7 Author contributions

J.P., F.S., P.L. and T.P. conceived of the presented review. J.P. and F.S. performed the literature analysis. J.P. and F.S. wrote the paper with inputs from all authors. All authors discussed and contributed to the final manuscript. T.P. took the lead on the structure of the paper and figures.

8 Competing Interests Statement

The authors declare no competing interests.

9 Data Availability Statement

This paper contains no data.

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