Design of IEC 62132-4 Compliant DPI Test Boards that Work up to 2 GHz

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Abstract—**DPI (Direct Power Injection) testing according to IEC 62132-4 has been widely adopted as an effective test method for IC-level pin-selective RF immunity testing. To enable DPI testing of an IC, a dedicated test board needs to be designed that basically makes up the whole EMC test set-up. Boards that are designed in accordance with IEC 62132-4, should work well up to 1 GHz. However, various anomalies can occur if no proper care is taken of all possible RF phenomena. This paper explains our design approach to effectively deal with these issues and at the same time even extend the useful frequency range up to 2 GHz. Specific guidelines to achieve this objective are given.**

Keywords-DPI; IEC 62132; IC-level RF immunity; automotive EMC

I. INTRODUCTION

In order to arrive at an international standardization of IC-level EMC testing, the IEC SC47A subcommittee "Integrated circuits" has been developing three families of standards that describe test methods for RF emission (the IEC 61967 series), RF immunity (the IEC 62132 series) and impulse immunity (the 62215 series). Concerning RF immunity, IEC 62132-1 [1] explains the general conditions and definitions whereas the other parts (named IEC 62132-x with x ranging from 2 to 9) describe specific test methods (both conducted and radiated ones). From these various possible test methods, the DPI (Direct Power Injection) method that is specified in IEC 62132-4 [2], appears to be the most widely used technique, especially in automotive applications.

According to the authors, there are two main reasons why the DPI technique has established itself as the number one IC-level RF immunity test method: (1) once the test board is available (assuming it has been designed well), DPI testing is very simple and straightforward to perform, and (2) DPI testing can be easily simulated by chip designers using their standard design tools. No advanced EMC test or simulation expertise is required to perform or simulate DPI testing. For the testing itself, this is the case because all required EMC testing know-how is implemented already in the test board so the user doesn't have to worry about it. For simulations, this is the case because the higher-level EMC product specifications are translated to simple pin-specific DPI specifications. Obviously the latter translation is not straightforward and requires a lot of EMC know-how and application knowledge to do it properly. Typically, target DPI levels are specified depending on the type of application (safety-critical or not) and the type of pin (global or local) [3]. A better approach in specific cases is to carry out a more rigorous translation using EM (electromagnetic) field solvers [4].

In this paper, we focus on the design of the test board. Section II describes the main requirements that the test board has to meet. Next, in Section III, a general concept for the test board is explained whereas specific guidelines for sub-circuits are given in Section IV. Finally, Section V deals with board validation through simulation and testing whereas conclusions are drawn in Section VI.

II. RF DESIGN REQUIREMENTS

A DPI test board has to contain the following circuits: (1) a minimal application circuit that allows to operate the IC-under-test in all functional states that need to be tested, (2) RF injection circuits that enable to inject a calibrated RF forward power level in any of the pins-under-test, and (3) monitoring circuits that allow to monitor the IC performance during RF injection in one of the pins-under-test. In addition, the board has to contain a number of connectors to connect these on-board circuits with the off-board equipment needed for the testing.

In principle, the pins-under-test are tested one-by-one so there should be one RF injection path for each pin-under-test. However, in some cases (such as differential inputs or outputs) it can be interesting to test more than one pin at once using one RF injection path, but such multiple-pin injection is not considered in this paper for the sake of simplicity.

In order for a DPI test board to work properly up to high frequencies, the following RF requirements will have to be met:

- The RF injection circuits need to provide a low-loss 50-Ω injection path to each of the pins-under-test.
- At the connector side, they need to be terminated by a 50-Ω load (either a termination or a well-matched RF power injection system) and at the IC side by a coupling capacitor (or DC block) located as close as possible to the pin-under-test.
- These RF injection paths (or transmission lines) should be well isolated from each other and from the other

circuits so that no unintentional coupling of RF power can occur on the board.

- All other circuits (both functional and monitoring) that connect to the IC, should be RF-decoupled so that no RF power leaving the IC can enter them. This decoupling (RF blocking) should be located as close as possible to the connected pins to prevent that the connected lines act as antennas.
- Finally, sufficient care should be taken that no unexpected board resonances can be excited.

If the above requirements are met, there should be an unimpeded flow of RF power (both incident and reflected) through the RF injection path of the pin-under-test whereas no RF power should leak to any other circuit on the board and so get conducted or radiated off it.

III. General Design Concept

In order to enable the use of internal ground planes (as ground plane for the RF transmission lines and as RF shield between circuits located on the top and bottom side), it is advantageous to use 4-layer PCBs for IC-level EMC testing such as DPI testing. Fig. 1 shows the general cross section of the test boards that have been used in this work. It was found that this type of 4-layer FR4 board allowed us to design boards that worked well up to 2 GHz.

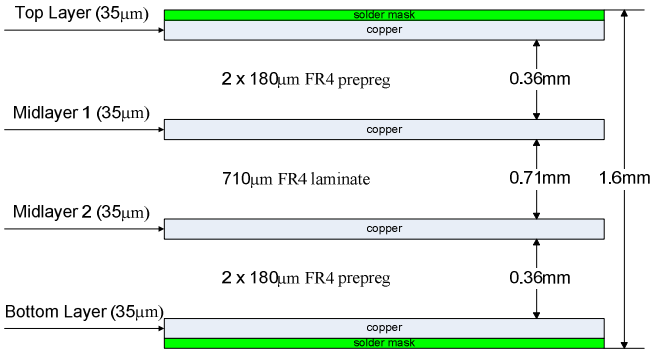

Figure 1. Cross-section of standard DPI test board.

Although the use of such a 4-layer board would make it simple to obtain a clean distinction between signal ground and RF ground with single-point connection at the IC, we found out that it is not a good practice to do so because there is a high risk that the board will become useless in some higher frequency ranges due to bouncing between these two grounds. Therefore, we recommend to use only one ground in DPI boards. In our preferred design, the layers are used as follows:

- The IC is mounted in the middle of the bottom layer.
- Apart from the IC-under-test, only the RF injection circuits are mounted on the bottom layer whereas all other circuits (both functional and monitoring) are mounted on the top layer.
- If SMD connectors are used, they can be mounted on the side of the circuit they are connecting to (ideal case). If through-hole connectors are used, care should be taken that they do not introduce unintentional couplings.
- The injection paths on the bottom layer are implemented as microstrips as they are easy to design and do not require lots of vias for proper functioning. Furthermore, their crosstalk behavior can be controlled easily by maintaining sufficient distance between adjacent lines.
- The lower internal layer (called Midlayer 2 in Fig. 1) serves as the ground plane for the microstrips and should be constructed as a solid ground plane.
- Preferably the higher internal layer (called Midlayer 1 in Fig. 1) should also be constructed as a solid ground plane, but it can also be used for signaling to ease routing on the top layer if necessary.
- A dense grid of ground vias should be used for (1) connecting the ground planes on the mid layers (if applicable), and (2) connecting to any ground traces on the top and bottom layers. For operation up to 2 GHz, the distance between adjacent vias should be less than 10 mm. Obviously, care should be taken that no vias interfere with components or PCB traces or come too close to them (i.e. closer than 3 mm).

IV. Specific Design Guidelines

A. RF Injection Paths

In order for the microstrip lines to have a characteristic impedance of 50 Ω on the standard board shown in Fig. 1, the width of these lines should be 0.66 mm as illustrated in Figure 2. In this calculation it was assumed that the FR4 material layer had a dielectric constant of 4.35 and a thickness of 0.36 mm whereas the copper thickness was assumed to be 35 µm.

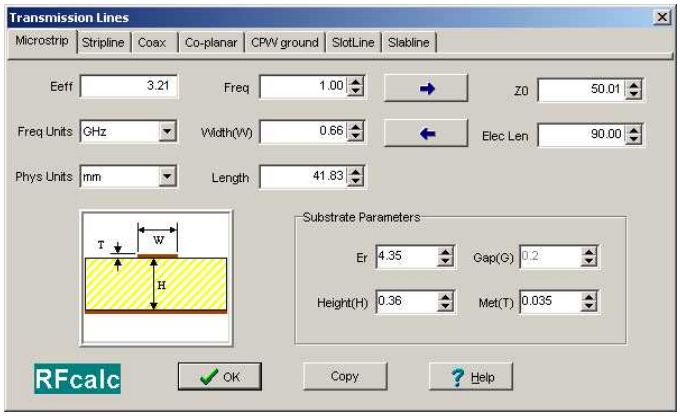

Figure 2. Cross-section of a 50-Ω microstrip line.

In order to obtain a good operation of these microstrip lines up to 2 GHz, one should route them as straight as possible and avoid sharp bends of more than 45°. One should also observe a distance of at least 3 mm to other lines, vias, connector pins or components (except in the close vicinity of the IC-under-test).

However, if the microstrip lines are well designed, there is no real need to make them as short as possible so the RF connectors can be moved towards the board edges to save space on the top layer for other circuits if necessary. In practice, it is usually advantageous to locate the RF connectors on a circle around the IC and use a star-like routing where the respective lines run radially from their RF connector to their pin-under-test as this configuration will minimise possible mutual coupling between the lines. Fig. 3 shows an example of such a radial configuration. In this board through-hole female SMA board connectors were used as RF connectors.

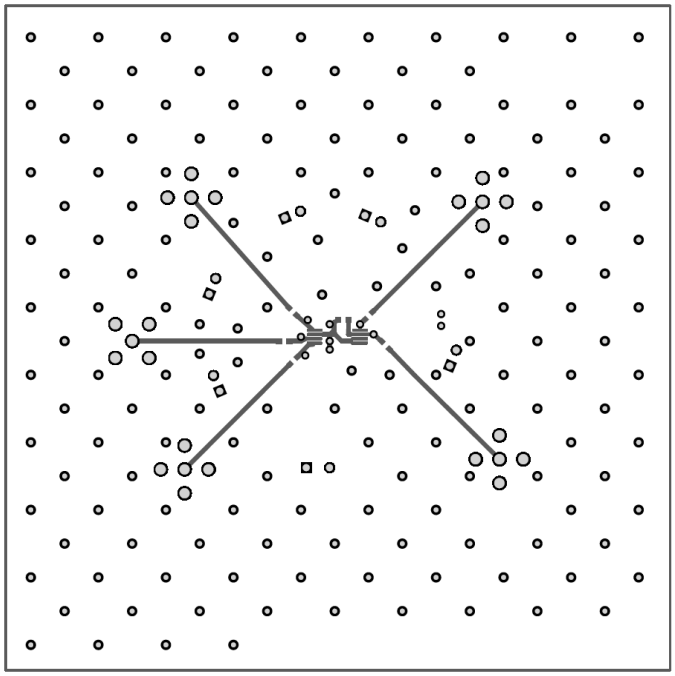

Figure 3. Bottom plane of a DPI test board.

B. RF decoupling networks

Fig. 4 shows an example of a supply filter (or other bias filter) where the impedance levels have been derived from the AN (artificial network) specified in Annex E of CISPR 25 [5]. However, to increase its frequency range to 2 GHz, a series connection of two inductors is used.

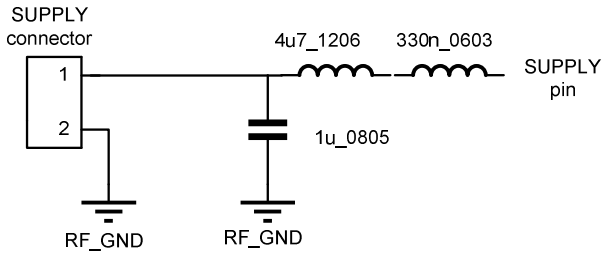

Figure 4. Example of supply filter.

For monitoring circuits or high-impedance functional connection circuits, a simple high-ohmic resistor can be used as shown in Fig.5. As mentioned before, it needs to be located very close to the pin to prevent radiation at high frequencies. If 10 kΩ is too high for functional reasons, a lower value (e.g. 470 Ω) can be used. If this is still too high, a ferrite bead can be used as it combines a low DC resistance with a high RF resistance.

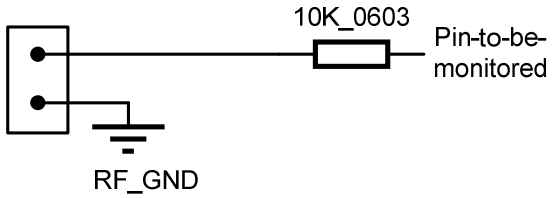

Figure 5. Example of simple decoupling circuit.

C. PCB components

When selecting the PCB components of the RF coupling and decoupling networks, sufficient attention should be paid to their operational frequency range and maximum power/current/voltage handling capability.

In order to maximize the frequency range, it is normally required to select the smallest possible sizes. However, if the maximum frequency does not exceed 2 GHz, there seems to be no need to go below the 0603 size.

Concerning the maximum voltage or power rating, it is recommended to use components than can withstand 100 V if DPI levels above 30 dBm are specified whereas 50 V should be sufficient if the DPI test level will not exceed 30 dBm.

V. BOARD VALIDATION

According to [2], the transmission loss from any RF connector to its corresponding pin should not exceed 3 dB in the test frequency range. To enable this measurement, the IC needs to be replaced by a 50-Ω coaxial port. This can be difficult to implement on existing boards that were not designed for it. In such cases it would be easier to measure the transmission loss from one RF connector to another one after having connected their associated pins-under-test together at the IC location. In this way, one would measure the combined transmission loss of two injection paths so that the equivalent criterion would double to 6 dB. We found out that we could easily meet this equivalent criterion (6 dB for two paths connected in series) for boards that were designed according to the design guidelines given in this paper.

As an example, Fig. 6 shows a number of such transmission loss measurements for the board shown in Fig. 3. These measurements were done with a well calibrated vector network analyser (Agilent E5071B) in the frequency range from 300 kHz (lower limit of the instrument) to 3 GHz (i.e. well above our design target of 2 GHz). The trace labelled “unloaded” can be considered as the reference. It includes the attenuation of the two SMA connectors, the two microstrip lines and the handmade connection between the two pins, but nothing else. It can be seen that this connection is almost perfect over the full frequency range showing that the parasitic effects of the SMA connectors and microstrip lines can be neglected. To perform

this test, special test lines were designed but it was found out that replacing the coupling capacitors by 0-Ω resistors on a existing board, produced the same results.

Next, the trace labelled "DC blocks #1" shows the effect of adding a 6.8-nF coupling capacitor (as recommended in [2]) to each of the two connected lines. It can be seen that the 6-dB criterion is met between 300 kHz and 2 GHz, but not outside this range. Hence, to meet this criterion below 300 kHz, larger capacitances than 6.8 nF have to be used whereas using smaller ones can help in meeting the criterion above 2 GHz. This is shown by the next trace labelled "DC blocks #2" where one of the two 6.8-nF capacitors has been replaced by a 100-pF one. For this combination the criterion is met from 10 MHz to over 3 GHz.

Finally, the last trace labelled "DC blocks #2 + RF blocks" shows the combined effect of the 6.8-nF and 100-pF DC blocks with one bias filter (such as shown in Fig.4 but shorted at the connector) and two monitoring circuits (such as shown in Fig. 5). This results in an additional attenuation below 3 MHz but not at higher frequencies except for a dip at 266 MHz due to a so-called anti-resonance of the two inductors in series.

A more powerful alternative to measurements such as shown in Fig. 6, would be a board validation by modelling as explained in [6]. This does not only allow to calculate the attenuation of the RF injection paths but also the mutual coupling between injection paths and other circuits.

VI. CONCLUSIONS

In this paper, design guidelines were developed that should allow the design of DPI test boards that work well up to 2 GHz. The main advantage of such an RF board optimization is that much cleaner DPI test results can be obtained that should not only correlate better with DPI simulation results of chip designers, but also with module-level EMC test results (see e.g. [4]).

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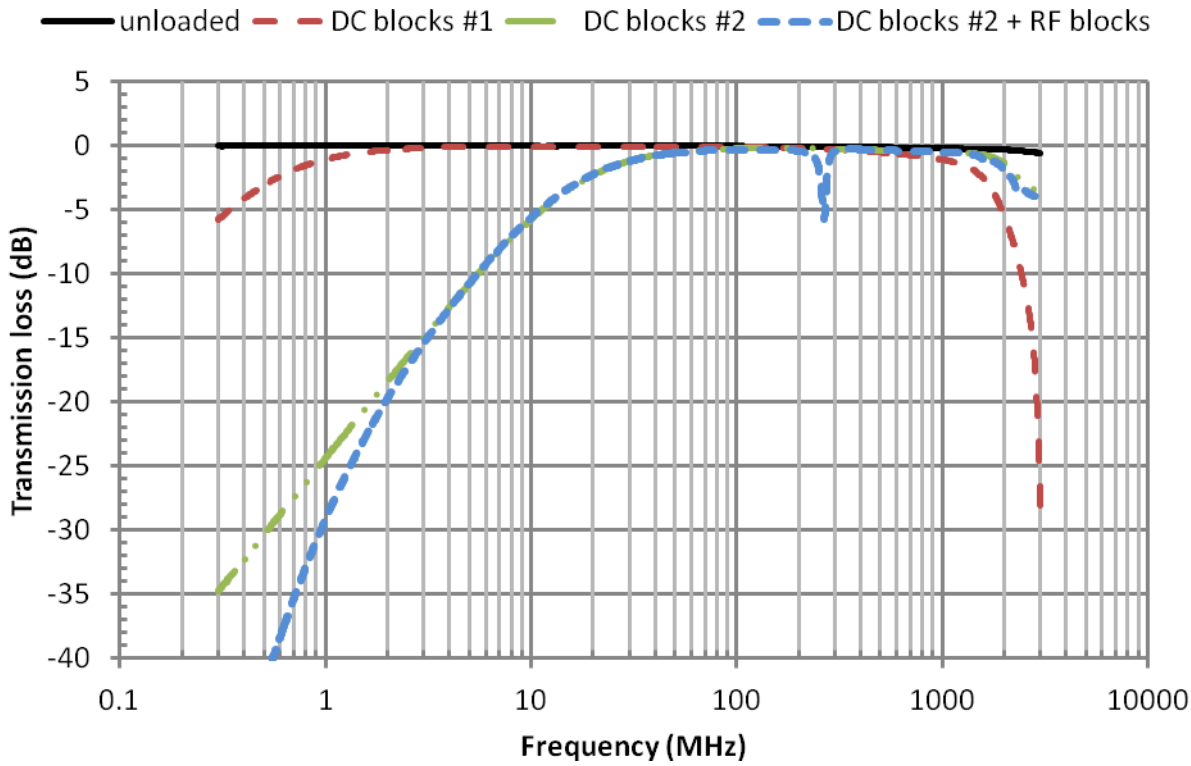

Figure 6. Measured traansmission loss of two connected RF injection paths.