Improved MW of IGZO-channel FeFET by Reading Scheme Optimization and Interfacial Engineering

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***Abstract*—We fabricated and characterized IGZO-channel back-gated FeFET. It has been found that a Memory Window (MW) reading scheme based on reverse I_d-V_g sweep can strongly attenuate the significant read disturb which affects the low-V_t state. This instability of low-V_t state origins from the asymmetric PV loop and small negative coercive voltage. With this optimized reading scheme, we proved that interfacial engineering, by inserting a NbO_x layer between La:HZO and IGZO, can significantly improve $2P_r$, MW (to 0.7V), and endurance (to 10^7 cycles). This makes the La:HZO/NbO_x/IGZO FeFET a promising structure for high-endurance and low-latency NVM.**

***Index Terms*—Ferroelectric, FeFET, IGZO, Oxide Semiconductor**

I. Introduction

HfO_2 based FeFETs have received a lot of interest since the discovery of ferroelectricity (FE) in doped HfO_2 [1], due to its CMOS compatibility and thickness scalability. 3D-structure FeFETs with memhole [2] and trench [3] structures have also been demonstrated, making the FeFET a promising candidate for high-density and non-destructive-readout NVM.

However, the endurance in Si-channel FeFET is usually limited below 10^6 cycles [4], because a low-κ and high-E_g SiO_2 interfacial layer (IL) results in significant charge trapping in FE layer and high E-field across IL, both of which will not only reduce Memory Window (MW) but also cause earlier dielectric breakdown [5]. To improve the endurance, Oxide-Semiconductor (OSC) channel FeFET is a promising solution. It has been demonstrated that by replacing Si channel with OSC materials such as IGZO [6]–[8], IZO [9], In_2O_3 [10], and InWO [11], the IL layer can be eliminated, which results in the suppression of charge trapping and improvement of endurance.

To be compatible with OSC channel, low-thermal-budget FE layer will be needed. The most promising one is $Hf_{1-x}Zr_xO$ (HZO), which can lower the process temperature to below 500°C [12]. Besides, it has been reported that the endurance of HZO MFM (Metal/Ferroelectric/Metal) capacitor can be improved to 10^{11} cycles by La doping [13], which can suppress the leakage current and decrease coercive field, so that the operation field can be pushed away from the breakdown electric field. However, the La doping also results in more oxygen vacancies as charged defects, prevents crystallization, and therefore offers very low $2P_r$ and pinched polarization-voltage (P-V) loop. This could be addressed by introducing NbO_x interfacial layer, which injects oxygen into HZO, facilitates the transition from anti-FE phase to FE phase, and significantly improves the FE response [14].

In this work, IGZO-channel FeFETs with La:HZO as FE layer were fabricated as the control sample, and a novel stack with interfacial engineering of NbO_x interfacial layer has been presented. PUND measurement was done to investigate the FE switching characteristic of pure La:HZO and La:HZO/NbO_x stacks. Asymmetric P-V loop was found to result in significant disturb during the FeFET V_t detection, and an optimized MW reading scheme was then proposed. Finally, endurance measurement of MW with this optimized reading scheme was done to study the impact of NbO_x interfacial engineering.

II. Device Fabrication

The fabrication flow of back-gated (BG) IGZO-channel FeFETs is shown in Fig. 1. The process started from a p++ Si substrate, on which 10-nm TiN was deposited by PVD as Bottom Electrode (BE). Ferroelectric layer of 10-nm-thick La:HZO was then deposited by ALD. After that, two different samples were prepared:

- La:HZO/NbO_x/IGZO stack: a 2-nm NbO_x capping layer was deposited on top of ferroelectric layer before IGZO.
- La:HZO/IGZO stack: No NbO_x capping layer.

Then, 5-nm IGZO channel was deposited, followed by annealing in 10% O_2 ambient for 1h at 350°C. Afterwards, 180-nm SiO_2 was deposited and active area was patterned. Finally, isolation oxide deposition, S/D patterning and PVD-TiN/W deposition was done to form the contact.

III. Results and Discussion

A. PUND measurements

PUND measurement was done to confirm the ferroelectricity in both the La:HZO/IGZO and La:HZO/NbO_x/IGZO stacks, by connecting S/D electrode of FeFET together as the top electrode. Triangular pulses with 25μs rise and fall time were applied to the back gate, and the current was measured from the top electrode. Fig. 2 shows the PUND P-V loop and the corresponding switching current (I_{SW}) of IGZO-channel FeFETs with and without NbO_x. In Fig. 2(a)(c), if there is no NbO_x capping layer, the ferroelectricity is weak, with a small remnant polarization ($2P_r$) of about 4μC/cm^2.

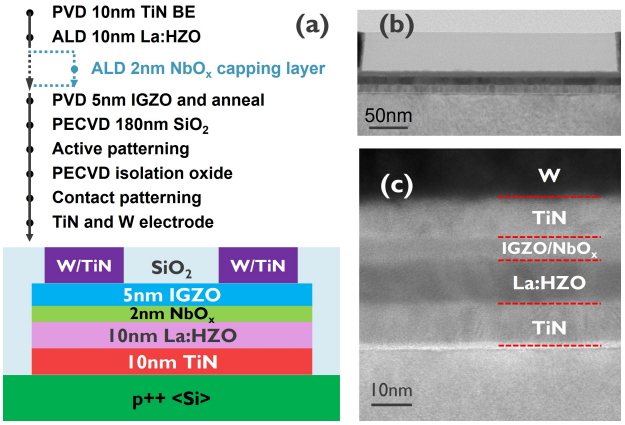

Fig. 1. (a):Device structure and fabrication flow of BG IGZO-channel FeFETs; (b)(c):Cross-section TEM images in the channel and Source/Drain.

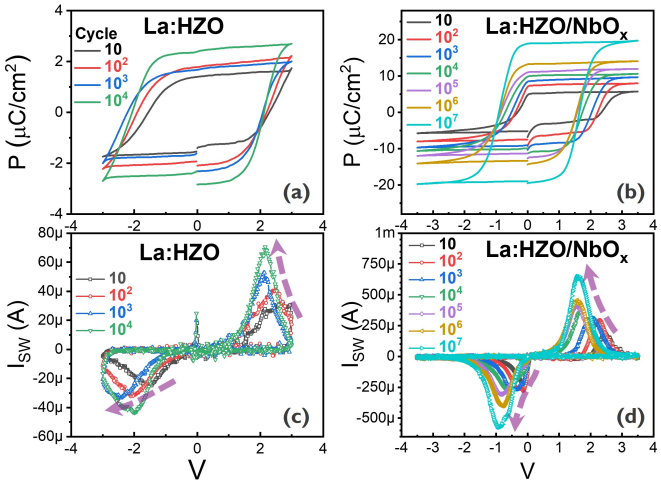

Fig. 2. PUND P-V loop and the corresponding I_{SW} of IGZO-channel FeFETs without NbO_x (a,c) and with NbO_x (b,d). Higher ferroelectric polarization is obtained by inserting NbO_x interfacial layer, which is a V_O sink to HZO and increases the amount of Orthorhombic phase [14].

Once a capping layer of 2-nm NbO_x is introduced in the gate stack, as is shown in Fig. 2(b)(d), the ferroelectricity will improve, with a much larger $2P_r$ of about $40\mu C/cm^2$ after full wake up, and no fatigue is seen up to 10^7 cycles. The possible reason is that NbO_x capping layer on top of HZO acts as an Oxygen Vacancy (V_O) sink to HZO. The removal of V_O facilitates the Tetragonal phase to Orthorhombic phase transformation, and thus improves the ferroelectricity [14].

For both the stacks of La:HZO and La:HZO/NbO_x, it could be noticed from Fig. 2(c)(d) that the positive and negative switching peaks are quite asymmetric before wake up, especially for the La:HZO/NbO_x/IGZO FeFET, which has a quite small negative coercive voltage (V_c^-) near 0V, and a much larger positive V_c^+ of 2.5V. After the bipolar cycling is applied, not only could the increase of I_{SW} peaks be observed, but also both the V_c^- and V_c^+ move toward the left, resulting in more symmetric P-V and I-V loops. This asymmetric coercive field could originate from built-in electric field in the gate stack of IGZO FeFET, and it will play an important role in the memory operation of IGZO-channel FeFET, resulting in significant read disturb, which is to be discussed in the next section.

B. Optimization of MW reading scheme

In this experiment, two different reading methods of single-pulse MW, which is defined as the ΔV_t between programmed (by positive pulse) and erased (by negative pulse) state, were compared, after the devices were woken up:

- Forward-sweep reading (Fig. 3(a)): forward I_d-V_g sweeps from -1V to +1V was taken at initial state, after program by $+3V/10\mu s$, and after erase by $-3V/10\mu s$.
- Reverse-sweep reading (Fig. 3(b)): Instead of forward sweep, reverse DC sweep from +1V to -1V was applied.

As is shown in Fig. 3(a), if a commonly used forward sweep after program/erase is conducted to measure the single-pulse MW, no V_t difference after program/erase can be seen. However, if a reverse sweep is used to measure the single-pulse MW, we observe an evident V_t difference after program/erase, shown in Fig. 3(b). Besides, if we compare the forward sweep

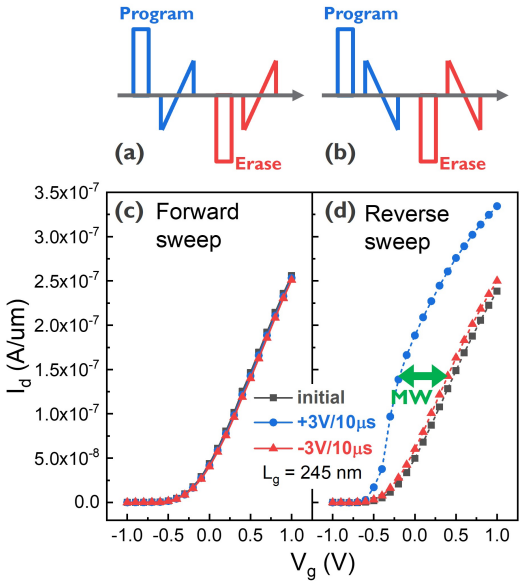

Fig. 3. I_d-V_g curves of initial state, and after program/erase pulses, read by forward (a) or reverse (b) sweep. Single-pulse MW could be measured by reverse sweep.

and reverse sweep I_d-V_g curves, the forward-sweep V_t after both program and erase are fixed at the same value as the reverse-sweep high-V_t (after $-3V/10\mu s$). This indicates that in the IGZO FeFETs, the low-V_t state (after programming by positive pulses) is quite unstable, and might be disturbed by the negative read voltage.

To further confirm the impact of DC voltage on the MW reading, another experiment using double-read process was taken. As is shown in Fig. 4, after the device was fully woken up, a positive pulse of $+3V/10\mu s$ was applied to the BG to program the FeFET into low-V_t state. A reverse sweep from +1V to different negative values was then used to

read the programmed I_d-V_g curve. Three sweep ranges with different stop voltage were selected: from +1.0V to -0.2V (Fig. 4(a)); from +1.0V to -0.5V (Fig. 4(b)); from +1.0V to -1.0V (Fig. 4(c)). After this 1st reading process of programmed state, a 2nd I_d-V_g reading was then conducted to confirm whether this low-V_t state had been disturbed during the 1st reading process or not. If the I_d-V_g curve measured by the 1st and 2nd read coincides with one another, it means there is no disturb induced by the stop voltage. Note that the 2nd I_d-V_g reading is always a forward I_d-V_g sweep starting from 0V, to make sure there is no additional disturb during the 2nd reading. Finally, an I_d-V_g sweep was measured after $-3V/10\mu s$, which establishes the erased high-V_t.

If the 1st reading voltage stops at -0.2V (Fig. 4(a)), there would be a slight difference between the 1st (in green) and 2nd (in red) I_d-V_g curve, which indicates that disturb already happens if the lower limit of sweep range is below 0V, however a large MW can still be measured. If the 1st reading voltage stops at -0.5V or -1V (Fig. 4(b)), the 2nd-read I_d-V_g has already been shifted towards the right, and the V_t, which should be a low value, is more and more close to the high-V_t state. These results imply that the reading disturb in IGZO FeFET will become more and more severe if a more negative DC bias is used during the V_t extraction.

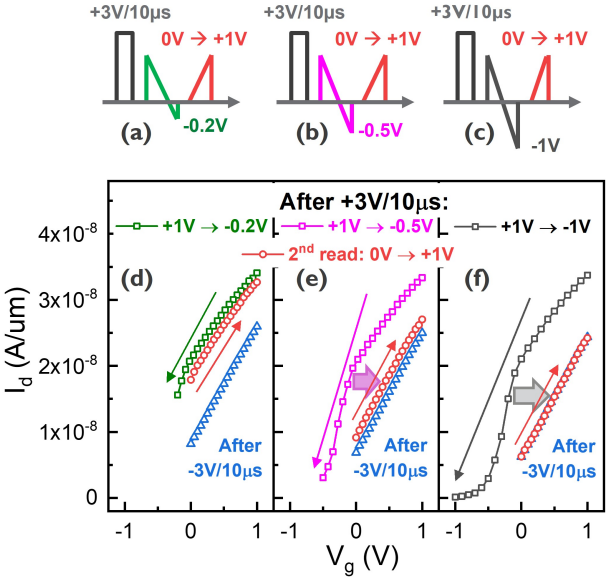

Fig. 4. Schematics and I_d-V_g curves with a 1st reverse read, starting from +1V to different stop voltages, and followed by a forward read from 0V to +1V. The 1st reading I_d-V_g stops at: (a,d). -0.2V; (b,e). -0.5V; (c,f). -1V. More negative V_g value will result in more disturb to low-V_t state.

Finally, fast measurement of read disturb by $\pm 1V/1\mu s$ pulses was also done to check disturb caused by $\pm 1V$ read voltage. After the device was fully woken up, a program operation of $+4V/1\mu s$ (Fig. 5(a)) or an erase operation of $-4V/1\mu s$ (Fig. 5(b)) was done to set the device into high-current or low-current state. To prevent the possible disturb of I_d-V_g read, fast-IV measurement was implemented. A pulse of 0.2V pulse amplitude and $10\mu s$ pulse width was applied to the gate, and drain current was measured. Afterwards, disturb pulses featuring $-1V/1\mu s$ (for programmed state) or $+1V/1\mu s$ (for erased state) were applied respectively to the gate for maximum 10^6 times, also followed by fast-IV measurement at V_g=0.2V to record the I_d after read disturb.

The result of read disturb measurement is shown in Fig. 5 (c) and (d). If the device is in programmed (high-current) state initially (Fig. 5 (c)), even a low number of $-1V/1\mu s$ pulses will immediately disturb the high-current, and this current value shows a gradual decrease with disturb cycles. Finally, the high-current, as well as the MW, disappears after 100 pulses. Whereas for the erased state, or low-current state (Fig. 5 (d)), the lower value of I_d is hardly disturbed by $+1V/1\mu s$ pulses. This result also confirms that, compared with erased high-V_t state, the programmed low-V_t state will be readily disturbed by a negative bias, as small as -1V.

The stronger disturb in low-V_t state as compared to high-V_t state could be well explained by the PUND measurements in Fig. 2. For both the La:HZO and La:HZO/NbO_x stack, the positive and negative switching peaks are not symmetric, with a much larger V_c^+ than $|V_c^-|$. Although the positive and negative switching peaks are moving toward the left and becoming more symmetric with cycling, the final $|V_c^-|$ is still smaller than V_c^+, especially for the case of La:HZO/NbO_x stack with a small $|V_c^-|$ less than 1V. Because of this small $|V_c^-|$, a small negative bias could readily flip the programmed low-V_t state.

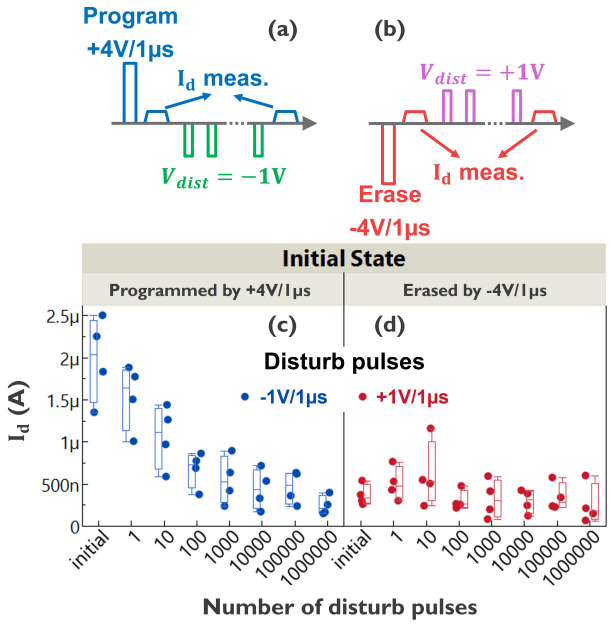

Fig. 5. (a),(c): Schematics and results of disturb induced by $-1V/1\mu s$ pulses on programmed state; (b),(d): Schematics and results of disturb induced by $+1V/1\mu s$ pulses on erased state.

C. *Effect of NbO_x interfacial layer on MW and endurance*

Through the optimization of MW reading scheme, we know that a rather small negative voltage would overwrite the

programmed low-V_t state. That is the reason why a reverse I_d-V_g sweep is used to prevent the read disturb and read the MW correctly. During the endurance measurement, the P/E-read pulse scheme is as shown in Fig. 3 (b), by using $\pm$4V/1μs pulses to program/erase the cell, followed by a reverse I_d-V_g sweep to read the low-V_t or high-V_t.

The I_d-V_g characteristic and MW during cycling are shown in Fig. 6. For the IGZO-channel FeFET with only La:HZO ferroelectric layer, we see no MW and poor endurance of 10^4 cycles, after which the devices break down. Besides, the MW, which is defined as $V_{t,erased} - V_{t,programmed}$, becomes negative after 10 cycles, implying that charge trapping dominates over ferroelectric dipole switching.

In the case of La:HZO/NbO_x stack, although there is still a very small MW at the initial state, the MW enlarges with cycling, showing a very strong wake-up and, afterwards, quite high MW of about 0.7V. Moreover, with the introduction of NbO_x layer, the endurance is also much higher than the pure La:HZO ferroelectric layer, which also implies that the high-κ and low-E_g ($\sim$4.0 eV [15] as compared to 5.25 eV of La:HZO) NbO_x interfacial layer will not result in extra charge trapping and will not degrade the endurance. However, except for the advantages of boosting $2P_r$, MW and endurance, the NbO_x layer also introduces a shift of V_t towards more negative values, as is shown in Fig. 6(c). As a result, although the ferroelectricity doesn't show fatigue in Fig. 2(b,d), the MW is however decreasing after 10^6 cycles because of this high-V_t rolling off. This negative V_t shift might originate from positive ion trapping [16], and is becoming more and more significant with larger number of cycles.

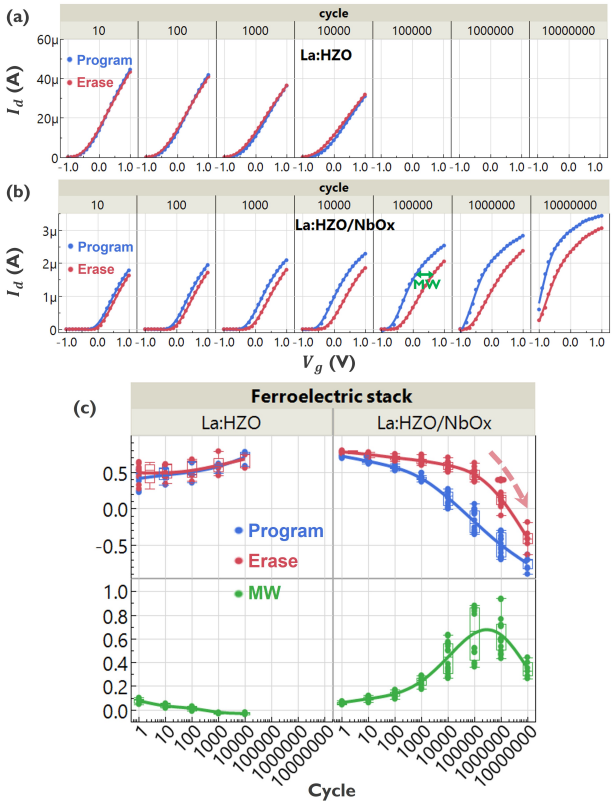

Fig. 6. (a,b).I_d-V_g; (c).V_t and MW after P/E of IGZO FeFET, on devices with 245-nm L_g, with La:HZO and La:HZO/NbO_x ferroelectric stack. FeFETs without NbO_x break down after 10000 cycles.

IV. Conclusions

In this work, we fabricated and characterized two structures of IGZO-channel FeFETs with and without NbO_x capping layer. It was found that the positive and negative ferroelectric switching peaks are quite asymmetric, with a very small negative coercive voltage, which results in a quite unstable low-V_t state. Further experiments including double-read and fast read disturb measurement were also done, confirming that this unstable low-V_t state will be easily disturbed by negative bias as small as -1V after tens of 1μs pulses. So, it's important to select the correct MW reading scheme, i.e. the reverse I_d-V_g sweep starting from positive V_g to prevent the read disturb.

With this optimized MW reading scheme, it was found that interfacial engineering in La:HZO and IGZO stacks is critical to boost ferroelectric response. By introducing a NbO_x interfacial layer, which plays an important role as oxygen vacancy sink and improves the ferroelectricity, large-$2P_r$, fatigue-free, and high-endurance could be achieved in La:HZO/NbO_x/IGZO capacitors. With this significantly improved ferroelectricity, we have successfully demonstrated IGZO-channel FeFET with high MW of 0.7V and endurance up to 10^7 cycles. However, the P-V loop shows strong asymmetry before fully woken up, and V_t of La:HZO/NbO_x/IGZO FeFET is unstable and shows strong V_t roll-off with cycling. Thus, more investigations of the wake-up behavior and V_t instability are needed in the future.

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