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A 90nm CMOS 5-bit 2GS/s DAC for UWB Transceivers

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***Abstract*— A 5-bit 2GS/s current-steering D/A converter for ultra-wideband (UWB) transceivers is presented in this paper. It is based on a full-binary weighted architecture and achieves better than 10-bit static linearity without calibration. The DAC occupies $0.5mm \times 0.75mm$ in a standard 90nm CMOS technology. A spurious-free dynamic range (SFDR) of more than 30dB has been measured over the complete Nyquist interval at sampling frequencies of 2GS/s. The power consumption at a 2GHz clock frequency for a near-Nyquist sinusoidal output signal equals only 12mW. For UWB signals, which have about 500MHz bandwidth, the DAC consumes even less than 8mW.**

I. Introduction

Ultra-wideband (UWB) is a technology which is specially suitable for short duration and very wide bandwidth data communication with low power dissipation. An efficient use of radio bandwidth is intended to provided by the Federal Communications Commission (FCC). It is expected to enable both high data rate communication systems, such as wireless USB, and long life, low data rate wireless personal area network (LR-WPAN) as well as sensoring and imaging systems.

Multiband orthogonal frequency-division multiplexing (MB-OFDM) is one of the most popular approaches in high speed UWB applications. A bandwidth of 528MHz is utilized in this method, which results in requiring a minimum 1.056GS/s Digital-to-analog converter (DAC). IEEE 802.15.4a standard for LR-WPAN specified the UWB PHY operating both in the sub-gigahertz(250-750MHz) band and the gigahertz band: the low band (3.1-5GHz) and the high band (6-10.6GHz). A DAC operating at a minimum of 1.5GS/s without a mixer is required in the UMB sub-gigahertz band. To relax the requirements of the followed filter, a 2GS/s DAC is designed instead of 1.5GS/s in this work. The high speed DAC can also fit in other channels on the gigahertz band of the UWB with the help of extra mixers.

The systems based on UWB standards demand only moderate signal-to-noise ratios. This implies that the data converters used in these systems have to operate at increasing sampling rates, but require less precision. This paper presents a 5-bit current-steering Digital-to-Analog Converter (DAC) that fulfills the requirements of such next generation UWB communication systems. The designed DAC was manufactured in a pure-digital 90nm technology and consumes only 12mW for Nyquist signal at its nominal 2GS/s update rate.

The basic architecture, topology and floorplan are discussed in section II. Section III describes the different building blocks of the DAC and explains their design in detail. Section IV presents and evaluates the measurement results of the prototype. Finally, a conclusion is formulated.

II. Architecture

Current steering structure is a common choice for very high speed DACs.The sole of such converter is an array of current sources, which are switched on/off dependent on the input signal. The accuracy of the converter is determined by the matching behavior of the transistors of current sources [1]. The usage of transistors as the unity matching element makes the current-steering DACs highly compatible with standard CMOS process technology. There are three major architectures that are used to implement current steering DACs: binary, unary and segmented.

Since the DAC design for UWB systems targets moderate resolution and high speed at very low power, the full-binary implementation apparently is the most suitable choice. But this topology requires very tight timing control to reduce the nonlinearity induced by switching effects. The pseudo-unary principle introduced in [2] provides a mechanism to gain better control over the switching behavior. The pseudo-unary idea combines the advantages of the unary/segmented topology (high performances) with the advantages of the binary design (fast speed). Each binary bit has a group of unary current sources, which is corresponding to the bit weight, with their own drivers. This eliminates the power consuming decoder and avoids extra matching errors. It gains the low power and high speed properties of the binary weighted architecture while remaining able to achieve the high SFDR performance of the unary/segmented architecture.

The floorplan of the design is shown in Fig. 1. Five parts can be distinguished: the LVDS inputs, the pseudo-decoder, the switch drivers, the cascode and switches and the current source array. The 5 bits input signals and two clocks (the analog clock and the digital clock) are first received by a reduced specification Low Voltage Differential Signaling (LVDS) input stage. Then the pseudo-decoder rearranges and routes the binary inputs to the pseudo-unary signals. It also synchronizes the pseudo-unary signals with the help of the digital clock. Afterwords, the signals pass through the switch drivers and finally reaches the analog core of the converter. The output is routed in a tree structure and passes though the current source array.

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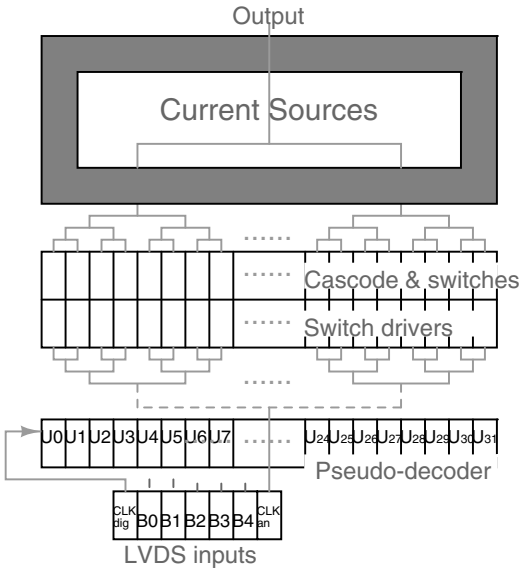

Fig. 1. Floorplan of the pseudo-unary DAC.

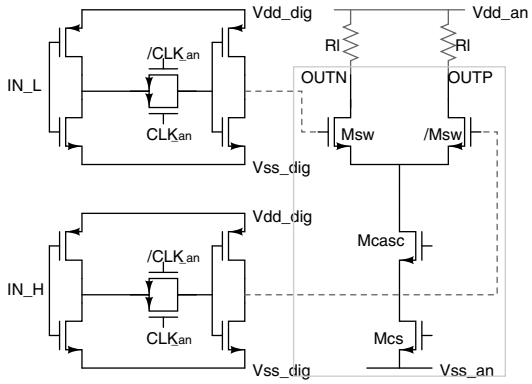

Fig. 2. Switch drivers and switched current cell.

III. DAC Building Blocks

The different building blocks of the designed DAC can be classified into three catalogs: the input stage, the digital part and the analog part.

A. Input Stage

Since the DAC is required to work at 2GS/s, reduced specification LVDS receivers basing on [3] are introduced in the input stage. The receivers can ensure the Nyquist-rate measurement of the DAC. On-chip resistor termination is used to reduce the resonant behavior of the bonding wire and on-chip parasitic capacitance. In order to save the power in digital part, the LVDS receiver converts the differential inputs into single-ended. As a result, only single-ended signals are processed in the digital part. They will be converted back to complementary signals again right before the analog core.

B. Digital Part

The digital part of the DAC is mainly a pseudo-decoder. It consists of a routing matrix and a array of digital registers. The routing matrix is used to connect the binary input signals to their corresponding unary registers. The traditional thermometer code decoder is replaced by this simple but carefully designed routing. The array of registers which is added after the routing matrix can synchronize the rearranged signals. In such way, good performances can be obtained while being able to enable the high speed ability. A separate supply voltage has been utilized in the digital part from the analog part. A lower than 1 volt voltage supply is enough for the digital part to work properly. As a result, the goal of low power consumption is achieved.

C. Analog Part

The analog core consists of the current sources, cascodes, switches and their drivers. The first three elements are designed together as one entity (switched current cell). It is shown in the gray box of Fig. 2. Since the matching behavior of the current sources determines the static accuracy of the DAC, the current source array need to be in the cleanest environment. Therefore, in layout one extra guard ring is added to ensure the smallest distortions from the other parts.

The switch driver, which is the left part of Fig. 2, is used to re-synchronize the digital control signals that drive the switches. Since very small timing differences between the control signals result in large nonlinearities in the output spectrum [4], the re-synchronization of the signals is very necessary.

1) Switched Current Cell: The static accuracy of a converter is set by the matching properties of the transistors used in the current source array. It provides an upper limit on the linearity of the converter for input signals with different frequencies. Based on the equations in [5], the minimum size of a LSB current source is calculated with a requirement of 10-bit static linearity. To make sure the design is robust with respect to inaccuracies in the foundry-supplied matching data and deep-sub-micron mismatch modeling issues, a safety margin has been used.

Large area of the current sources can only reduce the random errors in the DAC caused by the random variations inherently present in the CMOS manufacturing process. It can't cancel the systematic errors coming from gradients in physical parameters either due to edge effects or due to wafer level gradients. Gradient-induced mismatch errors are compensated by using a double common-centroid switching scheme in this design, as shown in Fig. 3. The current source of the unary cell is divided into 4 current sources each delivering 1/4 the least significant bit (LSB) current. In every quadrant, a current source is placed around a center of the area (A/B/C/D) based on a centroid scheme [6]. Four dummy rows and columns have been added to avoid edge effects, as shown in the grey area of the Fig. 3.

Because of the large area of the current source array as a result of static specifications, the parasitic capacitance at the drain of the current source transistor is significant. If we use the current source transistor alone, the linearity of the

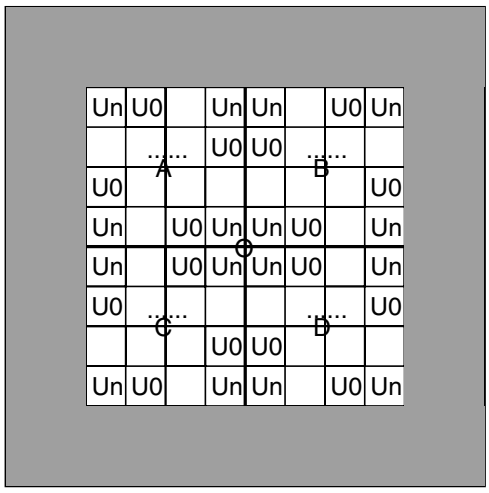

Fig. 3. The switching scheme of the current source array.

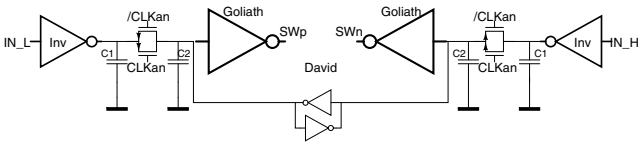

Fig. 4. Simplified schematic of the basic buffer-latch structure.

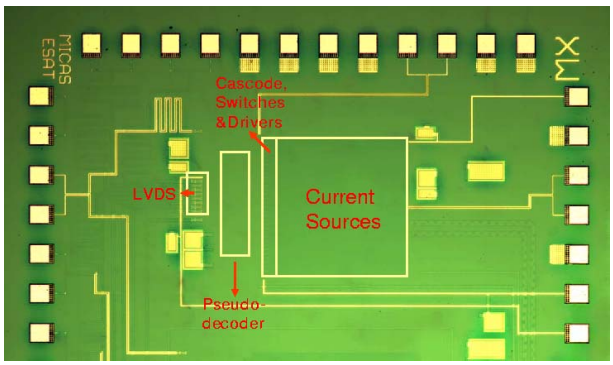

Fig. 5. Chip microphotograph.

converter will be degraded quickly with the output frequency increasing. In order to obtain enough output impedance over the entire Nyquist band, a cascoded current source structure has been chosen, as shown in Fig. 2. This cascoded current source, in combination with the switch transistor that also acts as a cascode, provides the required output impedance Z_{imp} of $6.4M\Omega$ for 10-bit INL and $6.25k\Omega$ for 5-bit SFDR up till the Nyquist frequency.

In order to meet the low power requirement and 1V supply voltage for 90nm CMOS technology, the total output current was chosen to be 5mA, and the load impedance Z_{Load} is 25Ω. This results in a single ended output swing of 125mV. A higher output swings will cause the switches to operate in their linear region for part of the signal, resulting in large signal dependent changes in output impedance, hence distortion. Full-swing control signals are used to ensure the switches always operating in saturation and being able to work on high speed.

2) Switch Drivers: The transition time of the signals that control the switches is dependent on the output voltage. It will also limit the maximum possible clock frequency of the DAC. Therefore the transition time is minimized by using the buffer-latch-switch structure shown in the left part of Fig. 2. It is based upon the structure proposed in [2]. It is used to re-synchronize the signals that control the switches. The David-Goliath inverters and input buffers compose the most important part of the driver. The simplified schematic is shown in Fig. 4. Special care has been taken on the size of the input inverter due to the capacitive division between C1 and C2. To increase switching speed of the original design, a transmission gate replaces the single NMOS pass-transistor. The usage of a transmission gate also improves the switching symmetry and the low-voltage compatibility.

IV. Measurement Results

Fig. 5 shows the photograph of the realized chip. The area of the core circuit is $0.75mm \times 0.5mm$. All measurements are performed on a single-ended output. The full scale load current of the DAC is 5mA. The measured results of INL and DNL are shown in Fig. 6. Since they are smaller than $0.012LSB_{5bit}$, the realized DAC reaches the 10-bit static accuracy.

The dynamic performance of the converter has been measured with different signal frequencies at the speed of 2GS/s. The measurements indicate that the 5-bit performance is sustained up to the Nyquist frequency, still showing a SFDR value larger than 30dB. The output spectrum for a 0.98GHz sinusoidal signal at 2GS/s clock is presented in Fig. 7, showing the near-Nyquist 5-bit performance. Fig. 8 summarizes the measured SFDR as a function of input signal frequency for a fixed update rate of 2GS/s. A two-tone test provides more information about the capability of the DAC to output real UWB modulated signals. The output spectrum for the two-tone test is shown in Fig. 9. The frequencies of the two tones are $500MHz$ and $509MHz$ and the sampling rate is 2GS/s. A better than 37dB IM3 can be seen in the figure.

TABLE I
Comparison With Another DAC Published in ICUWB

	This work	[8]
Sample rate	**2GS/s**	1.35GS/s
Resolution	5 bit	5 bit
INL	**0.008**	0.04
DNL	**0.011**	0.05
SFDR with Power consumption	33dB 12mW (980MHz@2GS/s) **35dB 7.9mW** (666MHz@2GS/s) **37dB 7.7mW** (2tones 500MHz@2GS/s)	30.3dB 10.4mW (740MHz@1.5GS/s) 30.7dB 9.7mW (666MHz@1.35GS/s)
FOM	**2.61GHz/mW**	2.27GHz/mW
Technology	90nm CMOS	180nm CMOS

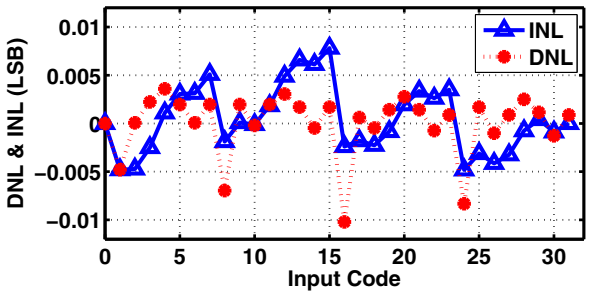

Fig. 6. INL and DNL profiles.

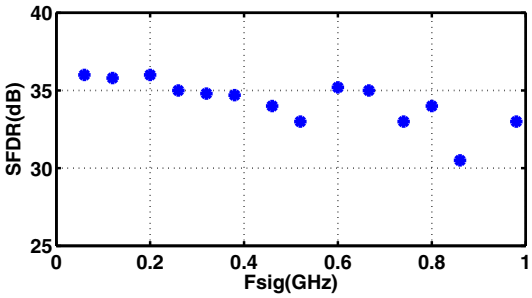

Fig. 8. Measured SFDR as function of signal frequency at 2GS/s.

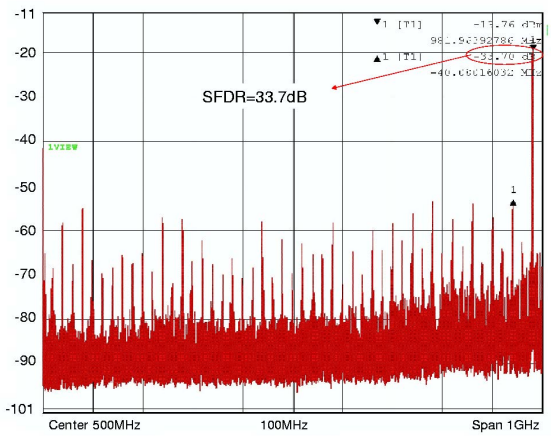

Fig. 7. Measured output spectrum for a 980MHz output signal at 2GS/s.

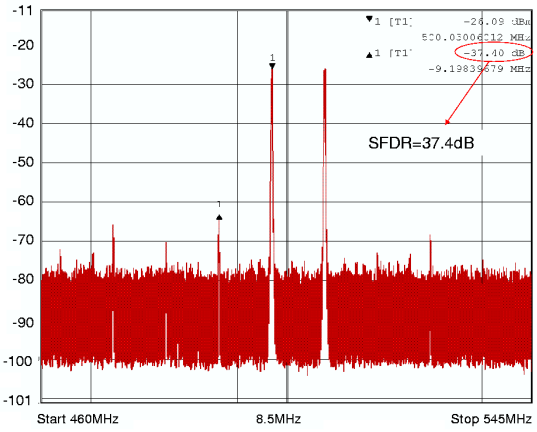

Fig. 9. Measured output spectrum for a two-tone signal at $F_1 = 500MHz$ and $F_2 = 509MHz$ at 2GS/s.

Table I compares a recently published D/A converter [8] in ICUWB with the converter presented in this work. In [8], a 5-bit DACs operating at around 1.35GS/s is presented. The definition of Figure of Merit (FOM) in equation 1 introduced in [7] is used to evaluate the performance of such large-bandwidth D/A converters. The comparison table indicates that this DAC has the ability to process signals with higher bandwidth. And for the specified UWB output signal it consumes 1/5 less power, which is also confirmed by the values of FOM. Since the MB-OFDM approach has a bandwidth of 528MHz, the two tone test provides the evidence of the ability of the DAC to output real UWB modulated signals. The DAC consumes only 7.7mW for the two tone signals centered at about 500MHz.

$$FOM = \frac{2^N \cdot f_{sig}@SFDR = 6(N-1)}{POWER} \quad (1)$$

V. Conclusion

A 5-bit current steering DAC for UWB transceivers is presented in this work. It achieves 30dB SFDR performance over the entire Nyquist range at 2GS/s with very low power consumption. Therefore, it fulfills the performance requirements for UWB transceivers. It consumes only 12mW at the 2GS/s speed with a near 1GHz output signal and less than 8mW for the signals with less than 600MHz bandwidth. The DAC exhibits a 10-bit intrinsic linearity. The full scale output current of the DAC is 5mA. The converter is implemented in a standard 90nm CMOS technology and has a core area of 0.375mm^2.

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