A High-Efficiency, High-Frequency Boost Converter using Enhancement Mode GaN DHFETs on Silicon

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***Abstract*—A boost converter was constructed using a high voltage enhancement mode (E-mode) AlGaN/GaN/AlGaN DHFET transistor grown on Si<111>. The very low dynamic on-resistance ($R_{dyn} \approx 0.23\ \Omega$) and very low gate-charges (e.g. $Q_{gate} \approx 15$ nC at $V_{DS} = 200$ V) result in minor transistor losses. Together with a proper design of the passive components and the use of SiC diodes, very high overall efficiencies are reached. Measurements show high conversion efficiencies of 96.1% ($P_{out} = 106$ W, 76 to 142 V at 512.5 kHz) and 93.9% ($P_{out} = 97.5$ W, 78 to 142 V at 845.2 kHz). These are, to our knowledge, the highest efficiencies reported for an enhancement mode GaN DHFET on Si in this frequency range. The transistor switching losses are concentrated in the turn-on interval, and dominate at high frequencies. This is due to a limited positive gate-voltage swing, as the gate-source diode restricts the positive drive voltage.**

***Index Terms*—boost converter, enhancement mode (E-mode), GaN DHFET, high efficiency, very high frequency, wide bandgap**

I. Introduction

GaN-based heterojunction field effect transistors (HFETs) are becoming of major interest as their outstanding properties make them a good replacement candidate for the currently used silicon devices in power electronic converters [1]. Their high electron mobility (1000-2000 cm^2/Vs), high breakdown voltage (3 MV/cm) and high power density make a further optimization of the energy conversion possible, resulting in an increase of efficiency and switching frequency compared to today's Si-based converters [2] - [3]. Moreover, these materials can be grown onto large diameter Si substrates, which is a major cost advantage, especially comparing to other wide-bandgap materials such as SiC. The performance of GaN-on-sapphire and GaN-on-SiC has already been demonstrated by 1 MHz, 120 and 300 W converters [2] - [3]. Nowadays more attention goes to enhancement mode (E-mode) GaN transistors due to the inherent safety [4] - [5]. In this paper, we show the performance of E-mode AlGaN/GaN/AlGaN double-heterostructure FETs (DHFETs) [5], using a dedicated high-frequency boost-converter set-up. A hard switching boost topology is a good tool to demonstrate the advantages of GaN-based transistors in a power electronic converter as it is often used for power-factor-correction (PFC) front ends and as the basic building block of half bridges. As in today's SMPS design the trend is to move toward a more compact circuit design, the switching frequencies of interest approach the MHz range. First, the converter construction is discussed, including the design of the main power circuit, the gate drive circuit and the inductor. State-of-the art SiC diodes and an in-house developed planar inductor contribute to a more compact design and a highest possible efficiency. In a next section, the used GaN-based power transistors, being driven by dedicated drive circuitry are highlighted, including the device fabrication and device characterization. Finally, the overall converter performance is discussed. Attention goes to the results of several efficiency measurements, to the distribution of the converter losses as also to a possibility to improve the device and converter performance.

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II. Converter construction

The design target was to construct a high-efficiency, high-frequency, hard switching boost converter wherein GaN-based DHFETs are used as switching devices. The frequency range of interest covers the 300 kHz to 1 MHz interval. The maximum convertible power mainly depends on the maximum allowed output voltage, being limited by the breakdown voltage of the used GaN switch to approximately $V_{BD} = 200$ V in this case. As a consequence, the results presented in this paper were obtained in a power range of 60 to 150 W output power. The main parts in the converter design are discussed in the next subsections. Special attention was paid to the design of the passive components and compactness of the converter, reducing the parasitic effects to a minimum and aiming for the highest possible efficiency.

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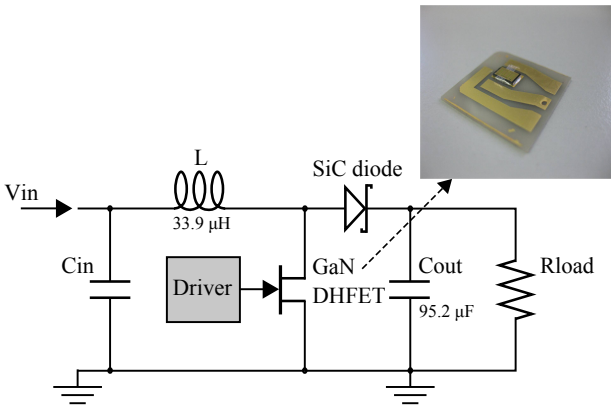

Fig. 1. Boost converter circuit with flexible high-frequency gate drive circuit (up to 2 MHz) to test the E-mode GaN DHFETs. (upper inset) GaN E-mode DHFET mounted on an AlN carrier substrate.

A. Main power circuit

Fig. 1 shows a diagram of the circuit under study. The main power circuit consists of an AlGaN/GaN/AlGaN E-mode DHFET power switch, a silicon carbide (SiC) rectifying diode, an inductor (L), two filtration capacitors (C_{in} and C_{out}) and a load (R_{load}). During the on-interval of the GaN switch, energy from the input line is stored in the inductor. As, for generality, only a duty cycle of around 50 % is considered, this energy is then released to the load at twice the input voltage during the off-interval of the switch. The power circuit was built on a two-layer printed circuit board, being optimized for high-frequency switching (up to 1 MHz). Special attention was paid to the compactness of the converter, reducing parasitic effects. The rectifying diode is a 600 V, zero recovery current SiC Schottky diode, providing superior switching characteristics which will lead to an increased efficiency, a reduced size and a higher possible switching frequency. The 4-A-rated C3D04060 diode from Cree Inc. showed the lowest sum of conduction and charging losses.

B. Gate drive circuit

The main requirement of the gate driver was the ability to deliver a gate-drive signal having a voltage range suitable to drive the E-mode GaN DHFET, at a frequency up to 1 MHz. In addition the fall and rise times of the gate signal had to be small in order to reach fast on and off switching. For meeting these requirements dedicated gate drive circuitry was developed [6]. A fully controllable gate-voltage range (V_{GS}) was obtained at a switching frequency up to 6 MHz:

$$\begin{array}{lcl} V_{GS,on} & = & V_{range} - V_{off} \\ V_{GS,off} & = & 0 - V_{off} \end{array} \quad (1)$$

with

$V_{GS,on}$	upper level of the gate-voltage range (V)
$V_{GS,off}$	lower level of the gate-voltage range (V)
V_{range}	gate-voltage range ($= V_{GS,on} - V_{GS,off}$) (V)
V_{off}	offset voltage, determining $V_{GS,off}$ (V)

V_{range} and V_{off} are input voltages that can be applied to the gate drive circuit in order to set $V_{GS,on}$ and $V_{GS,off}$. For example, to achieve a gate-voltage range of 1 to -9 V, V_{range} and V_{off} are respectively set to 10 and 9 V. The upper level of the gate-voltage range is limited by the internal gate-source diode (D_{int}) of the GaN DHFET to be at most 1.5 V. The lower level of the gate-voltage range is preferably sufficiently negative in order to realize a fast turn-off switching of the transistor, since the threshold voltage of the E-mode GaN DHFET used for this study is only slightly above zero Volt.

C. Magnetics: planar inductor

The inductor used in the boost converter is an in-house developed planar inductor. This type of inductor allows for easy and fast assembly and offers the flexibility of tailoring the sizes and shapes of the individual turns. In addition, it is a more competitive and effective approach in terms of physical size reduction compared to the conventional type of inductor, keeping the converter design as compact as possible [7]. Fig. 2 depicts an exploded view of such a planar module, showing the planar ferrite cores together with the flat PCB windings. The specifications of the used planar inductor are listed in table I. Three E/PLT cores of the magnetic material 3F3 were used in combination with an air gap length $G = 450$ μm, providing a total inductance factor $A_L = 3 \times 400 = 1200$ nH. In combination with six copper turns on the PCB, this results in a theoretical inductance of $L_{th} = 43.2$ μH, being sufficient to keep the current ripple under control in the studied frequency range. The real inductance slightly differs from the theoretical one as in practice the air gap length is difficult to control precisely. The real inductance of the planar inductor was measured to be $L_{meas} = 33.9$ μH. This was done by evaluating the change of inductor current during the on-state of the transistor at a given input voltage V_{in}. The inset of Fig. 5 shows an example of such an inductor current waveform. The physical volume of the inductor was calculated out of the core dimensions to be $V = 19.3$ mm^3 with a surface $A = 19.4$ mm^2 and a height $h = 9.98$ mm.

TABLE I
PLANAR INDUCTOR: SPECIFICATIONS

Core type	3 x E32/6/20-PLT32/20/3
Core material	3F3
Number of turns (N)	6
Gap length (G)	450 μm
Total inductance factor (A_L)	$3 \times 400 = 1200$ nH
Theoretical inductance (L_{th})	43.2 μH
Measured inductance (L_{meas})	33.9 μH
Physical volume (V)	19.3 mm^3
Surface (A)	19.4 mm^2
Height (h)	9.98 mm

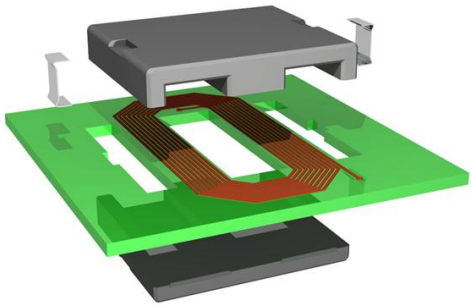

Fig. 2. Exploded view of a planar inductor, showing the planar ferrite cores and the flat PCB windings [8]

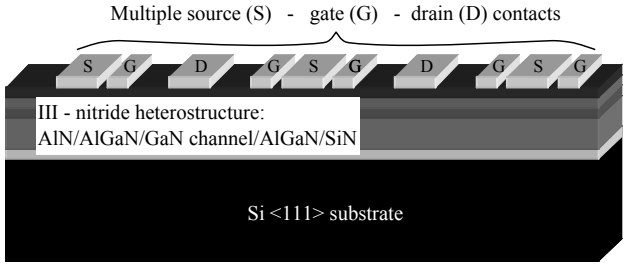

Fig. 3. Simplified cross-section of the GaN DHFET device. The power device is a lateral FET device, having multiple source (S) / gate (G) / drain (D) contacts on top of the III-nitride heterostructure.

III. GaN enhancement mode (E-mode) devices

A. Device fabrication

The used transistors are large (total gate width W_G = 57.6 mm, gatelength $L_G = 1.5$ μm) enhancement mode (E-mode) DHFETs, which are formed by parallelling smaller devices ($W_G = 400$ μm) via an interconnection layer. These lateral power components are fabricated starting from a $Si_3N_4/Al_{45}Ga_{55}N/GaN/Al_{18}Ga_{82}N$ MOCVD grown heterostructure on a Si<111> substrate [9]. The in-situ grown 50 nm Si_3N_4 layer caps the III-nitride heterostructure, passivating the surface and preventing strain relaxation of the $Al_{45}Ga_{55}N$ top layer [10]. In order to obtain an E-mode device, having a threshold voltage $V_{th} > 0$, the $Al_{45}Ga_{55}N$ barrier thickness is scaled down to a thickness below 5 nm and at the same time the in-situ grown Si_3N_4 is selectively removed under the gate [5]. Fig. 3 shows a simplified cross-section of the GaN DHFET device.

B. Device characterization

On-wafer transfer characteristic measurements on the small devices (total gate width $W_G = 200$ μm, gatelength $L_G = 1.5$ μm, and 4 nm top $Al_{45}Ga_{55}N$ layer) show a threshold voltage $V_{th} = 0.5$ V, an on-resistance $R_{on} = 12\ \Omega \cdot$ mm and a maximum saturation current $I_{DS} = 0.25$ A/mm. An off-state breakdown voltage V_{BD} of 600 V was obtained for a gate-drain gap $L_{GD} = 8$ μm and an $Al_{45}Ga_{55}N$ buffer-layer thickness of 2 μm [11].

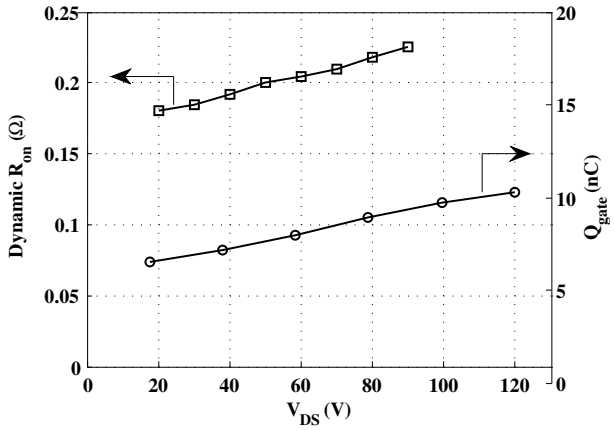

Fig. 4. Dynamic on-resistance (R_{dyn}) and total gate charge (Q_{gate}) of an E-mode GaN DHFET ($W_G = 57.6\ mm$), measured using the boost converter shown in Fig. 1.

The large devices were characterized using the boost converter setup [12]. Fig. 4 shows the measured dynamic on-resistance (R_{dyn}) and total gate charge values (Q_{gate}) of the GaN transistor. The dynamic on-resistance [13] is around 0.23 Ω and only shows a very minor increase with increasing off-state drain voltage ($V_{DS,off}$), proving the absence of the surface or bulk electron trapping in the device. A total gate charge value of 10 nC is obtained at $V_{DS,off} = 120$ V. These excellent properties result in low transistor losses (conduction respectively switching). To integrate the GaN DHFETs into power electronic circuits, the dies are packaged onto an AlN ceramic carrier (see inset of Fig. 1), acting as a heat spreader. Furthermore, the AlN carrier is mounted on an additional Al heat sink. A fan was used to force the convectional heat removal.

IV. Performance and discussion

A. Efficiency measurements: results

The performance of the converter was analyzed using a PM6000 Power Analyzer from Voltech. Input and output power are respectively measured through input channels I and II (see measurement setup in Fig. 5). For monitoring the waveforms of interest, a Tektronix oscilloscope was used in combination with a 1:100 voltage probe to measure voltages and with a differential probe to measure the inductor current via a shunt resistor ($R_{sh} = 0.083\ \Omega$). Both the voltage probe and differential probe have a bandwidth of 500 MHz. The inset of Fig. 5 shows an example of the voltage and current waveforms respectively measured at the drain of the GaN switch and through the inductor when operating with 149.2 W output power at 710.6 kHz switching frequency. Other operating parameters include a DC input voltage of 80.3 V, a DC output voltage of 170 V and a duty cycle of around 50%.

The converter was tested at several output voltages, frequencies and output power ranges, while keeping the duty cycle constant at approximately 50%. Fig. 6 shows the efficiency

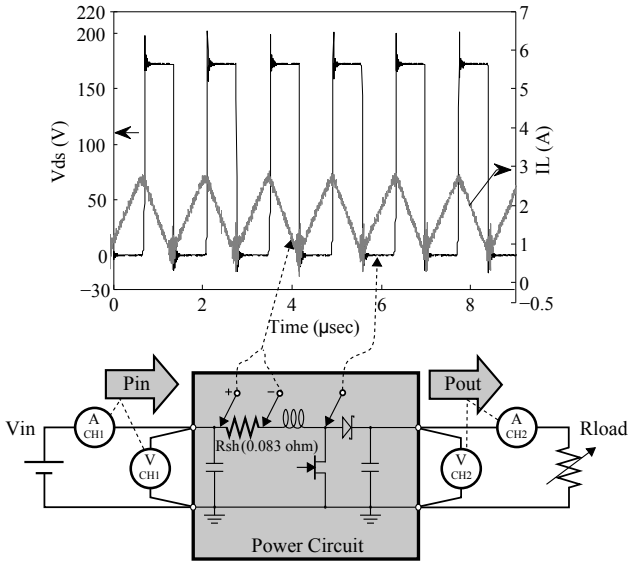

Fig. 5. Setup for measuring the input power, output power, inductor current and drain-voltage of the boost converter. (upper inset) Voltage and current waveforms, respectively measured at the drain of the GaN switch and through the inductor, showing hard-switched characteristics. Operating conditions include: $P_{out} = 149.2$ W, $V_{out} = 170$ V, $f = 710.6$ kHz and $D = 50$ %.

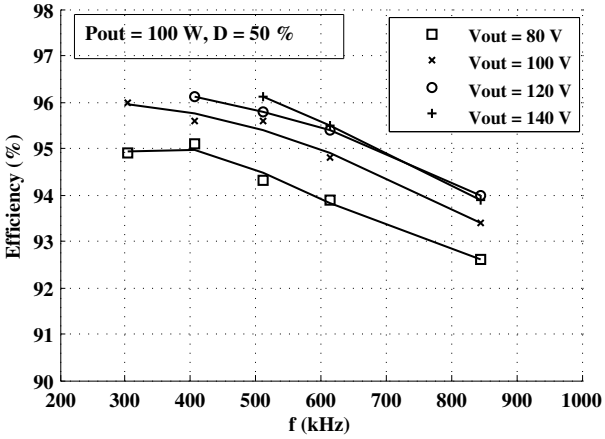

Fig. 6. Measured converter efficiency as a function of switching frequency, for various output voltages, at 100 W output power and 50 % duty cycle.

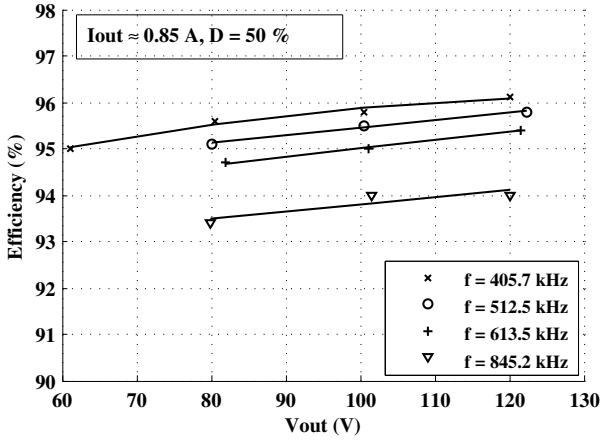

Fig. 7. Measured converter efficiency as a function of output voltage, for various switching frequencies, at 0.85 A output current and 50 % duty cycle.

measurements at 100 W output power for various output voltages in a frequency range from 303.8 to 845.2 kHz. The efficiency decreases, as expected, linearly with frequency. For an output voltage of 140 V the efficiency varies from 96.1% at 512.5 kHz to 93.9% at 845.2 kHz. To our knowledge, these are the highest efficiencies reported for an enhancement mode GaN DHFET on a Si substrate in these operating conditions and frequency range [4]. The measured efficiencies include input filter, output filter and wiring losses. Losses in the shunt measurement resistor are excluded through the calculations. In theory, with the same power level, the conduction loss remains constant, whereas the switching loss linearly increases with switching frequency. However, at elevated switching frequencies, the slope of the total efficiency decrease in Fig. 6 becomes steeper, being an effect of increased eddy-current, proximity and hysteresis losses in the inductor as also of the reduced skin depth in the capacitor films. It can also be seen that the efficiency is higher at increased output voltages, as was expected. From Fig. 6 it is clear that when decreasing the frequency or working at higher voltages, even higher efficiencies can be reached. This is also illustrated by Fig. 7 where the conversion efficiency is shown for various switching frequencies in an output voltage range from 60 to 120 V at 0.85 A output current and 50% duty cycle.

B. Distribution of the converter losses

An evaluation of the converter losses was performed based on SPICE simulations in combination with a MATLAB calculation model using generic formulas. A SPICE model for the GaN DHFET was made before, starting from the DC and CV characterization of the devices [14]. Fig. 8 shows the distribution of the converter losses, expressed as percentage converter efficiency decrease, at 845.2 kHz switching frequency, 142 V output voltage and 100 W output power. It can be seen that a major amount of the losses are switching related (2.7 % efficiency decrease). Also the inductor has a substantial contribution to the overall converter losses, especially at this high frequency. The remarkable high turn-on loss of the GaN transistor is a result of a high fall time of the drain-voltage, finding its cause in the limited upper level of the gate-voltage range as explained in section II-B. Fig. 9 shows, for illustration, an example of the rise and fall flanks of the measured drain-voltage waveform at 179.5 V output voltage, 405.8 kHz switching frequency and 50% duty cycle. The fall time ($t_{fall} \approx 26$ ns) is much higher than the rise time ($t_{rise} \approx 5$ ns). These numbers were read from the oscilloscope. One can also see that the measured waveforms are in very close agreement with the SPICE simulations.

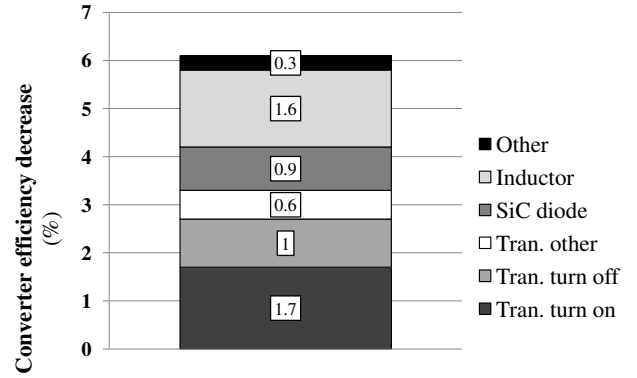

Fig. 8. Distribution of the converter losses at $P_{out} = 100$ W, $V_{out} = 142$ V, $f = 845$ kHz and $D = 50$ %.

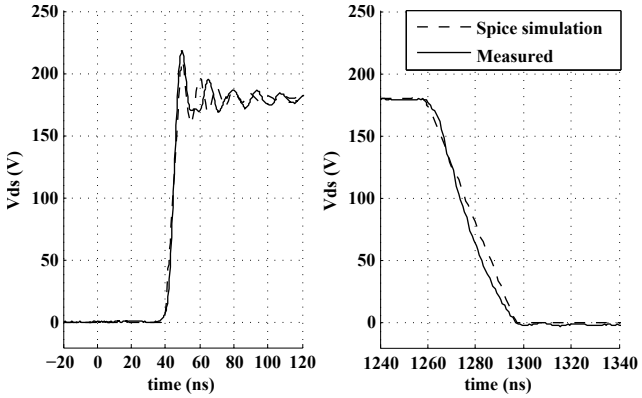

Fig. 9. Example of the rise and fall flanks of the measured drain-voltage waveform at $V_{out} = 179.5$ V, $f = 405.8$ kHz and $D = 50$ %. $t_{rise} \approx 5$ ns (left) and $t_{fall} \approx 26$ ns (right).

C. Improved on-switching: impact on the converter efficiency

As the turn-on losses are one of the major contributors to the overall efficiency decrease, it is accountable to have a close look to their origin. According to the current and voltage profiles shown in Fig. 10, the switching losses can be described by the following equations:

$$P_{SW} = P_{SW,on} + P_{SW,off} \tag{2}$$

where

$$\begin{aligned} P_{SW,on} &= \frac{I_D \cdot V_{DS,off}}{2} \cdot \frac{t_2 + t_3}{T} \\ P_{SW,off} &= \frac{I_D \cdot V_{DS,off}}{2} \cdot \frac{t_b + t_c}{T} \end{aligned} \tag{3}$$

with

P_{SW}	total switching loss (W)
$P_{SW,on}$	turn-on loss (W)
$P_{SW,off}$	turn-off loss (W)
I_D	drain current (A)
$V_{DS,off}$	off-state drain-source voltage (V)
t_2	rise time of the drain current (ns)
t_3	fall time of the drain voltage $= t_{fall}$ (ns)
t_b	rise time of the drain voltage $= t_{rise}$ (ns)

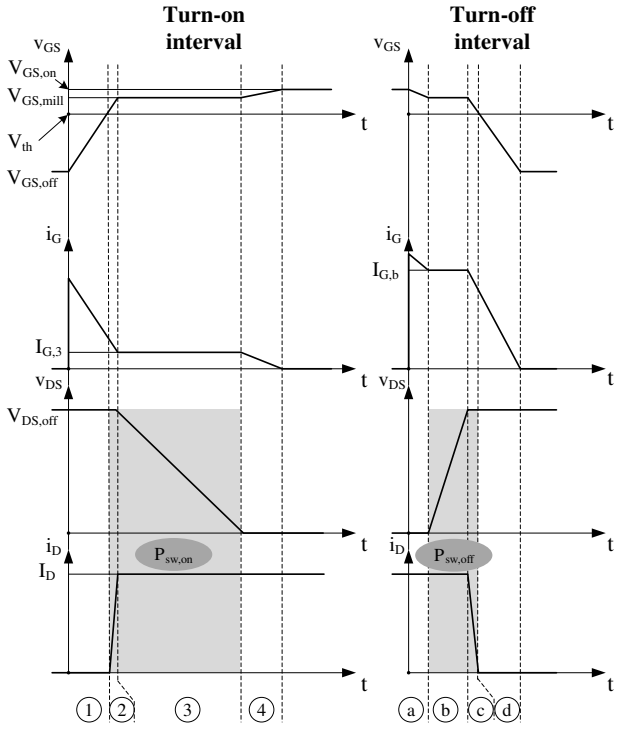

Fig. 10. GaN DHFET turn-on (left) and turn-off (right) intervals.

t_c	fall time of the drain current (ns)
v_{GS}	instantaneous gate-source voltage (V)
$V_{GS,mill}$	MILLER voltage (V)
i_G	instantaneous gate current (A)
$I_{G,3}$	gate current during time interval 3 (A)
$I_{G,b}$	gate current during time interval b (A)
i_D	instantaneous drain current (A)

Most of the switching losses are situated in time intervals t_3 and t_b. During these intervals the gate-drain capacitance (C_{rss}) is charged/uncharged until a $V_{DS,off}$ voltage change across its terminals is reached. For the measurement shown in Fig. 9, $t_3 = t_{fall} \approx 26$ ns and $t_b = t_{rise} \approx 5$ ns. According to the equations for charging/uncharging the capacitor C_{rss}, the difference in fall (t_3) and rise (t_b) times is related to the gate-current (I_G) in these intervals:

$$t_3 = C_{rss} \cdot \frac{V_{DS,off}}{I_{G,3}} \qquad t_b = C_{rss} \cdot \frac{V_{DS,off}}{I_{G,b}} \qquad C_{rrs} = C_{GD} \tag{4}$$

Hereby, I_G is constant during each interval (t_3 and t_b) and is determined by:

$$I_G = \frac{V_{A-B}}{R_{G,tot}} \qquad V_{GS,mill} \approx 0\ V \tag{5}$$

with

$$\begin{aligned} V_{A-B,t3} &= V_{GS,on} - V_{GS,mill} \\ R_{G,tot} &= R_{dr,hi} + R_G + R_{G,i} \end{aligned} \tag{6}$$

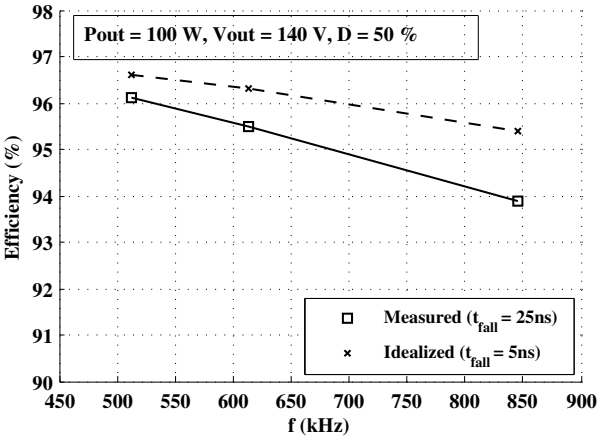

Fig. 11. Idealized efficiency assuming t_{fall} to be as small as $t_{rise} \approx 5$ ns. $V_{out} = 140$ V, $P_{out} = 100$ W.

and

$$\begin{aligned} |V_{A-B,tb}| &= |V_{GS,off}| + V_{GS,mill} \\ R_{G,tot} &= R_{dr,lo} + R_G + R_{G,i} \end{aligned} \quad (7)$$

V_{A-B}	driving voltage (V)
$R_{G,tot}$	total gate resistance (Ω)
$R_{dr,hi}$	internal high level output resistance of the driver (Ω)
$R_{dr,lo}$	internal low level output resistance of the driver (Ω)
R_G	external gate resistance (Ω)
$R_{G,i}$	internal gate resistance of the GaN DHFET (Ω)

$V_{GS,on}$ is limited by the internal gate-source diode D_{int} of the GaN DHFET. This means that the driving voltage $V_{A-B,t3}$ during t_3 is limited to only 1.5 V. In contrast, $V_{GS,off}$ is not limited and was chosen to be ≈ -9 V, resulting in a bigger driving voltage $V_{A-B,tb}$ during t_b of 9 V. This explains that $t_3 \gg t_b$. We conclude that in order to decrease the turn-on time, the positive gate-voltage swing needs to be increased. This can be realized by replacing the Schottky gate by a MOS gate. Fig. 11 shows for an output voltage of 140 V and an output power of 100 W what the efficiency would be if assuming that t_{fall} would be as small as $t_{rise} \approx 5$ ns. Now the efficiency varies from 96.6 % at 512.5 kHz to 95.4 % at 845.2 kHz instead of 96.1 respectively 93.9 %. Fig. 12 compares the new distribution of the converter losses with the one already mentioned in Fig. 8. The efficiency increase is around 1.5 %.

V. Conclusion

A high-frequency, hard-switching boost converter was constructed to test E-mode AlGaN/GaN/AlGaN double-heterostructure FETs and to investigate their benefit concerning converter efficiency and circuit compactness. The low dynamic on-resistance and low gate charges of the components result in low transistor losses, enabling very high switching frequencies and a compact converter design. A high power

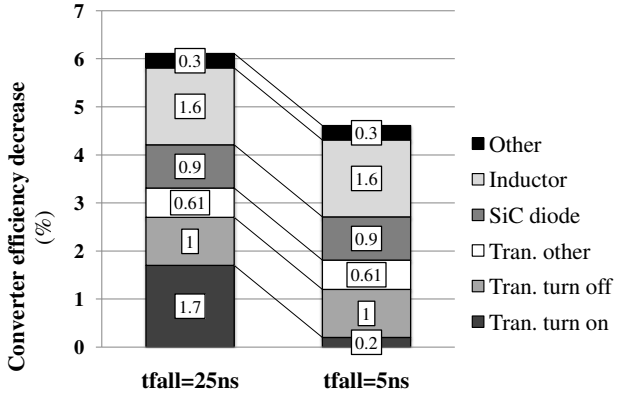

Fig. 12. Distribution of the converter losses at $P_{out} = 100$ W, $V_{out} = 142$ V, $f = 845$ kHz and $D = 50$ %.

efficiency of 93.9 to 96.1 % was reached in the 512-845 kHz frequency range at 100 W output power and 140 V output voltage. These are, to our knowledge, the highest efficiencies reported for an E-mode GaN DHFET on Si in this frequency range. Allowing higher positive gate drive voltages would increase these efficiencies to 95.4 respectively 96.6 %. By analyzing the power loss distribution in the converter, it was seen that a major amount of the losses are switching related. Also the passives substantially contribute to the overall converter losses, especially at higher frequencies. The optimization of these components, as well as driving the devices at higher gate voltages does offer a clear roadmap to even higher converter efficiencies.

Future work

Future work includes an optimization of the planar inductor. Crucial in the design of the inductor is the air-gap position as also the right choice of the core material. New core materials (3F45) have been developed and will be considered in the near future. A comparison with commercially available GaN devices (e.g. EPC) belongs also to the future roadmap.

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