# A Hard Switching VIENNA Boost Converter for Characterization of AIGaN/GaN/AIGaN Power DHFETs

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## Abstract

A high frequency, hard switching boost converter (VIENNA topology) was constructed for characterizing new power AlGaN/GaN/AlGaN Double Heterojunction Field Effect Transistors (DHEFTs) under operating conditions. This converter enables us to accurately measure the, in power circuit design, most important device parameters (dynamic on-resistance  $R_{dyn}$ , gate charge  $Q_g$ , Miller charge  $Q_{gd}$ , threshold voltage  $V_{th}$ , switching times  $t_{on}$  and  $t_{off}$ , figure of merit FOM, ...). A high accuracy is achieved by using the right measurement methods combined with an in-house developed accuracy/resolution-improvement circuit. Measurements of the dynamic on-resistance, together with gate charge measurements were performed on AlGaN/AlGaN DHEFT prototypes, showing good results.

## 1. Introduction

Recent technological improvements made GaNbased heterojunction field effect transistors (HFET's) a good replacement candidate for the currently used silicon devices in power electronic converters [1, 2]. The advantages of these new power devices are very promising for future energy conversion applications [3, 4], resulting in loss reductions and higher switching frequencies (more compact design).

One of the biggest concerns when using GaNbased HFETs as a power switch is the possible increase of the "dynamic" on-resistance ( $R_{dyn}$ ) when applying high voltage swings to the drain [5]. This effect, having a direct impact on the conduction losses of the circuit, is often called "drain current dispersion" and it can be explained by charge trapping at the surface or in the bulk of the III-nitride heterostructure. The trapped charge acts as a virtual gate and depletes the two-dimensional electron channel, resulting in a decreased drain current and an increased onresistance [6].

A second important parameter of interest is the gate-drain charge  $(Q_{ad})$ , often used in discus-

sions concerning switching speed and driver design [5]. The smaller  $Q_{gd}$ , the faster the switching. When multiplying  $Q_{gd}$  with  $R_{dyn}$ , a figure of merit (FOM) is obtained, making comparison of different devices possible.

This paper presents a hard switched VIENNA converter, enabling fast and accurate measurement of the two key quantities ( $R_{dyn}$  and  $Q_{gd}$ ). Also switching times ( $t_{on}$  and  $t_{off}$ ), currents and temperatures can be measured. Effort was put in making the power circuit extremely compact, reducing the parasitic influences to a minimum. The test conditions represent real operating circumstances, giving a good insight in the performance of the devices in a real converter.

Dynamic on-resistance, gate charge and switching times of newly developed AlGaN/GaN/AlGaN DHFET prototypes were measured and results are presented. The used measurement methods and possibilities to improve accuracy are discussed. Special attention goes to a circuit for clamping the "off"-state drain to source voltage to a diode voltage drop, improving measurement accuracy/resolution.

## 2. Converter construction

For characterizing and testing high voltage power switches, a hard switching circuit topology seems to be the right choice. The tested devices are stressed to a maximum (inductive switching) and useful information about their behaviour under operating conditions is acquired, knowing that many practical converter topologies are hard switching. Choosing a VIENNA converter [7] enables us to simultaneously test two, whether or not equal, devices while keeping operating conditions the same. Fig. 1 shows the main power circuit diagram of the VIENNA converter with its two separately driven, superimposed boost stages. Each boost stage has a power rating of 3,5 kW and a maximum output voltage of 600 V. The switching frequency range lies between 100 kHz and 2 MHz.

### 2.1. Main power circuit

The main power circuit in Fig. 1 has two identical boost stages, each containing an Al-GaN/GaN/AlGaN DHFET power switch, a filtration capacitor ( $C_{out}$ ), a rectifying diode ( $D_3$  or  $D_4$ ), a "selection" diode ( $D_1$  or  $D_2$ ), an inductor (L) and a load ( $R_1$ ). There is only one commonly used inductor in the circuit and only one boost stage is used at a time.



**Fig. 1.** Main power circuit diagram of the hard switching VIENNA converter.

The upper boost stage is "selected" by supplying a positive input voltage ( $V_{in}$ ) to the converter and putting the upper DHFET in "switching" mode. The lower "selection" diode ( $D_2$ ) is then reverse biased, while the upper one ( $D_1$ ) permanently conducts current. The lower DHFET conducts no current and its state ("switching", "on" or "off") is of no importance. The lower boost stage is "selected" by supplying a negative input voltage ( $V_{in}$ ) to the converter and putting the lower DHFET in "switching" mode. Now the upper DHFET conducts no current and its state is of no importance. The power circuit was built on a two-layer printed circuit board. The catch diodes are 600 V, 6 A SiC Schottky diodes, offering superior switching characteristics with very low recovery current. The selection diodes are 600 V, 9.5 A rated rectifying diodes, having a low forward voltage drop of 0.9 V at rated current. An in-house developed planar inductor was used, keeping the design as compact as possible. Fig. 2 shows the converter setup with its cooling facilities. The tested Al-GaN/GaN/AlGaN DHFET prototypes are bare die attached on an AIN plate (see inset of Fig. 2). This was glued on a copper plate, being screw mounted on an aluminium heat sink. A fan forces the convectional heat removal.



**Fig. 2.** Converter setup with its two heat sinks, planar inductor, output capacitors and a fan to force the convectional heat removal. (Inset) Al-GaN/GaN/AlGaN DHFET with its AIN substrate.

### 2.2. Drive circuit

The AIGaN/GaN/AIGaN DHFET prototypes we used in our test setup are field effect transistors (FET). A voltage applied to the gate induces an electrical field. This field controls the flow of charges between source and drain. In contrast to a conventional silicon FET, the channel of electrons is present without applying a voltage to the gate [4]. By applying a negative voltage to the gate, the channel is pinched off and the transistor is in its off-state. This makes an Al-GaN/GaN/AIGaN DHFET a "normally on" device instead of a "normally off" in the case of a silicon FET. As a result, being able to supply negative gate voltages is a first requirement of the gate drive circuit. A second requirement is that the driver must be able to reach high frequencies (up to 2 MHz), being the range where the GaNbased devices are supposed to be used [3]. Two gate drive circuits are constructed to meet these requirements, providing a fully controllable drivevoltage range V<sub>A</sub> (see Fig. 3):

$$\Rightarrow V_{A} = \begin{bmatrix} 0 - V_{off} & / & V_{dd} - V_{off} \end{bmatrix}$$

Where  $V_A$  is set by controlling  $V_{off}$  and  $V_{dd}$ . Even positive voltage ranges are possible by simply removing the offset voltage Voff, giving the possibility to also test conventional (normally-off) silicon power transistors. The external gate resistor  $(R_{q})$ , determining switching speed, can easily be replaced as preferred to investigate its influence on the behaviour of the tested devices. The inset of Fig. 3 shows the gate voltage waveform, measured directly at the gate (point B) of an Al-GaN/GaN/AIGaN DHFET. The pulsed voltage has a frequency of 303.6 kHz, a duty cycle of 50.02 % and a range of -9.6 V / 0.34 V. The rise and fall times are 19 and 18.7 ns, respectively. As will be shown this results in even faster transistor switching times ( $t_{on}$  and  $t_{off}$ ).



**Fig. 3.** Principle scheme of the gate drive circuit. (Inset) Waveform at the gate (point B), showing a voltage range of -9.6 V / 0.34 V.

### 3. Tested AlGaN/GaN/AlGaN DHFET Prototypes

The GaN-based transistors we used in our test setup are AlGaN/GaN/AlGaN DHFETs (Double Heterojunction Field Effect Transistors) [8]. They have a gate length of 1.5  $\mu$ m and a total gate width of 57.6 mm. See also Fig. 4. III-nitride (e.g. GaN) devices exhibit in general a high breakdown voltage due to their high field strength

(~ 3.5 MV/cm), being an order of magnitude better than that of silicon. Additionally, a very low on-resistance and a high switching speed can be obtained due to the two-dimensional electron gas (2DEG) of AlGaN/GaN based heterostructures, having a high mobility and large carrier concentration. Finally, the wide band-gap properties also enable operation at high temperatures.





**Fig. 4.** Simplified cross-section of the GaN DHFET device. The power device is a lateral FET device, having multiple source (S) / gate (G) / drain (D) contacts on top of the III-nitride heterostructure.

### 4. Dynamic on-resistance measurements

As explained earlier in the introduction, the dynamic on-resistance ( $R_{dyn}$ ) is defined as the instantaneous on-resistance of a device shortly after a high-voltage event [3]. As a consequence the most important parameter of influence is the off-state drain to source voltage. Other parameters (switching frequency, load impedance, duty cycle, current,...) are of less influence on the dynamic on-resistance. The conduction losses of a switching converter are proportional to  $R_{dyn}$ .

### 4.1. Measurement method

In literature, different methods for measuring the dynamic on-resistance of a power transistor are used. Some references [4, 5] continuously switch a resistive load, while others [3] use an inductive load. Various switching frequencies, currents and duty cycles are mentioned and post-processing of the measurement data deviates from one reference to another. The test setup presented in this paper measures the dynamic on-resistance in a hard switching GaN-based converter, representing conditions that are likely to occur in real converter implementations. This means inductive switching, relatively high frequencies (0.1 - 2 MHz), higher currents (2 - 5 A) and duty cycles between 20 and 60%. The whole on-interval data

is captured and can be post processed in either way.

Determining the dynamic on-resistance of a transistor by measurement is based on Ohms law, stating that:

$$R_{dyn} = \left(\frac{V_{ds}}{I_d}\right)_{ol}$$

where  $V_{ds}$  and  $I_d$  are respectively the drain-tosource voltage and drain-current during the onstate of the transistor.  $V_{ds}$  is measured with a voltage probe while  $I_d$  is measured using a shunt resistor and a differential probe. Fig. 5 shows the place of the probes and shunt resistor. The DC output bus midpoint of the power circuit is fixed to the ground of the oscilloscope, making simultaneous measurement of the two boost stages possible.



**Fig. 5.** Place of probes and shunt resistor for measuring the dynamic on-resistance  $R_{dyn}$ .

# 4.2. Measurement-resolution improvement circuit

When putting the voltage probes directly on the drain and source terminals of the transistor, a measurement resolution problem occurs. The reason is having large (off-state voltage) and small (on-state voltage) signals together in one measurement, giving an inaccurate on-state voltage drop value. Increasing the resolution by increasing the voltage sensitivity is not an option as the oscilloscope's internal amplifier becomes overdriven, giving poor results. The used oscilloscope (Tektronix 7254) has an 8-bit analog-todigital converter (ADC), giving 256 levels to divide the measured range in. When the off-state voltage is 400 Volts for example, the maximum resolution is 400/256 = 1,56 V. This is unacceptable for an accurate measurement of the onstate voltage drop. The dynamic range of an oscilloscope is a quantity that shows how well the oscilloscope can detect small signals in the presence of large signals. It is expressed in decibels (dB). The quantization error together with other noise sources (background noise, distortion, ...) limits this quantity. The equation for computing the dynamic range is:

dynamic range (db) = 20 log (
$$V_{max}/V_{min}$$
)

with  $V_{\text{max}}$  the maximum voltage that must be measured and  $V_{\mbox{\scriptsize min}}$  the minimum resolution. It can be seen that every bit of resolution stands for approximately 6 dB of dynamic range. This means that the 8-bit ADCs of our oscilloscope have a theoretical maximum dynamic range of 48 dB. Actually is it less due to above mentioned limitations. As a result, resolution can be improved and saturation can be avoided by keeping V<sub>max</sub> low. Fig. 6 shows the circuit constructed for doing this by clamping the measured drainsource voltage to a diode voltage drop when the transistor is in its "off" state. The circuit is based on a Wilson current mirror [9], providing two equal currents through diodes 1 and 2 during the "on"-state interval of the transistor. This gives an identical voltage drop across these diodes (same type diodes), projecting the "on"-state voltage drop between measurement points A and B. During the off-state interval of the transistor, diode 2 is reverse biased, pushing the current through a clamping diode (this diode can be chosen by closing one of the switches). Now this diode's voltage drop appears between the measurement points, determining V<sub>max</sub> and resulting in a greatly improved resolution. Assuming a clamping voltage of 1 V for example, the resolution becomes 1/256 = 0.0039 V. The on-state drain-source voltage is not allowed to become bigger than the clamping voltage as in this case it is never projected to the measuring points. By putting some diodes in series or by using a Zener clamping diode, bigger on-state voltages can be measured. The clamping circuit was designed to produce a current with an order of magnitude of a mA, giving a neglecting influence on the power circuit. The Wilson current mirror topology was chosen to avoid the Early effect of the two (necessarily identical) upper BJT transistors. Two emitter resistors ( $R_1$  and  $R_2$ ), carrying a few tenths of a Volt, were placed for optimizing the circuit (dealing with temperature differences, transistor characteristic variations,...).

### 4.3. Results of measurements

Fig. 7 shows an example of a dynamic onresistance measurement on an Al-GaN/GaN/AlGaN DHFET (off-state  $V_{ds} = 90$  V, f = 300 kHz and D = 50 %). The average input current was 1.5 A. Figure (a) shows the difference between the measured  $V_{ds}$  with ("real  $V_{ds}$ ") and without ("projected  $V_{ds}$ ") using the resolution improvement circuit of figure 6. The off-state drain to source voltage was clamped to 2.4 V by a Zener diode (a) and (b), giving a very good measurement resolution of 2.4 V/256 = 0.0094 V. The dynamic on-resistance (c) was calculated out of the projected V<sub>ds</sub> and on-state drain current (=I<sub>d</sub> = I<sub>shunt,on</sub>) from (b), resulting in a very low R<sub>dyn</sub> of approximately 0.2 ohm.



**Fig. 6.** Circuit for improving measurement resolution/accuracy at high off-state voltages. This circuit is based on a Wilson current mirror.

### 5. Gate-drain charge measurements

When switching an AlGaN/GaN/AlGaN DHFET, the gate-drain and gate-source capacitances ( $C_{gd}$  and  $C_{gs}$  respectively) are charged and discharged. This requires a total gate charge ( $Q_g$ ) being supplied by the gate drive circuit through the external gate resistance ( $R_g$ ). Switching time of a power electronic transistor in a converter however is only determined by the charging and discharging times of the gate-drain capacitance ( $C_{gd}$  = Miller Capacitance) [5], requiring a gatedrain charge ( $Q_{gd}$ ) which is independent from the gate-drive condition. This independency makes  $Q_{gd}$  a good quantity to discuss switching times. Switching loss is proportional to  $Q_{gd}$ .

#### 5.1. Measurement method

 $Q_{gd}$  was determined by integrating the gate drive current during the turn-on switching of the transistor. The gate drive current was measured from the voltage drop across the external gate resistance  $R_g$ , using a differential probe. For these measurements a bigger  $R_g$  of 220  $\Omega$  was used,

resulting in a slower switching with less reflection of drain oscillations to the gate and hence making it easier to accurately determine  $Q_{gd}$ . A compromise was made in choosing  $R_g$  for giving a good measurement accuracy and not affecting the measurement too much.



**Fig. 7.** Dynamic on-resistance measurement  $(V_{ds,off} = 90 \text{ V}, \text{ f} = 300 \text{ kHz}, \text{ D} = 50 \% \text{ and } I_{in,ave} = 1.5 \text{ A})$ . Drain to source voltage with ("Projected") and without ("Real") resolution improvement circuit is shown in (a). Figure (b) presents the drain current and the projected drain to source voltage during on-state, resulting in a R<sub>dyn</sub> of approximately 0.2 ohm (figure c).

### 5.2. Results of measurement on Al-GaN/GaN/AIGaN DHFETs

Fig 8. shows an example of a gate charge measurement on an AlGaN/GaN/AlGaN DHFET (off-state V<sub>ds</sub> = 30 V, frequency = 300 kHz and duty cycle = 50 %). The average input current was 1.5 A. The gate-drain charge  $Q_{gd}$  was measured to be 0.65 nC. The Miller voltage V<sub>mill</sub> was -2.09 V and the total gate charge  $Q_g$  was 2.46 nC.



Fig. 8. Gate charge ( $Q_g$ ) and gate-drain charge ( $Q_{gd}$ ) measurement ( $R_g$  = 220 ohm,  $V_{gs}$  = -9.28 / 0.32 V,  $V_{ds,off}$  = 30 V, f = 300 kHz, D = 50 % and  $I_{in,ave}$  = 1.5 A).

## 6. Switching times

Switching times can be obtained from the oscilloscope waveforms by directly measuring the drain-source voltage with a voltage probe. At  $V_{ds}$  = 120 V,  $t_{on}$  and  $t_{off}$  are respectively 22 ns and 4.5 ns. These fast switching times are the result of driver design, combined with the very low gate capacitance of the AlGaN/GaN/AlGaN DHFETs.

## 7. Conclusion

The characterization of AlGaN/GaN/AlGaN DHFETs, using a hard switching VIENNA boost converter was demonstrated. Gate drive requirements for this type of devices were met by two dedicated gate drive circuits, offering a maximum flexibility for testing. Methods for fast and accurate measurement of dynamic onresistance ( $R_{dyn}$ ) gate-drain charge ( $Q_{gd}$ ) and switching times were proposed and demonstrated. A circuit for clamping the "off"-state drain to source voltage in  $R_{dyn}$ -measurement showed its value for improvement of measurement resolution.

## 8. Literature

- [1] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, T. Ogura, and H. Ohashi, "High breakdown voltage AlGaN-GaN power-HEMT design and high current density switching behavior," *IEEE Trans. on Electron Devices*, vol. 50, no. 12, pp. 2528–2531, Dec. 2003.
- [2] L. F. Eastman, and U. K. Mishra, "The toughest transistor yet," *IEEE Spectrum*, vol. 39, Issue 5, pp. 28-33, May 2002.
- [3] W. Yifeng, M. Jacob-Mitos, M. L. Moore, and S. Heikman, "A 97,8% efficiënt GaN HEMT boost convertor with 300- W output power at 1 MHz," *IEEE Electron Device Letters*, vol. 29, Issue 8, pp. 824-826, Aug. 2008.
- [4] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, "A 120-W Boost Converter Operation Using a High-Voltage GaN-HEMT," *IEEE Electron Device Letters*, vol. 29, NO. 1, Jan. 2008.
- [5] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, "Suppression of Dynamic On-Resistance Increase and Gate Charge Measurements in High-Voltage GaN-HEMTs With Optimized Field-Plate Structure," *IEEE Trans. on Electron Devices,* vol. 54, NO. 8, Aug. 2007.
- [6] G. Meneghesso, G. Verzellesi, R. Pierobon, Fabiana Rampazzo, A. Chini, U. K. Mishra, C. Canali, and E. Zanoni, "Surface-Related Drain Current Dispersion Effects in AlGaN–GaN HEMTs," *IEEE Trans. on Electron Devices*, vol. 51, Issue 10, pp. 1554-1561, Oct. 2004.
- [7] M. Hartmann, S. D. Round, H. Ertl, and J. W. Kolar, "Digital Current Controller for a 1 MHz, 10 kW Three-Phase VIENNA Rectifier," *IEEE Trans. on Power Electronics*, vol. 24, no. 11, pp. 2496-2508, Nov. 2009.
- [8] D. Visalli, M. Van Hove, J. Derluyn, S. Degroote, M. Leys, K. Cheng, M. Germain, and G. Borghs, "AlGaN/GaN/AlGaN Double Heterostructures on Silicon Substrates for High Breakdown Voltage Field-Effect Transistors with low On-Resistance", *Jpn. J. Appl. Phys.*, vol. 48, 04C101, Apr. 2009.
- [9] P. Horowitz, and W. Hill, "The Art of Electronics," *Cambridge University Press*, Second Edition, 1994.