A Remote-Powered RFID Tag with 10Mb/s UWB Uplink and -18.5dBm-Sensitivity UHF Downlink in 0.18μm CMOS

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A remote-powered UWB RFID tag in 0.18μm CMOS is presented. The innovation is to employ asymmetric communication links, i.e. UWB uplink and UHF downlink in order to achieve extremely low power, high data rate and accurate positioning. Measurement shows the tag can operate up to 10Mb/s with minimum input power of 14.1μW, corresponding to 13.9 meters of operation range.

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Wireless sensing and positioning are new added functions highly demanded in future and emerging RFID technology [1]. Data rate of existing passive RFID is limited to few hundreds of kb/s causing large latency. On the other hand, the position accuracy is not better than 70cm [2]. In a advanced design, 3.4Mb/s data rate has been achieved in proximity operation [3]. Active tags with narrowband radio link overcome these weaknesses but, they are battery powered and more expensive.

Impulse Ultra wideband (I-UWB) technique using short pulses for data transmission has been recognized as a powerful candidate for future RFID systems. It has the possibility of achieving MB/s throughput, operating range of several tens of meters, centimeters positioning, low power consumption, and low cost implementation. Previous works have revealed that UWB transmitter is extremely area and power efficient, whereas the receiver is still area and power hungry which requires internal power source [4].

In this work, we present a 10Mb/s impulse UWB RFID tag in 0.18μm CMOS. The tag is remotely powered by UHF wave with minimum input RF power as low as 14.1μW. Our innovative contribution is to employ two different communication links (UWB and UHF) respectively in uplink and downlink of the tag. This is because the amount of data or instruction from a reader to a tag is very few and a normal communication link as conventional UHF-RFID at 900 MHz could be used as downlink. UHF also provides remote power to the tag. The uplink requires higher data rate and precise positioning capability therefore an I-UWB transmitter is employed.

Fig. 1 shows the block diagram of the tag. A power scavenging unit consisting of 9-stages CMOS voltage multiplier rectifies the incoming 900MHz RF signal to DC in a storage capacitor. The instantaneous power consumption of the circuits is too high to be operated constantly by remote-power. Therefore, a voltage-sensor, which consumes less than 1.5μA, activates the operation only when the voltage in storage capacitor reaches 2.75 V. The required energy for operation is provided by the stored energy in the storage capacitor. The size of the storage capacitor depends on the operation time and the required current which can be in the order of hundreds of nano-farad and therefore off-chip capacitor is used. A low-drop-out (LDO) voltage regulator provides regulated voltage of 1.8V for the circuits. When the capacitor voltage becomes less than 1.9V, the operation is stopped and the storage capacitor is recharged again. Fig. 2 shows the power management unit including the power scavenging circuits, the voltage sensor, the voltage regulator, and the power-on-reset.

The envelope of the UHF signal contains data and clock for the tag. An envelop detector similar to power scavenging unit but with only 2-stages extracts the envelope. Fig. 2 shows the block diagram of the RF demodulator including envelope detector and data and clock recovery circuitry. It supports the 900 MHz ISM band with data rates up to 160 kbps. The extracted clock is used for logic control and no local oscillator is needed which not only reduces power consumption significantly, but also enables scalability to various operation frequencies and data rate for different power and distance constrains.

Fig. 2 shows the schematic of the impulse UWB transmitter. Since there is no local oscillator on chip, digital pulse generator, up conversion or FIR transmitter is not feasible [4, 5]. These circuits consume high power which is also prohibitive in the proposed tag. Therefore, we use continuous-time filter architecture. Since one pulse is generated at each falling edge of the incoming clock, the pulse rate can be adjusted by the digital control logic easily according to the available power and desirable operation distance. Although Binary phase shift keying (BPSK) modulation offers higher performance, it requires more complex circuitry to control the pulse shape. Furthermore, BPSK detection is very sensitive to clock jitter and skew and therefore demands a synchronized on-chip clock with high accuracy. In this work, on-off keying (OOK) modulation is utilized which is implemented totally in baseband and energy detection used in reader is insensitive to clock jitter. A low-power harmonic injection locked (HIL) divide-by-9 is used to down convert the 900 MHz carrier frequency to 100 MHz clock for UWB transmission which is shown in Fig. 2. Compared with PLL or LC oscillators based clock generator, our approach consume much lower power and small chip area.

A digital control logic core is designed for the proposed communication protocol based on slotted-ALOHA anti-collision algorithm. The sketch of communication protocol and control logic diagram is shown in Fig. 3. Frame time is divided into slots. A tag randomly selects a slot number and responds to the reader. Because of the asymmetry in communication links, the tag listens to the channel in next slot for an acknowledgment to resolve collisions or failed transmissions. Collided tags retransmit in next frames. Simulation results show the throughput more than 2000 tags per second resulting great improvement compared with normal RFID system which is at most 1000 tags/s [6].

The measurement setup is shown in Fig. 4. The input sensitivity of -18.5 dBm (14.1 μW) has been measured. It corresponds to 13.9 meters operation range considering 4W EIRP and antenna with 0dB gain resulting a great improvement compared with existing passive RFID [7]. This improvement is due to the new proposed operation method which reduces power consumption during harvesting time and improves input sensitivity. As can be seen in Fig. 4 with a storage capacitor of 211 nF, the charging time is 31 ms and the operation time is 1.9 ms and 0.184 ms for 10 MHz and 100 MHz pulse rate respectively.

ASK modulated RF signal such as EPC class 1 standard is used to measure the data and clock recovery performance and the results are shown in Fig. 5. The output impulse of the UWB transmitter has an amplitude of 220 mV_{PP} and a duration of 620 ps as illustrated in Fig. 5. At 10 MHz pulse rate it consumes 51µA@1.8V (91.8µW) and the power spectral density meets the FCC indoor regulation. This corresponds to 9.2 pJ/pulse which is much less than others reported [5].

The remote-powered UWB tag is fabricated in the UMC 0.18µm CMOS process. The active area is less than $1mm^2$. The performance of the chip is summarized in

Fig. 6 and the chip micrograph is shown in Fig. 7. The innovative contribution is to employ two different communication links (UWB and UHF) respectively in uplink and downlink of the tag. It allows long-range remote-power operation along with high data-rate and precise positioning capability. The input sensitivity is measured to be -18.5 dBm (14.1µW) corresponding to 13.9 meters operation range. The UWB transmitter consumes 918 µW instantaneous-power at 100 MHz pulse rate which corresponds to 9.2 pJ/pulse. The new proposed communication protocol allows more than 2000 tags/s to be proceeded which is a great improvement compared to existing RFID systems.

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Figure captions

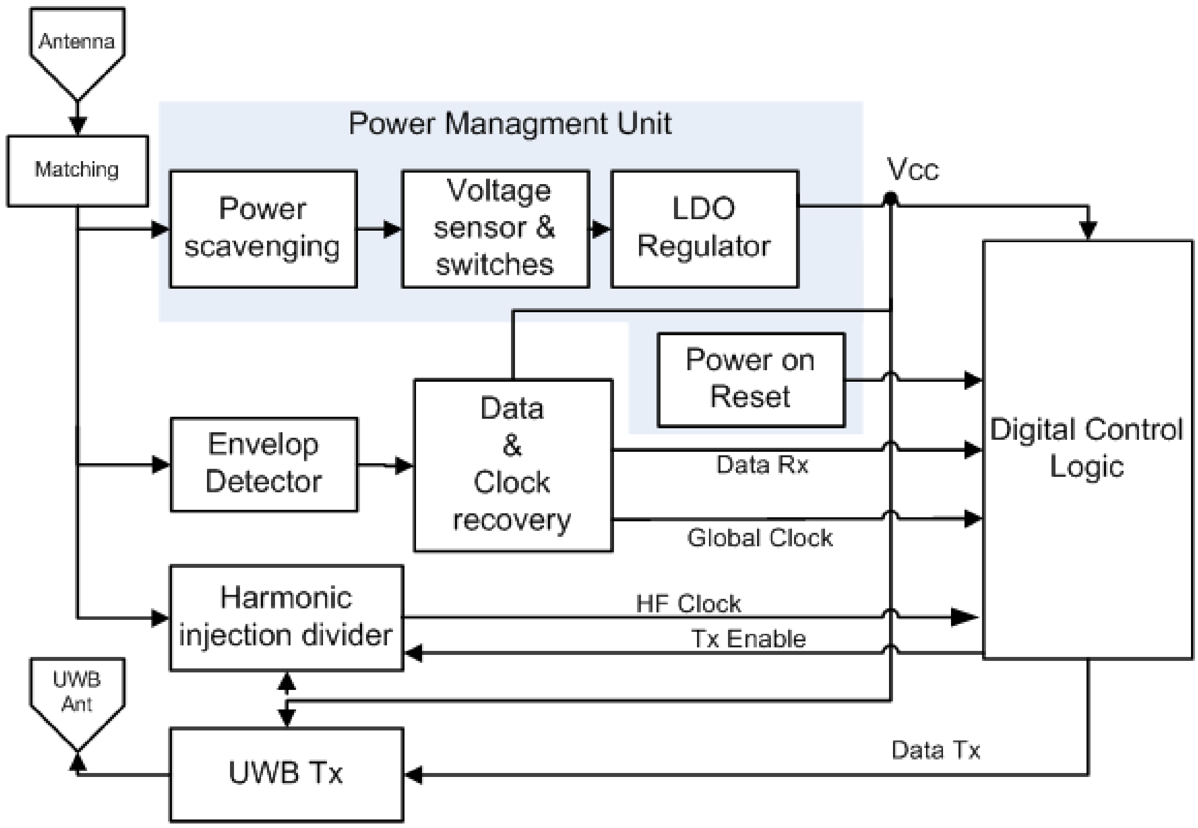


Fig. 1: Block diagram of the I-UWB RFID tag which is remote-powered by UHF Signal.

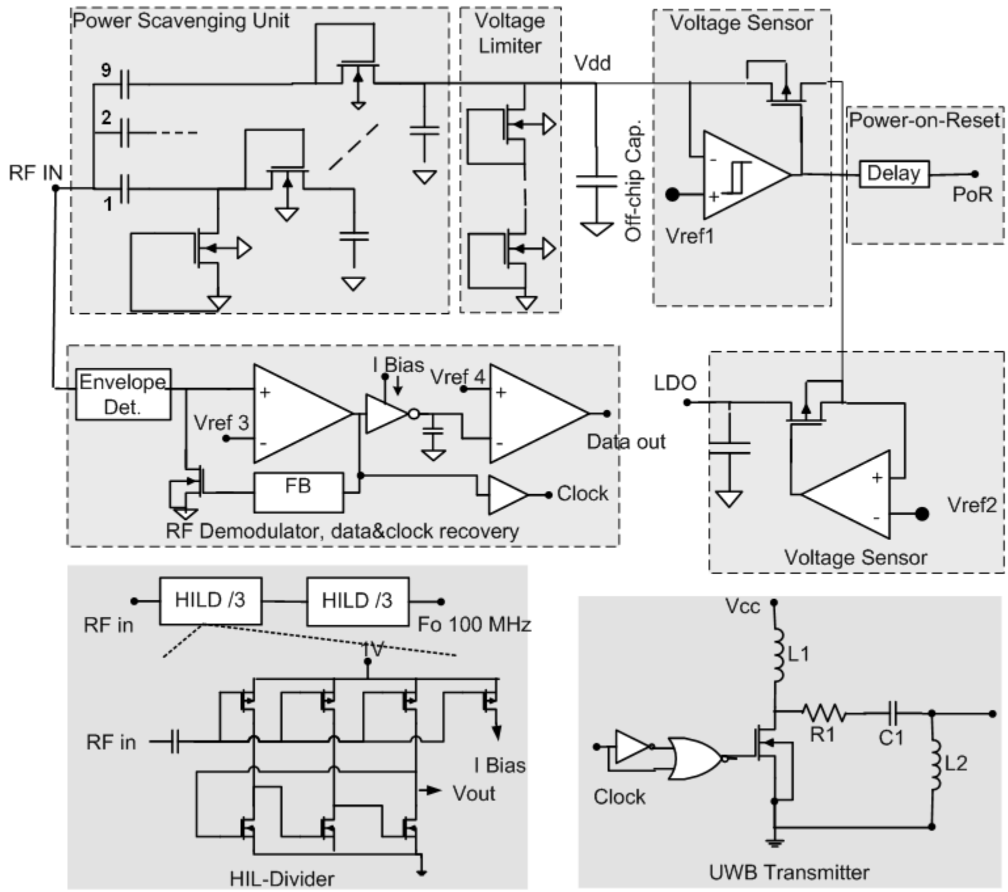
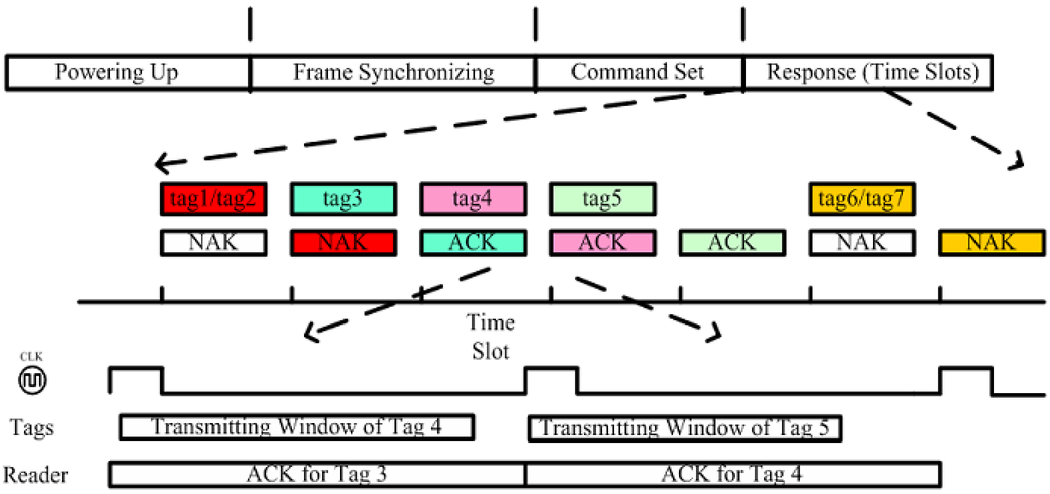
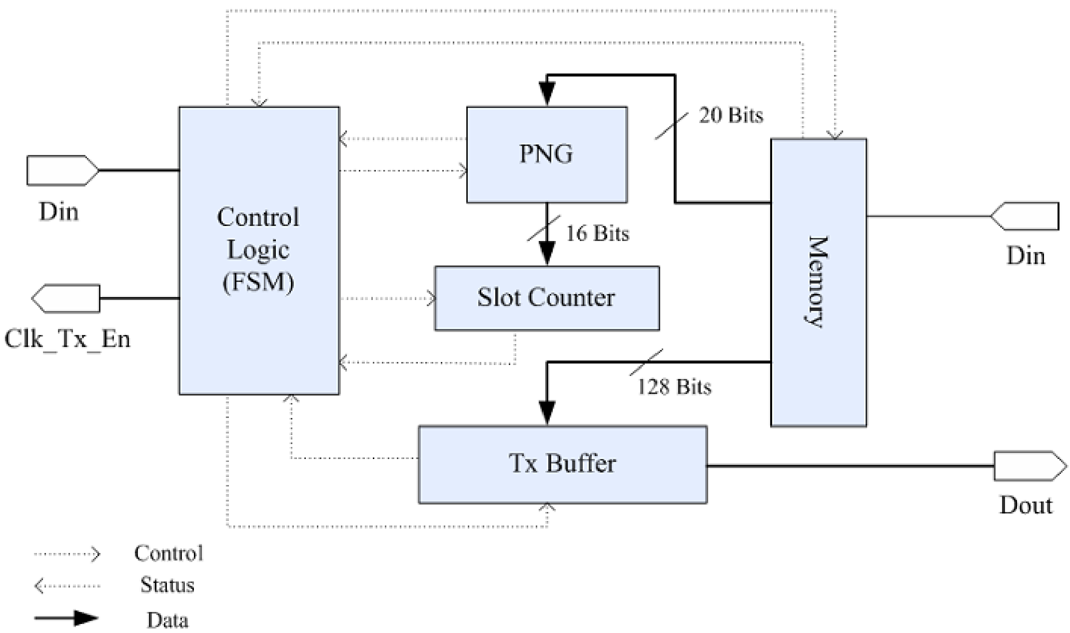


Fig. 2: Schematics of different building blocks of the tag, Top: power scavenging unit include voltage limiter, voltage sensor, and power on-reset circuits. Middle: UHF receiver which detects signal envelops and recovers data and clock, Bottom: low-power harmonic injection locked (HIL) divider for 100MHz UWB transmitter clock and UWB transmitter circuits



a) Communication protocol



b) Control Logic block diagram

Fig. 3: (a) Sketch of communication protocol based on slotted-ALOHA anti-collision algorithm, and (b) block diagram of the digital control logic core.

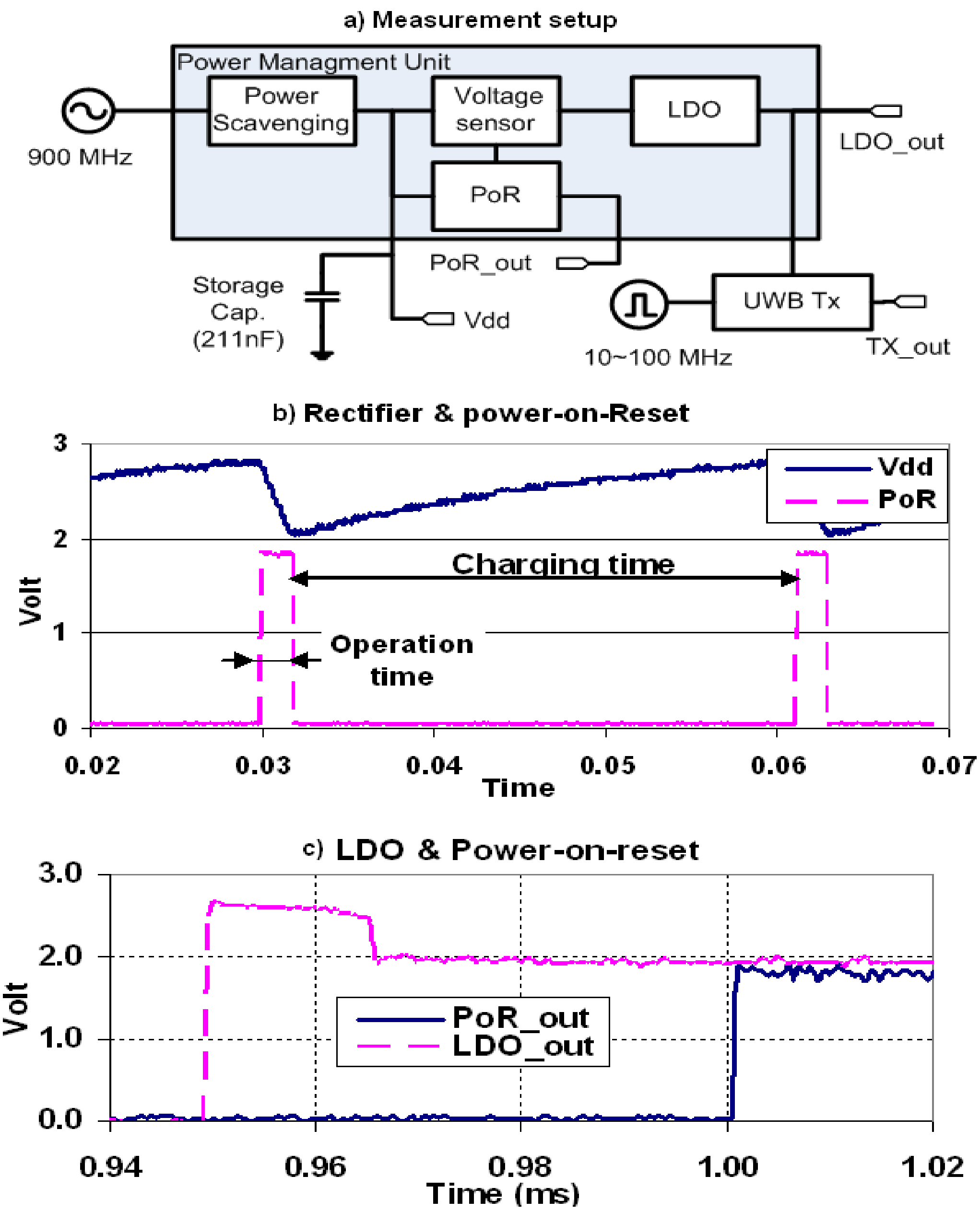


Fig. 4: (a) measurement setup, and measurement results: (b) output voltage measured at rectifier and power-on-reset, (c) output voltage at LDO regulator and PoR,

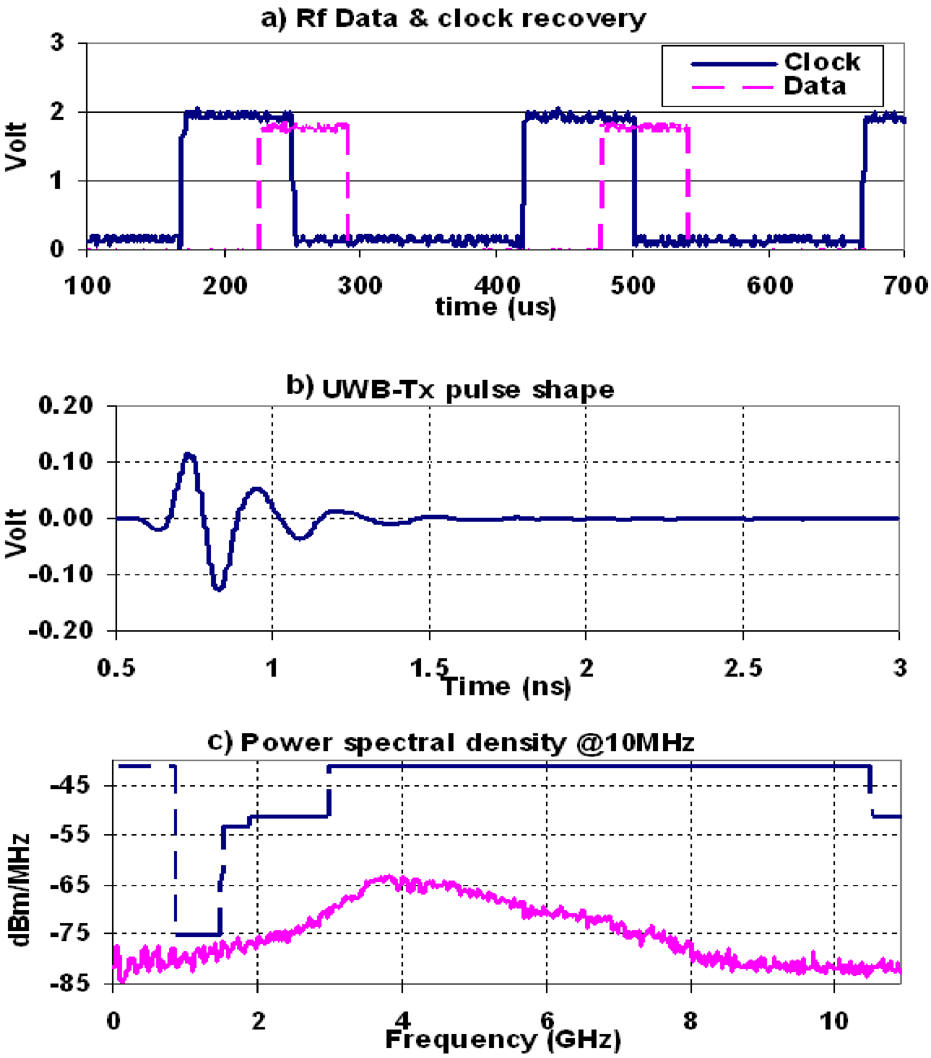


Fig. 5: Measurement results: (a) data & clock recovery, (b) UWB transmitter pulse, and (c) power spectral density at 10 MHz pulse rate.

	This work	[3]	[6]
Technology	0.18µm	0.18µm	0.13 µm
Die area	4.5mm^2 (active area 1	2.7 (active 0.75)	0.55 mm^2
<u>Downlink</u>	900MHz ISM band	13.56 MHz	900MHz ISM band
Data rate	40-160 kb/s	106 kb/s	40-160 kb/s
<u>Uplink</u>	UWB 3.1-10.6Ghz	HF, Load	UHF, backscatter
Pulse rate	10 MHz~100MHz	-	-
Data rate	Up to 10Mbps	3.4 Mb/s	40-640 kb/s
<u>UWB transmitter</u>		-	-
Pulse amplitude	220 mV$_{pp}$	-	-
Pulse width	620 ps	-	-
Power consumption 10Mhz	91.8 µW, 9.2 pJ/pulse	-	-
Power consumption 100Mh	918 µW, 9.2 pJ/pulse	-	-
<u>Power scavenging</u>		-	-
Vout	2.75 V	-	1.45 V
Iout	1.5 µA	-	-
Input Sensitivity	-18.5 dBm(14.1µW)	-	-14 dBm (39.8µW)
Typical Distance	13.9 meters (@4W EIRP)	10 cm	7 meters

Fig. 6: Performance summary of this work in comparison with passive UHF tag [6] and high data-rate HF tag [3]

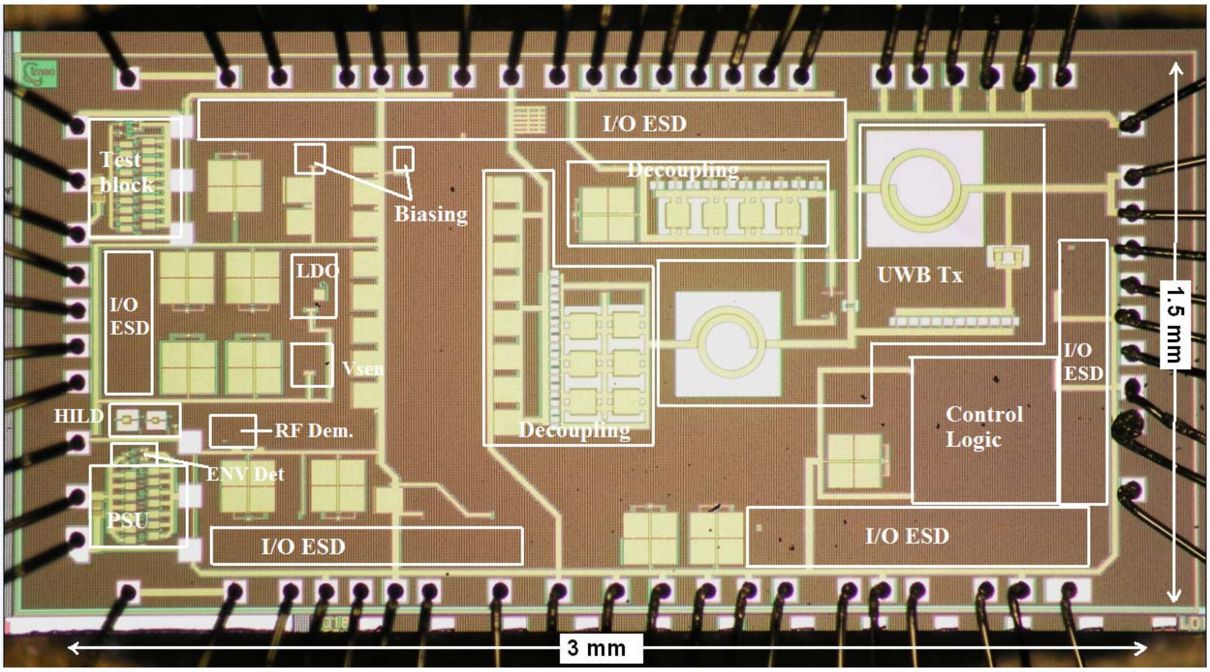


Fig. 7: Chip micrograph of the tag