A 2.45-GHz 0.13- μm CMOS PA With Parallel Amplification

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Abstract—In this paper, a fully integrated 0.13- μm CMOS RF power amplifier for Bluetooth is presented. Four differential amplifiers are placed on a single chip and their outputs are combined with an on-chip LC balun structure. This technique allows to have a low impedance transformation ratio for each individual amplifier, and thus a lower power loss. The amplifier achieves a measured output power of 23 dBm at a supply voltage of 1.5 V and a drain efficiency of 35% and a global efficiency of 29%. The parallel amplification topology allows to efficiently control the output power which results in an efficiency improvement when the output power is reduced.

Index Terms—CMOS, power amplifiers, power combining, power control.

I. INTRODUCTION

IN RECENT years, CMOS RF power amplifiers have proven their ability to efficiently amplify constant envelope RF signals ([1]–[4]). Today, linearization techniques and efficient power control have become the next issues on the road towards fully integrated CMOS transceivers ([5]–[7]). In addition, the evolution towards complex modulation schemes and multi-carrier based systems, resulting in high crest factors and severe power control accuracy, has a serious impact on the design of CMOS RF power amplifiers.

On the other hand, CMOS technology scaling has enabled the use of predistortion, digital correction and automatic calibration at a fairly low cost in terms of silicon area and power consumption [8], [9]. This in turn makes it possible to develop and implement complex linearization techniques. CMOS technology scaling also means a decreasing supply voltage and consequently a lower output power. To achieve sufficient output power in a low voltage technology, an impedance transformation network is required to convert the 50 Ω antenna impedance, R_L , to a much lower transformed impedance, R_t , seen by the amplifier. The impedance transformation ratio r is generally used to indicate the amount of transformation and is defined as

$$r = \frac{R_L}{R_t}. \quad (1)$$

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If the supply voltage is reduced by a factor of two, the transformed antenna impedance should be made four times smaller and the transformation ratio r should be made four times as large to achieve the same output power. One of the most common networks for impedance transformation are the so-called L-match and Π -match networks. Although these networks excel in simplicity and thus can be fully integrated, their power loss is rather high, especially for a high impedance transformation ratio [10]. This implies that at a low supply voltage, and thus for a large impedance transformation ratio, a large amount of power is wasted in the impedance transformation network itself.

This problem can be solved by using several power amplifiers in parallel, and combining their outputs into one single-ended output. This approach was first demonstrated in CMOS by Shirvani *et al.* [5]. The presented solution uses three power amplifiers and three external transmission lines to combine the outputs. Another important property of this topology is the power control ability. When a lower output power is required, one or more branches can be disabled which allows a discrete form of power control. The only drawback is the requirement of the external transmission lines. Another power combining technique was introduced by Aoki *et al.* [10]. It uses a transformer to combine several amplifiers in series to achieve a Watt-level output power.

Finally, CMOS power amplifiers are often implemented as differential amplifiers. This will reduce the required on-chip decoupling capacitance and will make the topology less sensitive to variation in the packaging. However, as most antenna filters and antenna switches are still single-ended, such a topology still requires a differential to single-ended conversion at the output of the power amplifier.

To summarize, it is beneficial to have a differential power amplifier topology, but the output should be single-ended. Also, the impedance transformation ratio should be kept low to avoid excessive power dissipation, but the amplifier should achieve sufficient output power at a low supply voltage. Furthermore, the power amplifier should have some means to regulate or control the transmitted power in an efficient way. And finally, the amplifier should be fully integrated in CMOS. In this paper, a parallel topology, based on a lattice-type LC balun, is developed in order to meet all these requirements [11]. The next section will first discuss the basic LC balun and the associated benefits regarding its use with a CMOS RF power amplifier. Section III will clarify the developed topology. An implementation of this topology, including measurement results, is given in Section IV. Final conclusions are drawn in Section V.

Fig. 1. LC balun connected to a differential power amplifier.

II. LATTICE-TYPE LC BALUN

To combine the outputs of two differential power amplifiers into a single-ended output and to perform the impedance transformation simultaneously, an LC balun, as shown in Fig. 1, is often used [12], [13]. This network was originally used in 1932 as an antenna balun to convert a balanced antenna, like a dipole or loop antenna, to an unbalanced transmission line, such as a coaxial cable [14]. In this paper, the LC balun will be used to combine the outputs of several power amplifiers to one single-ended output. We will first examine the LC balun itself. Section III will discuss the proposed topology, which consists of several baluns placed in parallel.

A. Basic Equations

Besides the conversion from differential to single-ended, the LC balun also performs an impedance transformation, needed to increase the output power of a power amplifier. Referring to Fig. 1, assume that

$$B = \omega L_m = \frac{1}{\omega C_m}. \quad (2)$$

If two ideal differential voltage sources are driving the LC balun of Fig. 1, the following current equations can be derived:

$$I_1 = \frac{+V_{PA} - V_{out}}{+jB} \quad (3)$$

$$I_2 = \frac{-V_{PA} - V_{out}}{-jB}. \quad (4)$$

From these equations, the output voltage is obtained as

$$V_{out} = (I_1 + I_2) \cdot R_L = \frac{2}{j} \cdot V_{PA} \cdot \frac{R_L}{B}. \quad (5)$$

The input admittances $Y_{in,L}$ and $Y_{in,C}$ are now derived as

$$Y_{in,L} = \frac{1}{Z_{in,L}} = \frac{1}{-jB} + \frac{I_1}{V_{PA}} \quad (6)$$

$$Y_{in,C} = \frac{1}{Z_{in,C}} = \frac{1}{+jB} + \frac{I_2}{-V_{PA}}. \quad (7)$$

Fig. 2. LC balun including the power loss of the inductors.

Substituting (3), (4), and (5) in (6) and (7), one can see that the input impedance becomes purely resistive and equal to

$$Z_{in,C} = Z_{in,L} = R_t = \frac{R_L}{2} \cdot \left(\frac{B}{R_L} \right)^2. \quad (8)$$

Decreasing the ratio (B/R_L) will thus reduce the impedance seen by the power amplifier. More power will then flow into the LC balun and if the latter is assumed to be lossless, the output power will also increase.

Assuming that V_{PA} is the RMS voltage at the output of each power amplifier, the output power is obtained as

$$P_{out} = 4 \cdot \frac{V_{PA}^2}{R_L} \cdot \left(\frac{R_L}{B} \right)^2 \quad (9)$$

and can be increased by selecting a higher ratio (R_L/B) , which is equivalent to a decrease of R_t .

Finally, the impedance transformation ratio r is given by

$$r = 2 \cdot \left(\frac{R_L}{B} \right)^2. \quad (10)$$

B. Efficiency of the LC Balun

The LC balun will exhibit some power loss and one can define the efficiency of an impedance transformation network as

$$\eta_m = \frac{P_{out}}{P_t}. \quad (11)$$

with P_t the total power flowing into the impedance transformation network. In CMOS, this efficiency will be dominated by the relative low quality factor of the matching inductor L_m . The quality factor of the capacitor C_m will always be higher and will only have a minor effect on the efficiency. At a specific frequency, the loss of inductor L_m can be modeled as a series resistance R_{Lm} , as shown in Fig. 2. The inductor quality factor is then defined as

$$Q_{Lm} = \frac{\omega L_m}{R_{Lm}}. \quad (12)$$

Likewise, the loss of capacitor C_m can also be modeled as a resistance placed in parallel with C_m , but this loss can be neglected in most cases.

Fig. 3. Efficiency versus power enhancement ratio. The solid line is the LC balun network, the dotted line is the L-match network. (a) $Q_{ind} = 5$. (b) $Q_{ind} = 10$. (c) $Q_{ind} = 15$. (d) $Q_{ind} = 20$.

In general, the efficiency of an impedance transformation network is dependent on the impedance ratio r . It can be seen from (8) that the input impedance is proportional to L_m^2 whereas according to (12), the loss resistance is proportional to L_m for a given Q_{Lm} . A high impedance transformation ratio therefore results in a low power efficiency of the transformation network [10]. Furthermore, a low efficiency means that less power than intended reaches the output, and the impedance transformation ratio should be made even higher to achieve a specific output power.

A better figure to indicate the performance of the impedance transformation network is the *Power Enhancement Ratio*, E , defined by Aoki *et al.* [10], [15]. It takes the loss of the impedance transformation network into account, and is defined as the ratio of the RF power delivered to the load with the lossy transformation network in place, P_{out} , to the power delivered to the load if this load is directly connected to the power amplifier, $P_{out,0}$.

$$E = \frac{P_{out}}{P_{out,0}} = \frac{P_{out,0} \cdot r \cdot \eta}{P_{out,0}} = r \cdot \eta. \quad (13)$$

To calculate the efficiency and power enhancement ratio of the LC balun, first a value for the impedance transformation ratio is chosen. From this, L_m and C_m are obtained from (2). The

power dissipation, for a given inductor quality factor, can then be calculated as

$$P_{diss} = R_{Lm} \cdot I_1^2 + R_{Lm} \cdot I_4^2 \quad (14)$$

From this, the efficiency of the impedance transformation network can be calculated. Finally, the power enhancement ratio E can be obtained from (13).

Fig. 3 shows the calculated efficiency of the LC balun versus the power enhancement ratio E for four different values of the inductor quality factor. As a comparison, the efficiency of a single L-match network is also shown on these figures. Clearly, the LC balun outperforms the L-match network for a power enhancement ratio higher than 2. This can be understood from the fact that the LC balun, for approximately the same component values as the L-match network, always has a power enhancement that is two times higher.

III. PROPOSED PARALLEL AMPLIFICATION TOPOLOGY

The performance of the LC balun can be improved by placing multiple LC baluns in parallel. This will increase the efficiency for a given power enhancement ratio and enables a discrete form of power control. Both effects are now discussed in greater detail.

Fig. 4. Parallel amplification topology, consisting of N sections.

A. Basic Equations

Fig. 4 depicts the proposed topology with multiple LC baluns placed in parallel. Using the same approach as in Section II-A, and again assuming that all sections are driven by ideal differential voltage sources, the transformed load impedance, seen by each power amplifier, now equals

$$Z_{in,C} = Z_{in,L} = R_t = \frac{R_L}{2} \cdot \frac{1}{N} \cdot \left(\frac{B}{R_L} \right)^2 \quad (15)$$

with N the number of parallel section. This topology thus consists of $2 \cdot N$ amplifiers and two differential amplifiers are needed for one section. As before, decreasing the ratio (B/R_L) will reduce the impedance seen by each of the power amplifiers. Yet another means to decrease the transformed impedance, as clearly visible from (15), is by increasing the number of parallel sections N .

Fig. 5. Efficiency versus power enhancement ratio for an inductor quality factor of 10. Four different values of N are used (1, 2, 4, and 8). The arrow indicates the direction of a higher N .

The total output power, i.e., the power dissipated in R_L , is equal to

$$P_{out} = 4 \cdot N^2 \cdot \frac{V_{PA}^2}{R_L} \cdot \left(\frac{R_L}{B} \right)^2 \quad (16)$$

and the impedance transformation ratio for each individual power amplifier becomes

$$r = \frac{R_L}{R_t} = 2 \cdot N \cdot \left(\frac{R_L}{B} \right)^2. \quad (17)$$

B. Efficiency of the Multi-Section LC Balun

As before, the efficiency of the proposed topology will depend on the impedance transformation ratio of each section. In this regard, one should realize that the ratio R_L/B has a quadratic effect on both the output power and the impedance transformation ratio r . On the other hand, the number of parallel sections N has the same quadratic effect on the output power, but it only has a linear effect on the impedance transformation ratio. As such, increasing the number of sections will quadratically increase the output power, and it will only linearly increase the impedance transformation ratio r of each section. Since the efficiency of each section depends on the impedance transformation ratio, increasing the number of parallel sections will allow to achieve a high output power with a relative low impedance transformation ratio for each section, and thus a high efficiency.

To demonstrate this effect, Fig. 5 depicts the efficiency versus power enhancement ratio E for 1, 2, 4, and 8 sections in parallel and an inductor quality factor of 10. Clearly, a higher number of parallel sections increases the efficiency, since each individual section then has a lower impedance transformation ratio.

C. Merging the LC Balun With a Switching RF PA

The very basic switching RF power amplifier consists of an nMOS switch with a shunt capacitance to ground and a DC-feed inductance. If this type of amplifier is used in conjunction with a LC balun network, two elements can be merged together as

Fig. 6. Merging the LC balun with a switching CMOS PA.

demonstrated by Fig. 6. The parallel capacitor C_m , necessary to create a pure resistive input impedance R_t , is added to the shunt capacitance C_1 . Likewise, the parallel inductor L_m , normally connected to the ground, can be placed in parallel with the DC-feed inductance L_1 . After all, the supply voltage can be considered as an AC ground, if sufficient decoupling is provided. This will reduce the total number of inductors and the required silicon area.

D. Power Control

The proposed parallel amplification topology also enables a discrete form of power control. If the two differential power amplifiers of a specific section are not operational, and their outputs behave as an AC ground, the LC balun of that section becomes a high-impedance parallel LC tank, connected in parallel with the $50\ \Omega$ load. This idea is depicted in Fig. 7, in which the differential amplifiers of Section II are assumed to be inactive and the output of these amplifiers behave as an AC ground. The corresponding section will not contribute to the total output power, N is reduced to $N - 1$ in (16) and because of the high-impedance nature of the parallel LC tank, the corresponding output network will, in the ideal case, not influence the operation of the other amplifiers.

Creating an AC ground at the output of each power amplifier can be achieved in two ways. A first technique is to switch on the RF nMOS transistors M_a and M_b in Fig. 6 by applying a large DC voltage at their gates, and to disconnect the power supply as otherwise excessive DC current would be consumed. The latter can be achieved by inserting a pMOS switch in series with the power supply connection of the amplifiers. This pMOS transistor needs to be large enough to reduce the voltage drop across its drain-source terminals when the amplifier is active. Since power control is a relative low-frequency mechanism, the

Fig. 7. Parallel amplification topology, consisting of N sections, with an inactive section 2.

large gate capacitance of that pMOS transistor only needs to be charged and discharged at a relative low rate. Another approach, described in [5], creates an AC ground at the output of each amplifier by switching off the RF nMOS transistor and by creating a short-circuit between the output of the amplifier and the DC power supply by means of a relative small pMOS transistor across the DC feed inductor L_1 . This approach avoids a DC voltage drop when the amplifier is active, but it requires a dynamic biasing of the bulk of the pMOS switch.

The power control ability will have a positive influence on drain the efficiency of the switching amplifiers. After all, the drain efficiency of a switching amplifier strongly depends on the ratio of the on-resistance of the switch r_{on} to the load resistance

of the power amplifier R_t . An approximated formula is given by [16] and [17].

$$\eta_d \approx \frac{1}{1 + 1.4 \cdot \frac{r_{on}}{R_t}} \quad (18)$$

By deactivating one or more differential power amplifiers, thus decreasing N in (15), the load of the remaining active power amplifiers, R_t , will increase. This in turn increases the drain efficiency of the remaining power amplifiers, according to (18). This effect is actually a discrete form of load pull, and is also related to the efficiency improvement that occurs in the Doherty amplifier [18], [19].

Of course, a power amplifier never stands alone and one or more driver stages need to be added to increase the power gain of the transmitter. CMOS devices have a relative large gate capacitance and as a result, the power consumption of the driver stages becomes relatively large compared to HBT and FET technologies. The global efficiency of the amplifier takes this power consumption into account and is defined as

$$\eta_g = \frac{P_{out}}{P_{DC,PA} + P_{DC,DRV}} \quad (19)$$

with $P_{DC,PA}$ the DC power consumption of the power amplifier stage and $P_{DC,DRV}$ the DC power consumption of the driver stages. Another commonly used definition is the power-added efficiency, defined as

$$PAE = \frac{P_{out} - P_{in}}{P_{DC,PA} + P_{DC,DRV}} \quad (20)$$

with P_{in} the RF input power. If the power gain is large, the power added efficiency and global efficiency are almost equal. Apart from the positive influence on the drain efficiency, the discrete form of power control will have a more pronounced positive effect on the global efficiency, which can be understood as follows. The transmitted output power of a switching or saturated amplifier is commonly regulated by changing the supply voltage. Reducing the supply voltage will quadratically reduce the output power while the switching amplifier still maintains its high drain efficiency. On the other hand, the supply voltage of the driver stages can not be reduced as otherwise the power amplifier will no longer operate as a switching amplifier and the drain efficiency would drastically reduce. As such, the power dissipation of the driver stages will remain constant when the supply voltage is reduced and from (19), this means that the global efficiency will reduce at lower output power. With the presented topology however, one or more power amplifiers can be turned off in order to reduce the output power. In that case, the driver stages of the corresponding sections can be shut down as well. The total power consumed by the driver stages will then reduce and the global efficiency will increase.

Fig. 8 shows an example of this effect. In this figure, eight amplifiers, i.e., four section, are placed in parallel. The DC power consumption of the driver stages is assumed to be one fifth of the peak power dissipation of each individual amplifier and the drain efficiency is assumed to be 100%. The peak output power is achieved when the four sections are all active. When the

Fig. 8. Global efficiency versus output power for 1, 2, 3, and 4 sections in parallel.

supply voltage of all four amplifiers is reduced in that case, the global efficiency strongly decreases as indicated by the bottom dashed line in Fig. 8. However, at lower output power levels one or more sections can be turned off and this will result in a higher global efficiency for the same output power. As such, this topology allows to select the optimum number of parallel sections that gives the best global efficiency for the required output power. This optimal curve is shown by the solid black line in Fig. 8.

E. Multi-Section LC Balun With Non-Identical Sections

Until now, it is assumed that all sections are identical. This is the best approach to distribute the total required output power amongst all sections. If it is the goal to control the output power over a wide range, it is better to implement different sections, each one with a specific impedance transformation ratio. In other words, each section will have a different value of B . To analyze this, the formulas are first rewritten in a more general way for section i .

$$R_{inL,i} = R_{inC,i} = \frac{1}{2} \cdot \frac{B_i}{R_L} \cdot \frac{1}{\left(\sum_{k=1}^N \frac{1}{B_k} \right)} \quad (21)$$

$$V_o = -j2 \cdot V_{PA} \cdot R_L \cdot \sum_{k=1}^N \frac{1}{B_k} \quad (22)$$

$$P_o = 4 \cdot \frac{V_{PA}^2}{R_L} \cdot \left(\sum_{k=1}^N \frac{R_L}{B_k} \right)^2 \quad (23)$$

To achieve the highest accuracy with the least number of stages, a binary scaling can be employed. In that case,

$$\begin{aligned} R_L/B_1 &= \beta \\ R_L/B_2 &= 2\beta \\ R_L/B_4 &= 4\beta \\ &\dots \end{aligned} \quad (24)$$

By turning on and off the sections, the output voltage will behave in a binary manner. Therefore, such a partition can also be seen as an RF digital-to-analog power converter [5].

Fig. 9. Circuit implementation of the Bluetooth PA.

If only the first stage is active, the input impedance, and thus the load impedance of the power amplifiers of the first section, is equal to

$$R_{in,1} = \frac{1}{2} \cdot B_1 \cdot \frac{1}{\beta}. \quad (25)$$

On the other hand, if all stages are active, that impedance becomes

$$R_{in,1} = \frac{1}{2} \cdot B_1 \cdot \frac{1}{7\beta} \quad (26)$$

which is seven times smaller. Clearly, all power amplifiers have to be able to deal with this small load impedance.

IV. DESIGN OF A BLUETOOTH PA

A. Circuit Implementation

The presented parallel amplification structure was used to implement a Bluetooth PA in a 0.13- μm CMOS technology with an f_T of 70 GHz. The goal was to demonstrate that with native 0.13- μm transistors and the power combining network, sufficient output power can be achieved to meet the Class 1 Bluetooth requirements. Therefore, no thick gate oxide transistors or device stacking techniques were used. To achieve the 20 dBm output power specification at 2.45 GHz, four amplifiers are placed in parallel and their outputs are connected by means of two LC baluns. To provide some margin, each amplifier is designed to deliver 60 mW of output power, resulting in a theoretical maximum output power of 240 mW or 23.8 dBm.

For the design of the output stage, a switching topology was chosen that combines the high efficiency of Class E with the high output power capability of Class B. Class E suffers from the high peak drain voltage, especially in deep-submicron CMOS where the breakdown voltage of the MOS devices is the main

limiting factor for PA design. However, compared to Class E, the peak drain voltage of this amplifier is reduced to about 2.5 times V_{DD} which is more favorable for CMOS integration. On the other hand, the conduction angle of this operating class remains 50% to ensure the maximum output power of Class B. Hence, we have denoted this operating regime as *Class BE* [20].

At zero drain current, the nMOS transistor of this technology can safely withstand a drain voltage of 4 V. Assuming a Class BE waveform with a peak drain voltage of 3.5 V, the equivalent load impedance required to have an output power of 60 mW is $R_t = 9.6 \Omega$. In Section III, it was found that

$$R_t = \frac{R_L}{2} \cdot \frac{1}{N} \cdot \left(\frac{B}{R_L} \right)^2. \quad (27)$$

From which B can easily be obtained:

$$B = \sqrt{2 \cdot N \cdot R_L \cdot R_t} \approx 44 \Omega.$$

At a frequency of 2.45 GHz, the corresponding values of L_m and C_m become

$$L_m = B/\omega = 2.86 \text{ nH}$$

$$C_m = 1/(B\omega) = 1.48 \text{ pF}$$

and these values are both easily implemented in CMOS.

The optimum size for the nMOS switches in the Class BE power amplifier, was found to be a gate width of 1000 μm and minimum gate length. Making the switch larger would result in a minor increase of the drain efficiency η_d , but it would also increase the driver power $P_{DC,DRV}$ and hence the global efficiency η_g would be reduced.

Fig. 9 shows the complete circuit of the PA. To turn off a specific section, the gate voltage is tied to V_{DD} and the supply voltage is disconnected by means of an external switch.

Fig. 10. Micrograph of the fully integrated CMOS Bluetooth PA.

TABLE I
COMPONENT VALUES OF THE INTEGRATED CMOS PA

component	value	component	value
L_{1a}	1.3 nH	L_{1b}	0.9 nH
C_{1a}	1.2 pF	C_{1b}	1.1 pF
L_m	3.1 nH	C_m	0.8 pF
C_{BL}	10 pF		

As pointed out before, and referring again to Fig. 6, inductor L_m and capacitor C_m , connected between each input of the LC balun and ground, are completely absorbed into the Class BE power amplifier. As such, less passive components are needed. The consequence is that the components of the two branches of the differential Class BE amplifier are no longer identical, i.e., $C_{1a} > C_{1b}$ and $L_{1a} > L_{1b}$. Furthermore, the outputs of the four RF amplifiers need to be combined which results in long and non-equal interconnect lines that introduce parasitics. These interconnect parasitics are also included in the design and are modeled as lumped transmission lines. The non-symmetric parasitics, together with the existing imbalance (i.e., $C_{1a} > C_{1b}$, $L_{1a} > L_{1b}$ and the different higher harmonic behavior of the two branches of each LC balun) requires a re-tuning of the Class BE amplifier in order to achieve a symmetrical waveform at each output. A numerical optimizer was used to achieve this. The final component values are summarized in Table I.

The RF driver stages are digital inverters, operating at the nominal supply voltage of 1.2 V. The main reason for this choice was the smaller required silicon area. The drawback is the increased DC power consumption, since the gate capacitance of the output transistor is not tuned by an inductor. The input power is only -6 dBm which enables a direct connection of the up-conversion mixers to the first RF driver stage. All the inductors

and capacitors of Fig. 9 are integrated on-chip and no external matching or tuning is necessary.

B. Layout

Fig. 10 shows a photograph of the fully integrated RF amplifier. The size of the chip is 2.74 mm by 2.00 mm. A reduction of the consumed silicon area could be achieved by merging L_{1a} and L_{1b} together in one single inductor. However, since $L_{1a} > L_{1b}$, this would require an inductor with a non-centered common tap.

At 2.45 GHz, the value of L_m is still relatively large. Therefore, this topology is even better suited at higher frequencies, since that would reduce the values of L_m and L_1 and the consumed silicon area. This would also enable to place more than four amplifiers in parallel, and to use tuned driver stages without consuming excessive silicon area.

To connect the four outputs, long interconnections are necessary. Underneath the interconnect lines lies a patterned metal ground plane to accurately model the parasitic capacitance, to avoid capacitive signal injection into the substrate and to short-circuit the substrate losses.

Finally, a total value of two times 206 pF is implemented to bypass the supply voltage of the Class BE stage. High-density metal-insulator-metal (MIM) capacitance with a density of 2 fF/ μm^2 is used for this task.

C. Measurements

1) *Output Power and Efficiency:* Fig. 11 shows the measured output power and efficiency at 2.45 GHz versus the supply voltage, for both two and four amplifiers in parallel. With all four amplifiers operating in parallel, a maximum output power of 200 mW or 23 dBm can be achieved at a global efficiency of 28%. The corresponding drain efficiency of the amplifier is 34% and the driver stages consume 118 mW. The latter number

Fig. 11. Measured output power, drain efficiency (η_d) and global efficiency (η_g) versus supply voltage for (a) two sections and (b) one section.

Fig. 12. Efficiency improvement: (a) global efficiency versus output power and (b) power dissipation versus output power.

could be reduced if tuned driver stages were used, but it would drastically increase the chip area. Notice the reduction of the global efficiency η_g for lower output power, which is due to the constant dissipation in the switching driver stages.

Fig. 11 also shows the measurement when only one section or two amplifiers are activated. If N is reduced from 2 to 1, the output power should drop by 6 dB if the supply voltage is kept constant. In this case, the peak output power is 60 mW or 17.8 dBm, which is close to the theoretical difference of 6 dB. For two amplifiers, the maximum global efficiency is 21% at 50 mW and the corresponding drain efficiency is 27%. The power dissipation in the driver stage is divided by 2, resulting in a consumption of 59 mW. When only one section is used, the dissipation of the driver stage is divided by 2, which results in an increase of the global efficiency at lower power levels. This mechanism is clearly indicated on Fig. 12(a). At a power level of 17 dBm and below, it is beneficial to use only one section or two power amplifiers. To further demonstrate the benefit to switch off one section at lower power levels, Fig. 12(b) shows the measured power dissipation of the entire amplifier, including the driver stages.

In Fig. 13, the output power, drain efficiency and global efficiency versus frequency is given for both one and two sections

TABLE II
MEASURED CONSTANT ENVELOPE PERFORMANCE SUMMARY

parameter	measured performance	
	2 sections - 4 PAs	1 section - 2 PAs
maximum output power	200 mW - 23 dBm	60 mW - 18 dBm
maximum drain efficiency	42 %	32 %
maximum global efficiency	29 %	21 %
input power	-6 dBm	-6 dBm
driver stage power consumption	118 mW	59 mW

working at a supply voltage of 1.1 V. With two sections operating at 1.1 V, an output power of 20 dBm can be achieved with a drain efficiency of 39% and a global efficiency of 28%. With only one section at 1.1 V, an output power of 15 dBm with 30% drain efficiency and 20% global efficiency can be achieved. Table II summarizes the power and efficiency measurements.

2) *Bluetooth Measurements*: Fig. 14 shows the measured Bluetooth output spectrum at the maximum output power of 23 dBm and an input power of -6 dBm. At ± 500 kHz frequency offset, the transmitted power is -22.1 dBc and -21.25 dBc,

Fig. 13. Measured output power ($\circ$), drain efficiency ($\square$) and global efficiency ($\diamond$) versus frequency at a supply voltage of 1.1 V for (a) two sections and (b) one section.

Fig. 14. Measured Bluetooth output spectrum at maximum output power.

TABLE III
MEASURED BLUETOOTH PERFORMANCE SUMMARY

parameter	measured performance	Bluetooth specification
spectral mask	-22.1 dBc and -21.25 dBc	-20 dBc
ACP at channel offset 2	-46 dBm	-20 dBm
ACP at channel offset 3	-47 dBm	-40 dBm

which is compliant with the -20 dBc specifications. The adjacent channel power is obtained by integrating the power density over a bandwidth of 1 MHz. The measured adjacent channel power is -46 dBm for a channel offset of two and -47 dBm for a channel offset of three, surpassing the Bluetooth specifications of -20 dBm and -40 dBm adjacent channel power. Table III summarizes the Bluetooth measurements.

It should be noted that the $+20$ dBm Bluetooth specification requires more than two power control steps. However, the presented topology can easily be extended to have more discrete power levels. Furthermore, this architecture can also be combined with a dynamic power supply technique, although such a

TABLE IV
COMPARISON WITH OTHER BLUETOOTH POWER AMPLIFIERS

Reference	Technology	P_{out} [dBm]	P_{in} [dBm]	G_P [dB]	η_d [%]	PAE [%]	V_{DD} [V]	fully integrated	differential	single-ended output
[21]	0.25 μ m CMOS	24.0	+2	22	—	48	2.5			v
[22]	0.18 μ m CMOS	23.0	-7	30	—	45	2.4			v
[24]	0.25 μ m CMOS	21.4	-8.6	30	38	26	2.6	v	v	
[23]	0.35 μ m CMOS	23.0	—	—	—	37	1.5		v	
[25]	SiGe	23.0	0	23	—	35	3			v
[26]	GaAs HBT	23.5	0	23	—	41	3.6			v
[27]	InGaP HBT	23.0	+3	20	—	50	3.2			v
this work	0.13 μ m CMOS	23.0	-6	29	35	29	1.5	v	v	v

solution would be less efficient, given the fixed DC power consumption of the driver stages.

D. Comparison With Other Work

A comparison between this Bluetooth power amplifier and other solutions is shown in Table IV. This table contains four published Bluetooth CMOS power amplifiers and three commercially available Bluetooth amplifiers in a SiGe, GaAs, and an InGaP technology.

The presented work is the only Bluetooth power amplifier that is fully integrated and has a single-ended output. It also works at the lowest supply voltage and is able to efficiently control its output power. One can also notice that the use of external striplines and external matching networks results in an increased efficiency compared to the two fully integrated designs. The efficiencies of the CMOS solutions in [21]–[23] are comparable or even better than the more expensive technology solutions. In other words, CMOS transistors can do the job.

The power combining technique of this work is actually able to outperform the global efficiency of the SiGe and GaAs solutions at a lower output power level. This is shown in Table V. For example at an output power level of 15 dBm, the presented topology has the benefit that it can make a change from two to

TABLE V
COMPARISON WITH OTHER BLUETOOTH POWER AMPLIFIERS: GLOBAL
EFFICIENCY AT LOWER OUTPUT POWER

Reference	Technology	P_{out} [dBm]							
		5	7	10	12	15	17	20	23
[25]	SiGe	4%	5%	7%	9%	13%	20%	25%	35%
[26]	GaAs HBT	3%	3%	6%	9%	14%	17%	25%	41%
[27]	InGaP HBT	—	10%	—	20%	—	32%	—	50%
this work	0.13 μm CMOS								
	two sections	(3%)	(4%)	(7%)	(10%)	(17%)	(20%)	27%	29%
	one section	5%	7%	11%	15%	20%	21%	-	-

one power amplifier. In that case, the global efficiency of this implementation is higher compared to the SiGe and GaAs implementations, whose output power is regulated by changing the bias settings of the PA. It should be noted that the presented CMOS amplifier only allows a two-level power control, and that the different power levels for this implementation in Table V assume an efficient voltage regulator (except for two discrete power levels). Nevertheless, this topology can be extended to supply more discrete output power levels.

V. CONCLUSION

In this paper, the architecture, design and implementation of a Bluetooth power amplifier, implemented in a 0.13- μm CMOS technology, was discussed. The amplifier is based on a parallel amplification topology composed of multiple LC balun networks that combine the output of four power amplifiers into one single-ended output. This allows to reduce the impedance transformation ratio of each LC balun network, which in turn results in a lower power dissipation. This power combining technique also allows to control the output power in a power efficient way and requires no expensive off-chip components.

A measured output power of 23 dBm at 2.45 GHz is achieved by using the four amplifiers in parallel, which surpasses the 20 dBm requirement of Bluetooth. The measurement results of the amplifier clearly indicate the efficiency improvement that can be achieved with this topology. The Bluetooth spectral mask and adjacent channel power requirements are met as well.

In comparison with other power amplifiers, this amplifier is the only fully integrated CMOS differential power amplifier with a single-ended output. It achieves 23 dBm of output power at the lowest power supply. Compared to more expensive technologies, this solution achieves a higher efficiency when the output power is reduced.

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