29.6 A 660-to-676GHz 4x2 Oscillator-Radiator Array with Intrinsic Frequency-Filtering Feedback for Harmonic Power Boost Achieving 7.4dBm EIRP in 40nm CMOS

Gabriel Guimaraes, Patrick Reynaert

KU Leuven, Leuven, Belgium

The THz region of the electromagnetic spectrum is gaining interest due to its unique spectroscopic properties that make it useful for gas detection, biological imaging and accurate timekeeping. While several techniques allowed these applications to be explored in the lower region of the THz spectrum, effective power generation at frequencies above 500GHz is still a challenge in CMOS. However, maximum gas absorption for rotational spectroscopy occurs at this range, and at even higher frequencies gas vibrational modes can be detected [6], making such frequency sources attractive for current and future applications.

As fundamental oscillation is not possible above the transistor f_{max} , THz sources have to multiply the frequency of an external or an on-chip mmWave oscillator. For the same resulting frequency, a combination of different fundamental frequencies and multiplication numbers can be used. However, as the fundamental frequency rises, oscillation becomes increasingly difficult and with reduced amplitude. Furthermore, the amount of power generated by transistor non-linearity drops sharply with harmonic number N and voltage swing. This creates a tight constraint in silicon for the available power in the mid-THz range. To achieve high power in this case requires providing the transistor with proper impedances, high isolation between drain and gate at the harmonic frequency to prevent self-loading, and to combine the output of many sources coherently. Previous work such as the ones in [2] and [3] uses even harmonic numbers such that the radiated signal is in common mode while the fundamental is in differential mode to achieve some of these conditions. In the case of a 2nd harmonic source this severely limits the maximum achievable frequency while in the case of 4th harmonic this limits the attainable power, requiring large number of array cells and DC power consumption even in high- f_{max} technologies.

To address the trade-off between achievable frequency and output power in a scalable array we propose a new oscillator-radiator cell topology with frequency filtering feedback that works on the $N=3$ harmonic number (Fig. 1). A $N/4$ resonator is used as tank as it also intrinsically provides a high-impedance resonance at three times the fundamental frequency at $3N/4$. In previous art, this resonance does not coincide with the output harmonic number and is therefore dampened by the lossy transistor gate, resulting in a single-resonance tank that does not increase harmonic power generation. Differently than in those works, frequency filtering is built into the proposed feedback transmission-line network of this circuit to provide isolation between gate and drain and enable a high-Q resonance at the 3rd harmonic. The multi-resonant tank boosts harmonic power generation and improves the phase-noise performance of the oscillator. The proposed topology only relies on coupling between neighboring cells, avoiding signal distribution constraints and the use of additional oscillators for coupling as presented in [1] and [2], and is easily scalable to even larger array sizes.

The unit-cell layout is shown in Fig. 2 along with part of adjacent cells. It oscillates at 223GHz with 3rd harmonic radiation at 670GHz. A virtual PEC represents differential-mode cell coupling while a virtual PMC represents common-mode cell coupling. The standing-wave patterns at the slotlines are also exhibited. The wide slot in the middle of the cell is part of the feedback path and only propagates differential signals, preventing common-mode oscillations [2]. This slot couples to the microstrip at a virtual-ground on the 3rd harmonic frequency (Fig. 1) creating the filtering network along with the folded slot at the bottom. The drain-to-gate voltage gain is presented in Fig. 2. At 223GHz, the gain is 8.5dB while at 670GHz it is -10.4 dB, validating that the filtering network provides additional isolation at the 3rd harmonic to avoid gate loading and signal loss. The full array architecture is depicted in Fig. 3. A wall is implemented using all metals layers of the technology on the boundary of the array to mimic the presence of additional cells so that the edge oscillators have the same free-running frequency as the ones in the center, and thus facilitating locking. The array cells are coupled by either shorted slotlines or shared slotlines in the tank. The shorted lines forces the signal to be in-phase such that no current flows through the short. The shared slots only propagate signals in differential-mode, presenting an open in common-mode [3] (Fig. 3).

The mechanism of radiation is better understood from looking at the slot configuration of the whole array as depicted in Fig. 3. The front-facing common-mode coupled cells complement each other forming a linear array of slotline antennas. These 5 antennas have $\lambda/2$ length and are spaced by $\lambda/2$ at 670GHz. The short length and small spacing at the fundamental contributes to suppressing its radiation. Additionally the wide feedback slots act as parasitic antennas at the 3rd harmonic with $\lambda/4$ length. This affects the total radiation pattern of the array and increases the directivity further at the desired frequency.

The chip radiates down into the substrate (through its back) where a high resistivity silicon lens is attached to prevent the build-up of substrate modes and to couple the signal to free-space. The shape of the hyper-hemispherical lens is optimized for the aplanatic case where it provides simulated directivity of 24.7dBi and low aberration, which makes the source easy to integrate into quasi-optical applications.

The design was implemented in a 40nm CMOS technology. The chip micrograph can be seen in Fig. 7. The chip consists of a 4x2 oscillator-radiator array and it is assembled on top of a high-resistivity silicon substrate and lens. To measure the performance, the radiated signal is received by a WR1.5 antenna in the far field (>200mm) and down-converted by a VDI WR1.5SAX for spectrum analysis. The conversion loss of the extender is calibrated with the use of a VDI WR1.5SGX whose power was measured by an Erickson PM5 power meter. The power, frequency and 3rd harmonic phase-noise measurement setup is shown in Fig. 4. The presence of a single tone in the measured spectrum confirms that the oscillators are locked to each other. The frequency tuning and EIRP characteristics are also shown in Fig. 4. The frequency of the source can be tuned from 662.5GHz to 676.6GHz with gate bias alone. The frequency range can go down to 660.8GHz by tuning the power supply. The maximum EIRP is 7.4dBm at 670GHz while consuming 99.7mW DC power. On Fig. 4 the E and H planes radiation patterns are shown. The measured directivity is 23.5dBi which indicates a total radiated power of -16.1dBm. The phase noise was characterized at both the fundamental frequency and 3rd harmonic to confirm the 20log3 (9.5dB) difference between them (Fig. 5). For the fundamental tone (223GHz) the phase noise at 1MHz and 10MHz offset are -76dBc/Hz and -102dBc/Hz respectively while at the 3rd harmonic (670GHz) the measured values are -69dBc/Hz and -93dBc/Hz for the same offsets. The phase noise performance over frequency is also depicted in Fig. 5.

In Fig. 6 this work is benchmarked against the state-of-the-art of silicon-based THz sources. The reported design is the highest frequency CMOS oscillator-based signal source with an output frequency of 660.8-676.6GHz. The EIRP is also one of the best of the compared CMOS sources and similar to SiGe sources. Furthermore, the chip achieves state-of-the-art out-of-band phase noise performance even when compared to lower frequency counterparts like [4] and [5]. In summary, by using the proposed technique of boosting the tank harmonic resonance through a frequency-filtering feedback network, this work advances the current state-of-the-art of THz CMOS sources to a frequency range above 650GHz.

References:

- [1] - K. Guo, Y. Zhang and P. Reynaert, "A 0.53-THz Subharmonic Injection-Locked Phased Array With 63- uW Radiated Power in 40-nm CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 54, no. 2, pp. 380-391, Feb. 2019.
- [2] - R. Han et al., "25.5 A 320GHz phase-locked transmitter with 3.3mW radiated power and 22.5dBm EIRP for heterodyne THz imaging systems," 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, San Francisco, CA, 2015, pp. 1-3.
- [3] - Z. Hu, M. Kaynak and R. Han, "High-Power Radiation at 1 THz in Silicon: A Fully Scalable Array Using a Multi-Functional Radiating Mesh Structure," in *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1313-1327, May 2018.
- [4] - Y. Zhao et al., "2.1 An integrated 0.56THz frequency synthesizer with 21GHz locking range and -74dBc/Hz phase noise at 1MHz offset in 65nm CMOS," 2016 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2016, pp. 36-37.
- [5] - C. Jiang, M. Aseeri, A. Cathelin and E. Afshari, "A 301.7-to-331.8GHz source with entirely on-chip feedback loop for frequency stabilization in 0.18 μ m BiCMOS," 2018 IEEE International Solid - State Circuits Conference - (ISSCC), San Francisco, CA, 2018, pp. 372-374.

Figure 29.6.1: Half-circuit schematic of the proposed topology (top) and comparison between features in previous works and this work (bottom).

Figure 29.6.2: Layout of the proposed oscillator-radiator with intrinsic frequency filtering (top-left), E-Field distribution in slotlines (right). The loop-gain inside a half-circuit is plotted demonstrating the isolation between drain and gate at 3rd-harmonic frequency (bottom).

Figure 29.6.3: Array architecture (top-left). Differential and Common-Mode propagation in a shared slot-line (top-right). View of main radiating slots in the array with E-Field magnitude for standing-waves at the third harmonic (Bottom).

Figure 29.6.5: Measured phase-noise at fundamental (top-left) and 3rd-harmonic (top-right). 10MHz offset phase-noise performance throughout the tuning range.

Figure 29.6.4: Measurement setup diagram (top-left). Measured output spectrum with single-tone for coupled array (top-right). Measured EIRP vs frequency performance (bottom-left) and radiation pattern (bottom-right).

	This Work	J5SC2019[1]	J5SC2016[4]	J5SC2014[8]	J5SC2018[5]	J5SC2015[2]	J5SC2018[3]	J5SC2015[7]
Technology (fmax)	40nm CMOS (300GHz)	40nm CMOS (300GHz)	65nm CMOS (280GHz)	65nm CMOS (280GHz)	130nm SiGe BiCMOS (280GHz)	130nm SiGe BiCMOS (280GHz)	130nm SiGe BiCMOS (500GHz)	130nm SiGe BiCMOS (350GHz)
Source Type	4x2 Oscillator Array	1x4 Injection-Locked Oscillator	PLL Oscillator	4x4 Oscillator Array	FLL Oscillator	PLL + 4x4 Oscillator Array	7x6 Oscillator Array	Injection-Locked Oscillator
Frequency (GHz)	660.8-676.6	531.5	538.7-559.9	336-339*	302-332	317	1010	485-511
Phase Noise (dBc/Hz) @100kHz	-69	-98*†	-74	-93	-78.5	-79	—	-87
Phase Noise (dBc/Hz) @500kHz	-93	-105*†	-85	—	-97*	—	—	—
EIRP (dBm)	7.4	2.3	—	17.1	—	22.5	13.1	—
Output Power (dBm)	-16.1 (Radiated)	-12 (Radiated)	-27 (Radiated)	-0.9 (Radiated)	-13.9 (Probed)	5.2 (Radiated)	-10.9 (Radiated)	-16.6 (Probed)
Die Size (mm x mm)	1.15 x 0.75	1.71 x 1.46	1.8 x 1.55	2 x 1.95	1 x 0.85	1.6 x 1.3	1 x 1	0.72 x 0.7 (core)
DC Power (mW)	99.7	260	172	1540	51.7	610	1100	388

* Value estimated from graph

† Phase-Noise from oscillator injection locked to external signal generator

Figure 29.6.6: Performance summary and comparison with CMOS and BiCMOS previously published THz sources.

Figure 29.6.7: Chip photograph.

Figure 29.6.8: Two-step calibration procedure diagram for EIRP measurement (top) and measurement setup for frequency, EIRP and 3rd harmonic phase-noise and radiation pattern (bottom).

Figure 29.6.9: Measured chip frequency and EIRP performance as a function of DC power consumption.

Additional References:

[6] - Townes, Charles H., et al. Microwave spectroscopy. Courier Corporation, 2013. [7] - T. Chi, et al., "A Multi-Phase Sub-Harmonic Injection Locking Technique for Bandwidth Extension in Silicon-Based THz Signal Generation," in IEEE JSSC, vol. 50, no. 8, pp. 1861-1873, Aug. 2015. [8] - Y. Tousi, et al., "A scalable THz 2D phased array with +17dBm of EIRP at 338GHz in 65nm bulk CMOS," , ISSCC, San Francisco, CA, 2014, pp. 258-259