Investigating the Current Collapse Mechanisms of p-GaN Gate HEMTs by Different Passivation Dielectrics

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***Abstract*—In this letter, the dynamic R_{on} degradation mechanisms of the p-GaN gate HEMTs induced by OFF-state stress are investigated with different passivation dielectrics AlON and SiN. The degradation mechanisms are twofold, including V_{TH} shift and surface trapping in the gate-to-drain access region, whose impacts are successfully distinguished. Surface trapping by SiN passivation is evidently proved to be the dominant factor that can almost induce a full current collapse. The V_{TH} positive shift diminishes the drain current by shrinking the overdrive V_{GS}, which however can be compensated by a higher V_{GS} overdrive in applications. SiN passivation can effectively suppress the positive bias temperature instability (PBTI) effect, probably by passivating the p-GaN fast traps with hydrogen during passivation. Last, the transient measurements unveil that both the surface trapping and V_{TH} shift have a very slow recovery process.**

***Index Terms*— p-GaN gate HEMTs, dynamic R_{ON}, V_{TH} shift, surface trapping**

I. Introduction

COMMERCILIATION of the enhancement-mode (e-mode) p-GaN gate HEMTs has been started recently, especially in the field of consumer electronics such as fast chargers [1][2][3][4]. There are mainly two types of e-mode HEMTs available, i.e., Schottky-type p-GaN gate HEMTs [1][2] and hybrid-drain-embedded Gate Injection Transistor (HD-GIT) [3][4]. Reliability issues beyond the JEDEC standard [5] such as current collapse, p-GaN gate failure, V_{TH} shift, etc., have been hampering the wide applications of the GaN power electronic devices.

Current collapse, or dynamic R_{ON} degradation, after high-voltage OFF-state stress has been heavily investigated for a long time. This problem is normally ascribed to several possible reasons including 1) surface trapping in the gate-to-drain access region [6][7], 2) V_{TH} positive shift [8][9][10][11], and 3) buffer trapping [12][13][14].For the Schottky-type p-GaN gate HEMTs, we have previously demonstrated p-GaN gate HEMTs with the current collapse well limited within ±20% by a bi-layer passivation [15][16]. It has also been unveiled that dedicated buffer stack design and surface passivation can effectively suppress the buffer trapping [14] and surface trapping [6].

Although the surface trapping and V_{TH} positive shift have been experimentally confirmed to contribute to the current collapse, their impacts are however difficult to be distinguished. Plus, the impact of passivation on the V_{TH} is seldom reported. In this work, the trapping and de-trapping behaviors will be unambiguously identified on the p-GaN gate HEMTs with different passivation dielectrics. Double-pulsed *I-V* and transient measurements will be conducted to stress and monitor the recovery behavior of the trapping effects.

II. Epitaxy and Fabrication

The p-GaN/AlGaN/GaN structure was epitaxially grown by a metalorganic chemical vapor deposition (MOCVD) on 200 mm p^+-Si substrates. The epi stack comprises an AlN nucleation layer, a superlattice layer, a C:GaN layer, a GaN channel layer, an AlGaN barrier layer, and a Mg-doped p-GaN layer. Detailed processing can be found in [15]. The measured DC and power HEMTs have a gate width W_G of 100 μm and 36 mm, respectively. They share the same gate length L_G of 1.5 μm, gate-source distance L_{GS} of 0.75 μm, and gate-drain distance L_{GD} of 16 μm. There are four field plates with lengths of 2, 4, 6, and 8 μm, measured from the gate edge of the drain side. Two wafers were compared with different passivation dielectrics of AlON and SiN on top of the AlGaN barrier layer. The double-pulsed measurements were performed using an Auriga AU4850 pulsed IV/RF characterization system. The DC and transient recovery measurements were performed by Keysight B1505A. The fast sweeping measurements were conducted by Keysight B1530A WGFMU (Waveform Generator/ Fast Measurement Unit).

III. Results and Discussion

Fig. 1 and Fig. 2 show the I_D-V_D output characteristics and I_D-V_G transfer characteristics of the 100-μm DC HEMTs. The SiN-passivated HEMTs feature a low V_{TH} of 1.1 V and a very sharp subthreshold slope, implying the SiN passivation can significantly impact the electrical performance of the p-GaN gate HEMTs. AlON-passivated HEMTs resemble the previous reported devices with a high V_{TH}>3 V and a smoother subthreshold slope, ascribed to the trapping effect in the p-GaN layer [17][18].

This paragraph of the first footnote will contain the date on which you submitted your paper for review. This work was supported in part by the Vlaams Agenschap Innoveren en Ondernemen and the imec.icon research program.

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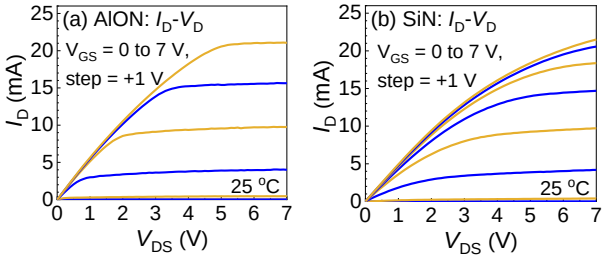

Fig. 1. Output characteristics of the 100-µm (a) AlON-passivated and (b) SiN-passivated HEMTs at 25 ºC.

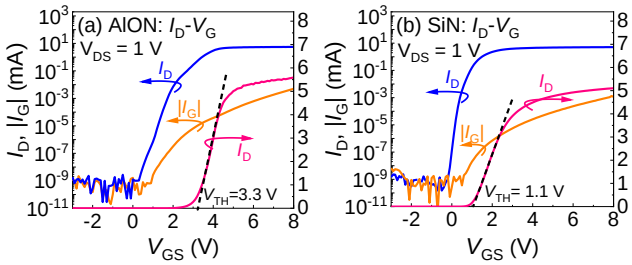

Fig. 2. Transfer characteristics of the 100-µm (a) AlON-passivated and (b) SiN-passivated HEMTs at 25 ºC.

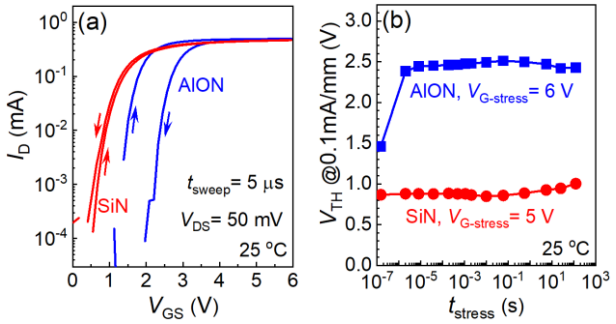

Fig. 3. (a) Double-sweep I_D-V_G curves and (b) V_{TH} evolution during the forward gate voltage stress of the 100-µm AlON-passivated and SiN-passivated HEMTs, by the fast sweeping measurements with an ultra-short I_D-V_G sweep time t_{sweep} of 5 µs.

Fast sweeping I_D-V_G curves by B1530A WGFMU are demonstrated in Fig. 3(a). Strikingly, the hysteresis of the SiN-passivated HEMTs is as small as 70 mV. Further positive bias temperature instability (PBTI) characterization was conducted by stressing the gate by 6 V and 5 V on the AlON-passivated and SiN-passivated HEMTs, respectively. During the characterization, their source terminals were grounded, and the drain terminals were biased at 50 mV. It is shown in Fig. 3(b) that the SiN-passivated HEMTs possess a lower but much more stable V_{TH}. This behavior is probably induced by the hydrogen passivation effect, where the hydrogen is introduced during the SiN deposition. It is worthwhile to mention that only the fast characterization can observe such a significant hysteresis and V_{TH} instability effect on AlON-passivated HEMTs, because of the p-GaN fast trapping and de-trapping characteristics [17].

To characterize the current collapse, the devices were then subjected to double-pulsed I_D-V_D measurements. The waveforms are depicted in Fig. 4(a). In the OFF state, the devices were stressed by (V_{GS_Q}, V_{DS_Q}), followed by a short dead-time of 200 ns. Afterwards, the devices were turned on by the (V_{GS_NQ}, V_{DS_NQ}), thus the drain current can be monitored after each OFF-state stress. It is known that the drain current decrease in the I_D-V_D saturation region and linear region is the signature of V_{TH} shift and trapping in the access region, respectively [19]. Fig. 4(b) and (c) clearly indicate that these two devices both suffer from V_{TH} shifts. However, only the SiN-passivated HEMTs possess a dramatic trapping in the gate-to-drain access region, leading to a significant drain current collapse.

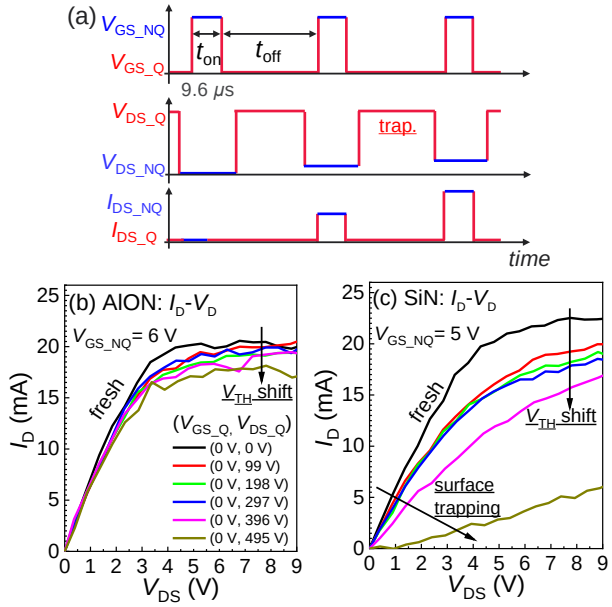

Fig. 4. Double-pulsed I_D-V_D (a) waveforms and I_D-V_D curves for the 100-µm (b) AlON-passivated HEMTs and (c) SiN-passivated HEMTs. The quiescent stressing $V_{DS\text{-}Q}$ is 0, 99, 198, 297, 396, and 495 V.

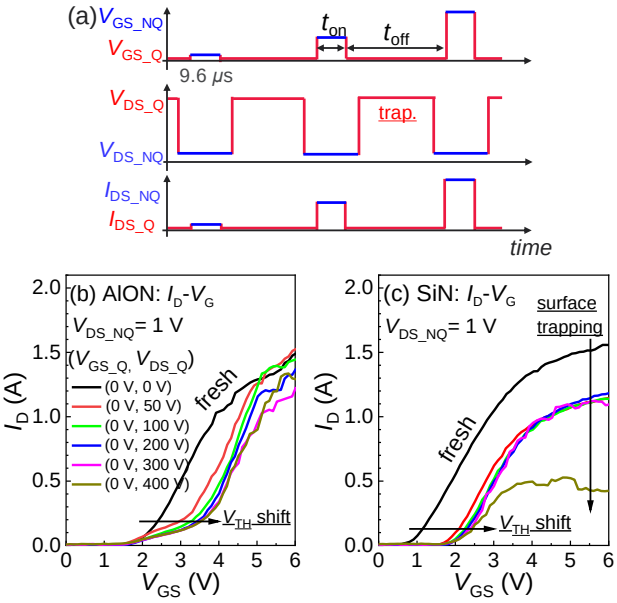

Fig. 5. Double-pulsed I_D-V_G (a) waveforms and I_D-V_G curves for the 36-mm (b) AlON-passivated HEMTs and (c) SiN-passivated HEMTs. The quiescent stressing $V_{DS\text{-}Q}$ is 0, 50, 100, 200, 300, and 400 V.

Double-pulsed I_D-V_G measurements were further performed

as shown in Fig. 5. Both devices show a large V_{TH} shift of more than 1 V. The AlON-passivated HEMTs give an abnormal current bump in the voltage range from 2 to 4 V. This is similar to the results in [17][18], which is possibly induced by trapping under the gate.

Notably, the I_D of the AlON-passivated HEMTs at V_{GS}=6 V under the stress condition of (0 V, 400 V) sees a 20% decrease because of the positive V_{TH} shift. Therefore, a large enough V_{GS} overdrive can effectively compensate the V_{TH} shift, provided the HEMTs are almost free of surface trapping. This can be verified by the fact that the drain current decreases by 30% for V_{GS}=5 V, whereas 68% for V_{GS}=4 V. The SiN-passivated HEMTs demonstrate a definite evidence of surface trapping, especially under the stress condition of (0 V, 400 V), where the drain current decreases by 65%. This is similar to the excessive current collapse reported in literature of the GIT HEMTs under high-voltage stress [20].

It has been shown in Fig. 3(b) that SiN passivation can efficiently suppress the PBTI effect. However, the V_{TH} shift appears again under the OFF-state drain stress. This proves that the OFF-stress-induced V_{TH} shift possesses a different mechanism from that of the gate PBTI. Previous studies have also pointed out that, instead of the p-GaN trapping effect, the trapping taking place in the AlGaN barrier [8] and GaN buffer [9], or p-GaN charging effect [10] are possibly responsible for the OFF-stress-induced V_{TH} shift.

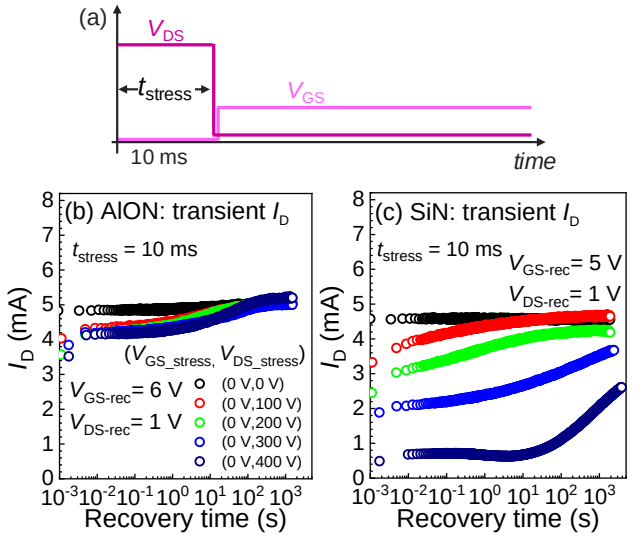

Fig. 6. (a) Stress and sense procedure, and the current transient waveforms of the 100-μm (b) AlON-passivated HEMTs and (c) SiN-passivated HEMTs during the recovery phase. The stress condition is V_{GS}=0 V/ V_{DS}=400 V and the stress time is 10 ms.

To monitor the de-trapping behavior, transient measurements were conducted with a Keysight B1505A. As shown in Fig. 6(a), the HEMTs were first subjected to a 10-ms OFF-state stress, then the stress was released, the HEMTs were switched on and the drain current recovery behavior was recorded. There is around 3-ms transition time between the stress and recovery. The AlON-passivated HEMTs show an almost constant current decrease of 13%, irrespective of the stressing voltages. In contrast, the SiN-passivated HEMTs show a monotonous current decrease with increasing stressing voltages.

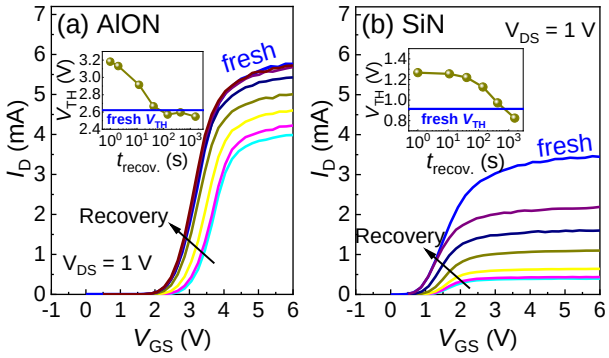

Fig. 7. Transfer I_D-V_G curves of the 100-μm (a) AlON-passivated HEMTs and (b) SiN-passivated HEMTs during the recovery phase. The stress condition is V_{GS}=0 V/ V_{DS}=400 V. The insets show the V_{TH} evolution during the recovery phase.

The recovery process was periodically interrupted by the I_D-V_G sweeps as shown in Fig. 7. For the SiN-passivated HEMTs, the V_{TH} and surface trapping were recovering simultaneously. After 1490 s, the V_{TH} fully recovered, but the surface trapping still existed. For the AlON-passivated HEMTs, the V_{TH} recovery dominated the current recovery process. Due to the limitation of the setup, the transition between the recovery and sweep takes around 1 s, whose impact is however negligible because of the very slow recovery process.

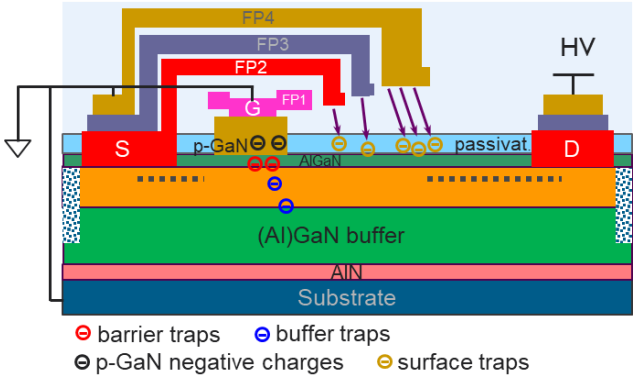

Fig. 8. Schematic cross-section of the p-GaN gate HEMTs with four field plates. Possible trapping occurs in the AlGaN barrier, GaN buffer, and gate-to-drain access region, and negative charging of the p-GaN is depicted as well.

Based on the experiments and comparison above, the possible current collapse mechanisms are depicted in Fig. 8. The surface trapping in the gate-to-drain access region is evidently dominant if the passivation quality is imperfect, which can be efficiently suppressed by using the AlON passivation dielectric, or similarly with Al_2O_3 in our previous work [15]. Another dominant factor of V_{TH} shift possibly stems from the trapping effects in the AlGaN barrier and GaN buffer, or from the p-GaN charging effect due to the charged gate-to-drain capacitance C_{GD}. The V_{TH} shifts induced by the

OFF-state drain-voltage stress and ON-state gate-voltage stress seem different from each other, because the OFF-stress-induced V_{TH} shift has a recovery time constant of around 10 to 100 s (Fig. 7), whereas the PBTI effect time constant is approximately 1 ms [17].

IV. Conclusion

Current collapse caused by V_{TH} shift and trapping in the gate-to-drain access region has been successfully distinguished and confirmed by passivating the p-GaN gate HEMTs with different dielectrics AlON and SiN. The trapping and de-trapping behaviors were comprehensively monitored by various characterization methods such as fast sweeping, double-pulsed I_D-V_D and I_D-V_G, and transient measurements. The V_{TH} shift by OFF-state stress was found to always exist in the Schottky-type p-GaN gate HEMTs, which however can be compensated by a large gate overdrive voltage. The trapping in the access region that induces a severe current collapse was proved to exactly locate in the SiN dielectric. This trapping can induce an almost full current collapse at high OFF-state V_{DS} of 400 V, which can be effectively suppressed by using the high-quality AlON or Al_2O_3 passivation layer. Both the V_{TH} recovery and surface de-trapping processes are very slow. Moreover, SiN passivation was found to be able to efficiently suppress the PBTI effect, probably by passivating the p-GaN fast traps with hydrogen.

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