Integration of 650 V GaN Power ICs on 200 mm Engineered Substrates

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Abstract—GaN power ICs on engineered substrates of Qromis substrate technology (QST®) are promising for future power applications, thanks to the reduced parasitics, thermally matched substrate of poly-AlN, high thermal conductivity, high mechanical yield in combination with thick GaN buffer layers. In this work, we will elaborate in detail on epitaxy, integration, and trench isolation. Electrical characterizations show that the GaN buffer bears a breakdown voltage of > 650 V under the leakage criterion of 10 $\mu\text{A}/\text{mm}^2$ at 150 °C. The fabricated 36 mm power HEMTs with L_{GD} of 16 μm show a high threshold voltage of 3.1 V and a low OFF-state drain leakage of <1 $\mu\text{A}/\text{mm}$ until 650 V. The horizontal trench isolation breakdown voltage exceeds 850 V. The device dispersion is well controlled within 20% over full temperature and bias range. Finally, GaN power ICs on this platform are demonstrated.

Index Terms—GaN, HEMTs, Power ICs, Engineered Substrates

I. INTRODUCTION

ENGINEERED substrates are a promising technology to extend the performance of GaN epitaxy beyond 650 V while maintaining high yield and a good control on wafer bow to process wafers breakage-free in a production environment. Qromis Substrate Technology (QST®) has been a pioneer in this regard and commercially offers 200 mm engineered substrates with SEMI standard thickness capable of sustaining high breakdown voltages (≥ 600 V) [1]. The QST® substrate consists of a polycrystalline ceramic core (poly-AlN), covered by several encapsulation layers, on top of which is a SiO_2 bonding layer and a single crystalline Si layer which serves as the nucleation layer for the MOCVD growth [2].

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Depletion-mode (D-mode) HEMT was first fabricated on 15 μm -thick epitaxial layers on 150 mm QST® [3]. Later, lateral GaN-based p-n junction gated field effect transistor (LJFET) was demonstrated on 200 mm engineering QST® [4]. Recently, Tanaka *et al.* exhibited Schottky barrier diodes (SBD) on GaN-on-QST® with a forward I - V characteristics comparable to that on GaN-on-GaN native substrates [5].

Resembling the work achieved for GaN power ICs on SOI [6], 200 V half-bridge with integrated drivers on GaN-on-QST® has been rolled out for a higher switching speed, better power conversion efficiency, and reduced form factor [7]. Both in the industry [8, 9, 10] and academia [11, 12], GaN power ICs have been attracting a lot of interest because of the great advantages of reducing chip size and suppressing the parasitic inductance. Recently, we have reported a fully integrated GaN smart pulse-width modulation (PWM) 48V-to-1V buck converter [13].

In this work, 650 V GaN buffer and p-GaN gate power HEMTs, trench isolation, and GaN power ICs on 200 mm engineered substrates will be demonstrated as a first show-case to verify the feasibility of this concept.

II. EPITAXY AND FABRICATION

The AlGaIn/GaN buffer and active layers were all epitaxially grown on 200 mm engineered substrates using an AIX G5+ C Planetary Reactor® from AIXTRON, Germany. The 5×200mm mini-batch reactor combined with cassette-to-cassette configuration allows for a high productivity while maintaining very low number of particles for optimal yield. As shown in Fig. 1(a), the epi stack consists of a 200 nm AlN nucleation layer, a 3.9 μm (Al)GaN superlattice (SL) buffer, a 1 μm carbon-doped GaN back barrier, a 400 nm GaN channel, a 12.5 nm $\text{Al}_{0.23}\text{Ga}_{0.77}$ barrier, and an 80 nm Mg-doped p-GaN layer. The epitaxial layer stack was optimized regarding wafer

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bow ($<50 \mu\text{m}$), defect density, barrier tuning (Al-content and thickness), and the Mg-doping density in the p-GaN gate. *In-situ* data of the wafer surface temperature and the reflectance at 633 nm as well as an optical micrograph after the epitaxy are shown in Fig. 2.

Fig. 1. (a) Schematic cross-section of the epitaxial layer stack and (b) process integration flow.

The devices were processed using imec's 200 mm CMOS compatible process modules (Fig. 1(b)) [14]. A TiN layer was first deposited on the p-GaN, followed by the TiN layer dry etching. Then, a selective p-GaN to AlGaN dry etch was conducted using a BCl_3/SF_6 chemistry. Afterwards, the access area was passivated by a dielectric stack containing Al_2O_3 and SiO_2 . Nitrogen implantation was conducted for lateral isolation. The dielectric stack was then etched open in the gate area followed by the deposition and patterning of the gate metal stack. The gate processing was finalized by the deposition of a second SiO_2 layer. Ohmic contact formation of the source and drain contacts was done after the gate processing, using a low temperature annealing of the metal stack consisting of Ti, Al, Ti and TiN [15]. Trench isolation was made by etching the dielectric, (Al)GaN buffer, and Si(111) top layer, stopping in the SiO_2 buried oxide layer, followed by SiO_2 filling and chemical-mechanical polishing (CMP). The process flow was completed by local substrate contact, back-end metallization, and SiN passivation, as shown in Fig. 3. Fig. 4 demonstrates the photograph of a fully processed 200 mm GaN-on-QST® wafer.

The fabricated power HEMTs have a gate length (L_G) of $1.5 \mu\text{m}$, a total gate width (W_G) of 36 mm , a gate-to-source distance (L_{GS}) of $0.75 \mu\text{m}$, and a gate-to-drain distance of (L_{GD}) of $16 \mu\text{m}$. Multiple field plates are included to avoid premature OFF-state breakdown and also to suppress the current collapse.

Fig. 2. *in-situ* data of the surface temperature and the reflectance. The inset shows an optical micrograph of the surface after the epitaxial growth.

Fig. 3. Schematic cross-section of the integrated half-bridge, trench isolation, and local substrate contact.

Fig. 4. Photograph of the processed 200 mm GaN-on-QST® wafer.

III. ELECTRICAL CHARACTERIZATION

As shown in Fig. 5, the GaN buffer demonstrates a breakdown voltage of $>650 \text{ V}$ under the criterion of $10 \mu\text{A}/\text{mm}^2$ leakage current at 150°C . The higher leakage level at elevated temperatures is stemming from the surface leakage, which is inherent for GaN surface after passivation [16]. Tuning the epitaxial growth condition and buffer thickness is essential to reach the high voltage level. Fig. 5(c) compared the leakage behaviors of an optimized GaN buffer and a non-optimized GaN buffer on QST®. The horizontal trench isolation

breakdown voltage exceeds 850 V as presented in Fig. 6, fulfilling the 650 V power ICs integration requirement.

Fig. 7(a) demonstrated the processed 36 mm interdigital power HEMT. As shown in Fig. 7(b), the fabricated 36 mm power HEMTs with L_{GD} of 16 μm show a low on-resistance of 13 $\Omega\cdot\text{mm}$. The Au-free ohmic contact resistance reaches 0.5 $\Omega\cdot\text{mm}$. Fig. 7(c) shows the HEMTs feature a high threshold voltage V_{TH} of 3.1 V. The high V_{TH} is vital to suppress faulty turn-on during device switching.

Fig. 8 gives the OFF-state drain leakage that is $<1 \mu\text{A}/\text{mm}$ until 650 V, proving the high voltage blocking capability and pinch-off capability of the p-GaN gate HEMTs processed on QST®.

The dynamic performance is assessed by the double-pulsed I - V measurement as shown in Fig. 9(a), for which the transistor is stressed in OFF-state to induce some trapping in the device to mimic the real operating condition. The trapping possibly takes place in the p-GaN, in the buffer, or in the gate-to-drain access region. The normalized dynamic R_{ON} shift is below 20 % for the full voltage range, compared to a fresh HEMTs. The characterization has been performed until 600 V (Fig. 9(b)).

Fig. 5. Forward and reverse bias buffer vertical leakage characteristics of the epitaxial layer stack in Fig. 1(a) at (a) 25 and (b) 150 °C, and (c) comparison of the buffer leakage characteristics between an optimized and a non-optimized GaN buffer on QST®.

Fig. 6. Lateral breakdown characteristics of the trench isolation. The horizontal trench isolation breakdown voltage exceeds 850 V.

Fig. 7. (a) Photograph, (b) output, and (b) transfer characteristics of the processed 36 mm p-GaN gate power HEMTs on 200 mm GaN-on-QST® substrates.

Fig. 8. OFF-state leakage of the processed 36 mm p-GaN gate power HEMTs.

Fig. 9. (a) Double-pulsed I - V waveforms for measuring HEMTs dynamic R_{ON} and (b) dynamic R_{ON} is $< 20\%$ until 600 V.

IV. GAN IC

Furthermore, fully functional GaN power ICs of a HEMT with integrated driver, half-bridge, and half-bridge with integrated drivers have been processed as shown in Fig. 10. Fig. 10(a) depicts the schematic IC of the power HEMT with integrated driver, which can significantly reduce the parasitic inductance in the gate loop. The driver consists of a push-pull driver and two resistor-transistor logic (RTL) inverters, because of lacking p-MOSFET. The driver and the power HEMT are electrically isolated by two trenches. The monolithically integrated half-bridge comprising a low side HEMT and a high side HEMT is shown in Fig. 10(c) and (d). The source terminals

of these two devices are connected to their respective substrate, in order to suppress the back-gating effect [17]. Fig. 10(e) and (f) demonstrates the half-bridge with integrated drivers and a level shifter. These designs are beneficial to dramatically suppress the oscillation, to reduce the area consumption, and to promote the switching frequency.

Fig. 10. Photographs of the (a) schematic IC and (b) photograph of the fabricated HEMT with integrated driver, (c) schematic IC and (d) photograph of the fabricated half-bridge, and (e) schematic IC and (f) photograph of the fabricated half-bridge with integrated drivers and a level shifter.

V. CONCLUSION

In summary, 650 V high-performance e-mode p-GaN gate HEMTs and power ICs on 200 mm engineered substrates have been successfully demonstrated. The effective trench isolation in combination with the matched coefficient of thermal expansion make the engineered substrates a promising platform for next-generation power system. Future work will target the demonstration of 1200 V-class devices.

REFERENCES

[1] T. J. Anderson, A. D. Koehler, M. J. Tadjer, J. K. Hite, A. Nath, N. A. Mahadik, O. Aktas, V. Odnoblyudov, C. Basceri, K. D. Hobart, and F. J. Kub, "Electrothermal evaluation of thick GaN epitaxial layers and AlGaIn/GaN high-electron-mobility transistors on large-area

engineered substrates," *Appl. Phys. Express*, vol. 10, no. 12, pp. 126501-1–126501-3, Nov. 2017.

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- [2] V. Odnoblyudov, C. Basceri, and S. Farrens, "Engineered substrate structure for power and rf applications," U.S. Patent, 15, 621,335, 15 Feb., 2018.
- [3] T.J. Anderson, A. D. Koehler, M. J. Tadjer, J. K. Hite, A. Nath, N. A. Mahadik, O. Aktas, V. Odnoblyudov, C. Basceri, and K. D. Hobart, "Electrothermal evaluation of thick GaN epitaxial layers and AlGaIn/GaN high-electron-mobility transistors on large-area engineered substrates," *Appl. Phys. Express*, vol. 10, no. 12, pp. 126501-1–126501-3, Nov. 2017.
- [4] T. J. Anderson, L. E. Luna, A. D. Koehler, M. J. Tadjer, K. D. Hobart, F. J. Kub, O. Aktas, V. Odnoblyudov, and C. Basceri, "Lateral GaN JFET Devices on 200 mm Engineered Substrates for Power Switching Applications," In *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Oct. 2018, pp. 14–17.
- [5] A. Tanaka, W. Choi, R. Chen, R. Liu, W. M. Mook, K. L. Jungjohann, P. K. L. Yu, and S. A. Dayeh "Structural and electrical characterization of thick GaN layers on Si, GaN, and engineered substrates," *J. Appl. Phys.* Vol. 125, no. 8, pp. 082517-1–082517-12, Feb. 2019.
- [6] X. Li, M. Van Hove, M. Zhao, K. Geens, V. Lempinen, J. Sormunen, G. Groeseneken, and S. Decoutere, "200 V Enhancement-mode p-GaN HEMTs Fabricated on 200 mm GaN-on-SOI with Trench Isolation for Monolithic Integration," *IEEE Electron Device Lett.*, vol. 38, no. 7, pp. 918–921, Jul. 2017.
- [7] X. Li, K. Geens, W. Guo, S. You, M. Zhao, D. Fahle, V. Odnoblyudov, G. Groeseneken, and S. Decoutere, "Demonstration of GaN Integrated Half-bridge with On-chip Drivers on 200 mm Engineered Substrates," *IEEE Electron Device Letters*. 40, 1499-1502 (2019).
- [8] Navitas, NV6113 Datasheet. (2019). [Online]. Available: <https://www.navitassemi.com/download/>.
- [9] Efficient power conversion, EPC2108 datasheet. (2019). [Online]. Available: <https://epc-co.com/epc/Products/eGaNfetsandICs/EPC2108.aspx>.
- [10] S. Ujita, Y. Kinoshita, H. Umeda, T. Morita, S. Tamura, M. Ishida, T. Ueda, "A compact GaN-based DC-DC converter IC with highspeed gate drivers enabling high efficiencies," in *Proc. IEEE 26th Int. Symp. Power Semiconductor Devices IC's*, Jun. 2014, pp. 51–54.
- [11] B. Weiss, R. Reiner, V. Polyakov, P. Waltereit, R. Quay, O. Ambacher, and D. Maksimovic, "Substrate biasing effects in a high-voltage, monolithically-integrated half-bridge GaN-Chip," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Oct./Nov. 2017, pp. 265–272.
- [12] H. Wang, A. Man Ho Kwan, Q. Jiang, and K. J. Chen, "A GaN pulse width modulation integrated circuit for GaN power converters," *IEEE Transactions on Electron Devices*, 62(4), 1143-1149.
- [13] X. Li, N. Amirifar, K. Geens, M. Zhao, W. Guo, H. Liang, S. You, N. Posthuma, B. De Jaeger, S. Stoffels, B. Bakeroort, D. Wellekens, B. Vanhove, T. Cosnier, R. Langer, D. Marcon, G. Groeseneken, and S. Decoutere, "GaN-on-SOI: Monolithically Integrated All-GaN ICs for Power Conversion," in *IEDM Tech. Dig.*, pp.4.4.1-4.4.4, Dec. 2019.
- [14] N. E. Posthuma, S. You, S. Stoffels, H. Liang, M. Zhao, and S. Decoutere, "Gate architecture design for enhancement mode p-GaN gate HEMTs for 200 and 650V applications," in *Proc. IEEE 30th Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, May 2018, pp. 188–191.
- [15] B. D. Jaeger, M. V. Hove, S. Decoutere, and S. Stoffels, "Low temperature ohmic contacts for III-N power devices." U.S. Patent No. 9,634,107. 25 Apr. 2017.
- [16] X. Li, M. Zhao, B. Bakeroort, K. Geens, W. Guo, S. You, S. Stoffels, V. Lempinen, J. Sormunen, G. Groeseneken, and S. Decoutere, "Buffer vertical leakage mechanism and reliability of 200-mm GaN-on-SOI," *IEEE Electron Device Lett.*, vol. 66, no. 1, pp. 553–560, Jan. 2019.
- [17] X. Li, M. Van Hove, M. Zhao, K. Geens, W. Guo, S. You, S. Stoffels, V. Lempinen, J. Sormunen, G. Groeseneken, and S. Decoutere, "Suppression of the backgating effect of enhancement-mode p-GaN HEMTs on 200-mm GaN-on-SOI for monolithic integration," *IEEE electron device letters*, 39(7), 999-1002, 2018.