Investigation of the impact of hot-carrier-induced interface state generation on carrier mobility in nMOSFET

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***Abstract*—A comprehensive investigation on the hot carrier induced interface state generation and its impact on carrier mobility in nMOSFET is performed. I-V compact modelling and charge pumping characterization are used as independent ways to evaluate the interface state density as a function of hot carrier induced aging. From the two techniques, similar power-law time exponents of the interface state density kinetics are obtained. Assisted by the quasi-spectroscopic (temperature-resolved) charge pumping measurement, the extracted interface state density is further correlated with the I-V modelling results: an universal mobility degradation normalization parameter $N_{it,ref}$ =~4.1x10^{11}/cm^2 is reported, irrespective of the effective-oxide-thickness (EOT), stress temperature, or the relative degradation of the device-under-test (DUT). Supported by the fundamental principles deployed in the derivation as well as the broad range of experimental conditions considered for its validation, the reported normalization parameter could serve as a modelling constant in the commonly used I-V compact models to correlate the mobility degradation with the interface state density induced by hot carrier stress.**

***Index Terms*—Charge pumping, hot carrier degradation, MOSFET, compact model, reliability, electron mobility, interface state**

I. Introduction

As transistor's dimensions shrink without a corresponding reduction of the supply voltage, hot carrier degradation is becoming one of the main reliability concerns for state-of-the-art nMOSFETs [1,2]. Both TCAD- [3,4] and compact-model-based strategies [5,6,7] have been demonstrated for modelling the hot carrier induced device degradation. However, among all these efforts, no detailed investigation of the crucial correlation between the generated interface states and mobility degradation has been reported. Historically, different numerical forms have been used to translate a given interface state density into the corresponding mobility degradation [8,9,10,11,12]. Different proportionality relations have been used in these works, and no systematic match between experiments and models has been consistently demonstrated. While an accurate correlation between the interface state density and mobility degradation is clearly crucial, it is particularly challenging to establish given the combined effect of interface states on the device threshold voltage. Furthermore, establishing such correlation is crucial also for unambiguously decoupling the threshold voltage shifts induced by generated interface states and trapped oxide charge [13,14,15]. A lack of experimental validation of the consistency between the interface state density extracted by modelling the I-V curves and the physical defect density actually present in the aged device as probed, e.g., by charge pumping technique, may weaken any hot carrier degradation modelling effort. Therefore, establishing the correlation between hot carrier induced interface states and the corresponding mobility degradation is of fundamental importance for understanding and modelling hot carrier aging.

In this work, a systematic evaluation of hot carrier induced MOSFET degradation is performed, with focus on exploring the relation between carrier mobility degradation and interface state density: for the former, the charge-based EKV model [16,17] is used to fit the aged device I-V characteristics; for the latter, temperature-resolved charge pumping measurements are performed to estimate the total interface state density [18,19,20]. A consistent power-law time exponent is observed for both the interface state density as estimated by charge pumping and for the mobility degradation ratio as estimated by calibrating the EKV model; based on this agreement, a normalization relation between interface state density and mobility degradation ratio is established, and a single normalization parameter is reported for all the investigated experimental conditions and device technologies. These results demonstrate unambiguously that a single modelling equation with a universal normalization parameter can be used to translate the hot carrier induced interface state into the mobility degradation. This approach can be deployed in device aging compact models for circuit simulations.

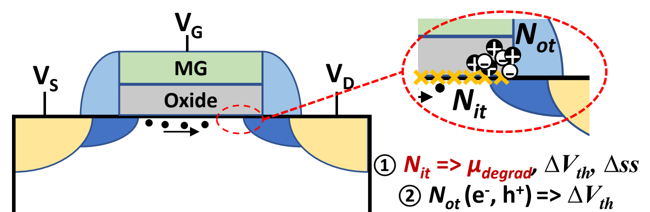

Fig. 1: Schematic representation of the hot carrier induced damage in the MOSFET, which typically localizes near the drain side due to the carrier energy peak there. Inset shows the hot carrier induced interface state N_{it} and oxide charge trapping N_{ot}: for the latter one, both electron

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and hole (from impact ionization) trapping can occur, depending on the carrier energy and local oxide field.

II. I-V Modelling

Hot carrier degradation, driven by the high energy carrier near the drain side of the channel [21], causes non-uniform degradation in the MOSFET. A schematic representation of the hot carrier induced localized damage in a MOSFET is shown in **Fig. 1**, where both hot carrier induced interface state (N_{it}) and oxide charge trapping (N_{ot}) are highlighted. The impact of hot carrier induced N_{it} is two-fold: first, it degrades the carrier mobility by introducing additional Coulomb scattering center; second, it affects the device electrostatics by shifting the threshold voltage and degrading the subthreshold slope. The localized nature of hot carrier degradation, combined with the kinetics of the defect density during stress, further complicates the interpretation of its impact on the device I-V characteristic. As the first step for correlating a given defect profile with the corresponding aged device I-V characteristic, in the next Section the connection between defect density and corresponding I-V modelling parameters is established.

A. The I-V model and its implementation

The charge-based EKV model [16,17] employed here to describe the device I-V is briefly introduced. The normalized pinch-off potential v_p and the normalized source and drain potential $v_{S,D}$ are defined in Eqs. (1-2):

$$v_p = (V_G - VTH)/(NIDE \cdot ut) \quad (1)$$

$$v_{S,D} = V_{S,D}/ut \ with \ ut = kT/q \quad (2)$$

Where k is the Boltzmann constant, T is the temperature in Kelvin and q is the elementary charge. $NIDE$ is the so-called ideality factor and mainly influences the device subthreshold current. $NIDE$ can be converted from the subthreshold slope as $NIDE=ss/[ut \cdot ln(10)]$. As the solution of the "charge-potential linearization" [16], the gate, drain, and source voltage are connected to the normalized charge $q_{S,D}$ through the Lambert-W (also known as product logarithm) function in Eq. (3).

$$q_{S,D} = 0.5 \cdot lambertw\left[2\,exp(v_p - v_{S,D})\right] \quad (3)$$

$$i_{f,r} = q_{S,D}^2 + q_{S,D} \quad (4)$$

By applying Eqs. (3-4) separately to the gate-to-source (forward current i_f) and gate-to-drain (reverse current i_r) sides, the drain current (5) is calculated as the difference between forward i_f and reverse current i_r, multiplied by the current normalization factor ($2 \cdot NIDE \cdot ut^2 \cdot C_{ox} \cdot W/L$) and carrier mobility ($\mu$). Such normalization relation helps in decoupling transistor sizes or technology dependence, as the normalized drain current is only a function of the device bias voltages (V_G, V_D, V_S), electrostatic control ($NIDE$) and temperature.

$$I_D = 2\frac{W}{L} NIDE \cdot ut^2 C_{ox} \mu (i_f - i_r) \quad (5)$$

Under strong inversion condition, where v_p-$v_{S,D} \gg 1$, Eqs. (4-5) can be further simplified into Eqs. (6-7) [16]:

$$i_{f,r} = \left[(v_p - v_{S,D})/2\right]^2 \quad (6)$$

$$I_D = \frac{W}{L} NIDE \cdot ut^2 C_{ox} \mu (v_D - v_S) \left[v_p - \left(\frac{v_D + v_S}{2}\right)\right] \quad (7)$$

Based on Eq. (7) and specifically to the hot carrier generated interface state N_{it}, several conclusions can be drawn: first, the impact of N_{it} on carrier mobility μ enters as a multiplication factor and will degrade the device transconductance; second, the impact of N_{it} on the threshold voltage VTH enters the pinch-off potential v_p and will only shift the I-V and transconductance parallelly; third, since the pinch-off potential v_p has already been normalized by $NIDE$ [this is to reflect the gate electrostatic control over the channel, see Eq. (1)], the impact of N_{it} on $NIDE$ only results in a slightly rescaled (v_D+v_S)/2 (right term inside the square bracket of Eq. 7). For a linear transfer characteristic (V_D=0.05V) and under strong inversion (v_p-$v_{S,D} \gg 1$), such impact is small. From above discussion and for the aged state, only the linear transfer characteristic under strong inversion will be modelled and only the N_{it} impact on μ and VTH needs to be considered.

Furthermore, to account for the impact of N_{it} on Coulomb scattering limited mobility (cf. ECO term), a bias dependent mobility model is introduced, whereas for all other scattering mechanisms, e.g., phonon-limited and surface-roughness limited scattering, a single power-law term is adopted to capture the lumped effect (cf. $EMOB$ term). The mobility representation is listed in Eqs. (8-9).

$$E_{eff} = -(Q_d + \theta \cdot Q_i)/\varepsilon_{si} \quad (8)$$

$$Q_i = NIDE \cdot ut \cdot C_{ox} \cdot q_s \quad (9)$$

Where E_{eff} is the effective field in silicon, and θ is the weighting factor for the inversion charge and equals 0.5 for electron [22]. Using Matthiessen's rule, the final mobility expression is obtained in Eq. (10).

$$\mu = 1/\left[\left(\frac{E_{eff}}{ECO}\right)^{-1} + \left(\frac{E_{eff}}{EMOB}\right)^{pmo}\right] \quad (10)$$

Where $ECO=ECO_0$ for pristine device. As described above, the hot carrier induced interface states will introduce additional Coulomb scattering centers and therefore modifying ECO. Such physical effect is addressed by the mobility degradation ratio K as defined below in Eqs. (11-12), which is then fed back to Eq. (10) to capture the degraded mobility μ.

$$ECO = ECO_0 \cdot (K + 1) \quad (11)$$

$$K = N_{it}/N_{it,ref} \quad (12)$$

With increasing interface state density N_{it} (e.g., generated by hot carrier stress), the Coulomb scattering term in Eq. 10 (left term in the denominator) becomes evens larger, and therefore the mobility μ within the Coulomb scattering-limited regime becomes smaller (note the negative exponent for the Coulomb scattering term). Such relation originates from the proportional relation between Coulomb scattering limited mobility and mean momentum relaxation time, which is inversely proportional to the defect density [23]. The modelling equations have also been widely used in [9,10,11,12]. It is worth to emphasizing again that the target of this work is to validate this mobility degradation relation experimentally, as well as to explore and to establish the mobility degradation normalization parameter $N_{it,ref}$.

To summarize this Section, the EKV model and its simplification under strong inversion are introduced, together with the physical mobility expression. Without considering the localization effect, the main feature of hot carrier degradation can be readily incorporated into the I-V model. For capturing the fresh linear transfer characteristic, 4 parameters (VTH, ECO_0, $EMOB$, pmo) need to be calibrated against measured I-V data of the pristine device. By combining Eqs. 1, 2 and 7, it can be seen that any $NIDE$ variation only results in a slightly rescaled (v_D+v_S)/2 (i.e., the right term inside the square bracket of Eq. 7) and has no impact on the gate electrostatics (through

v_p) under strong inversion; *NIDE* is therefore fixed to its pristine value calculated from the subthreshold swing (*ss*) without further adjustment. For reproducing the aged linear transfer characteristic under strong inversion, only 2 parameters (*ECO*, *VTH*) are modified: notice that only N_{it} will degrade Coulomb scattering and thus the transconductance, and therefore the proposed calibration scheme is inherently robust against parameter covariance.

B. The localized degradation and its equivalence

The other crucial aspect of hot carrier damage is its strong localization as depicted in **Fig. 1**, which significantly complicates its physical understanding and modelling. To address this issue and to enable correlating the I-V modelling with experimental techniques that directly probe the interface defects, e.g., charge pumping, in the following, a simple transistors chain model is used to demonstrate the equivalence between the degradation caused by a localized N_{it} profile and a uniformly distributed N_{it} profile for what concerns the mobility degradation ratio K.

The model of a single transistor in linear regime under strong inversion adopts Eq. (7); to formulate the drain current of the transistor chain, a current sensitivity model is considered following Eq. (13), where N is the number of identical transistors in the chain:

$$I_D = 1\Big/\left[N\cdot\left(\frac{1}{I_{D,1}}+\frac{1}{I_{D,2}}+\cdots+\frac{1}{I_{D,N}}\right)\right] \tag{13}$$

Based on the discussion above, two representative cases are considered. In the first case, only V_{th}-shift with different degree of localization is explored, whereas a fixed total degradation is maintained. As can be seen in **Fig. 2**, the nominal degradation of the "entire" device (transistors chain) depends on the degree of localization: the stronger the localization effect, the more the drain current degrades. Such result clearly indicates that the nominal V_{th}-shift fitted from the I-V model, only reflects an apparent V_{th}-shift of the aged device, which is closely coupled to the localization effect.

ΔV_{th} (V) vs. channel position (#1 near source and #10 near drain)

Slice	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10
A	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04
B	0	0	0	0	0	0	0	0	0.2	0.2
C	0	0	0	0	0	0	0	0	0	0.4

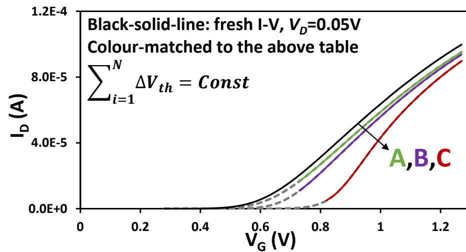

Fig. 2: V_{th}-shift calculations by using the transistor chain model (10 identical transistors): a uniform V_{th}-shift (case A in green) results in the smallest current degradation, whereas the strong localized degradation (case C in red) results in the largest degradation. The "deformation" in curve C is due to the large degradation of a single slice. Note: the solid-line represents the modelling results in strong inversion, whereas the dashed-line represents the entire I-V curve (only for reference).

The second case is the mobility degradation ratio [K, as defined in Eqs. (11-12)], where the mobility is degraded, and a constant total degradation is maintained. The result, as summarized in **Fig. 3**, clearly indicates the overall mobility degradation is completely insensitive to the localization effect, and only reflects the "integrated" degradation. This key property will be exploited for exploring the mobility degradation under hot carrier stress, and to correlate it with charge pumping measurement results.

The difference between V_{th}-shift and mobility degradation under different localization conditions can be understood as a direct result of the transistor chain and current sensitivity models (Eqs. 7 and 13). In fact, such positional sensitivity to interface states, which degrade carrier mobility, can be verified experimentally by measuring the forward and reverse (swapped Source/Drain) current degradation of the linear transfer curve under strong inversion, as exemplified in **Fig. 4**: for a given interface defect density generated under hot carrier stress, the linear current degradation is the same both for the case where defect-induced carrier scattering takes place at the source side (i.e., when carriers enter the channel region, cf. reverse current degradation), or for the case where such scattering takes place at the drain side (i.e., when carriers have travelled already along the channel, cf. forward current degradation) beyond which carriers are collected by the drain terminal. In fact, virtually no difference is observable between the forward and reverse linear current degradation. This observation readily confirms that the linear transfer curve under strong inversion is intrinsically insensitive to the relative defect location along the channel, whereas the defect density is the dominant factor for mobility (and thus linear current) degradation.

Mobility degradation ratio K vs. channel position

Slice	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10
A	2	2	2	2	2	2	2	2	2	2
B	0	0	0	0	0	0	0	0	10	10
C	0	0	0	0	0	0	0	0	0	20

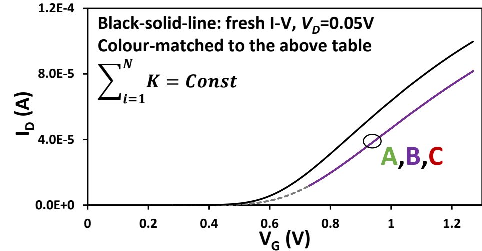

Fig. 3: The same "slicing" approach is applied to explore the mobility degradation. In contrast to the V_{th}-shift (Fig. 2), the mobility degradation ratio shows no dependence on the damage localization. Therefore, the average degradation extracted from the I-V model can be directly used.

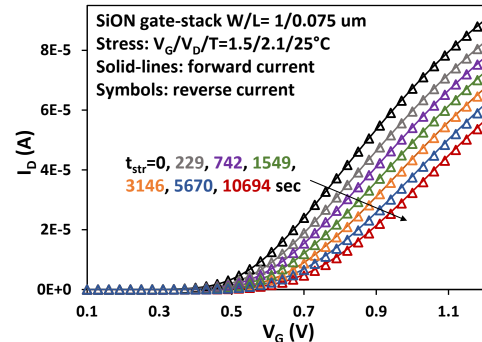

Fig. 4: Experimentally measured forward and reverse current degradation on device with SiON gate-stack (cf. device-B below), i.e., by swapping the bias (0.05V, 0V) between source and drain terminals. The negligible difference between forward and reverse current

degradation effectively supports the simulation results in Fig. 3, where the linear transfer characteristic under strong inversion is intrinsically insensitive to the defect localization.

III. Experiment

Following the model-based study presented in the previous Section, a wafer-level stress-measure experiment is performed with the goal of generating different degree of interface damage, including different degree of localization as well as different interface state density, which is then quantified by the charge pumping technique and is further correlated with I-V modelling results. For this purpose, two types of planar nMOSFET with gate-stack optimized to minimize oxide trapping are used. The V_{th}-shift under bias-temperature stress for device-A (V_G=1.8V, V_D=0.05V, T=125°C) is below 1mV for the longest stress time considered, and therefore the charge trapping component can be neglected in our study, focusing only on the hot carrier degradation. **Table I** summarizes the DUTs and test conditions: note in this study, we are considering the averaged-out impact of a sufficiently large interface state population, whereas the individual defect induced degradation under hot carrier stress is beyond the scope of this work, as it would require a description of the percolated channel conduction in ultra-scaled devices, as opposite to the continuous compact model used here.

Table. Ⅰ: Summary of device technologies and stress conditions used in this work.

	Gate-stack	EOT	W/L_{eff}(um/um)	Stress {V_G,V_D}	Stress T (°C)
Device-A	HKMG	1.3nm	1/0.075	{1,1.8}, {1.2,1.8}, {1.4,1.8}, {1.6,1.8}	25, 75, 125
Device-B	SiON	2.3nm	1/0.075	{1.5,1.9}, {1.7,1.9}, {1.9,1.9}, {1.5,2.1}	25, 75, 125

For the electrical characterization, the cycled stress-measure sequence shown in **Fig. 5** is used: after the DC "stress" stage, the device's linear transfer characteristic is probed, followed by the charge pumping (CP) measurement using the base level sweep technique [19]. The base level of the CP trapezoidal waveform is swept from inversion to accumulation, whereas the amplitude is kept at 1.2V; the leading and trailing edges are kept at 50ns. The CP measurement within each "measure" stage will be referred to as "in-situ" CP (as opposed to the more thorough post-stress CP discussed next). Since the CP probed N_{it} is strongly dependent on the measurement temperature (i.e., the hot carrier stress temperature for the "in-situ" CP) and does not reflect the total N_{it} value, a post-stress temperature-resolved CP measurement (CP-T) is performed (referred below as "ex-situ") for extracting the temperature dependence of N_{it} which allows to estimate the total N_{it} and to rescale the "in-situ" CP results.

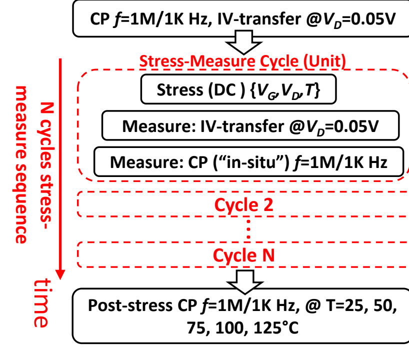

Fig. 5: A cycled stress-measure sequence is used for hot carrier degradation characterization. After the DC stress, both I-V and CP measurements are performed in each "measure" stage. Up to 10^4 seconds cumulative stress time is applied experimentally.

IV. Results and Discussion

The wafer-level stress experiment is performed with the above-described measurement sequence (**Fig. 5**), covering the test devices and conditions listed in **Table I**. The measured I-V transfer characteristics are fitted with the EKV model. An example of the fitting results is plotted in **Fig. 6**-the linear transfer characteristic under strong inversion is accurately captured. The inset of **Fig. 6** shows the time evolution of the fitted K and ΔV_{th}: a power-law ($y=kx^n$) is used to describe the kinetics of both the extracted quantities. The discrepancy between the kinetics (i.e., time-exponents n) of the two quantities–despite them being manifestations of the same generated interface state profile–is due to the strong dependence of ΔV_{th} on the underlying damage localization, as discussed in Section II-B. Furthermore, recalling **Fig. 2**, it is to be expected that the apparent ΔV_{th} in the inset of **Fig. 6** represents a (large) over-estimation of the actual ΔV_{th} (intended as the pure electrostatic impact of a given interface charge density). It is important to point out that the ΔV_{th} will also modify the mobility-gate voltage relation via the inversion carrier [n_{inv} in Eqs. (8-10)]; however, such secondary effect is small compared to the mobility degradation ratio K, especially for devices with gate-stack specifically optimized to minimize charge trapping under the relevant stress conditions, as done here. Based on the I-V fits, the modelled carrier mobility is plotted as a function of inversion carrier density n_{inv} in **Fig. 7**, for increasing stress times.

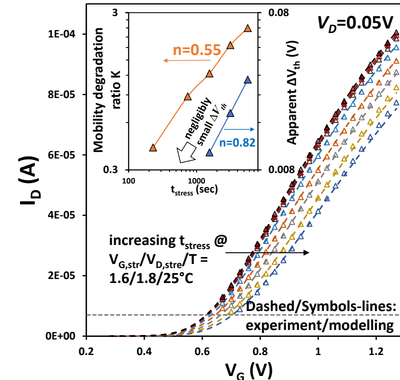

Fig. 6: Measured I-V curves (dashed lines) plotted against the calibrated compact model (symbols). For the aged I-V's, only the I-V curve under strong inversion is fitted and plotted. The inset shows the time evolution

of the fitted quantities K (mobility degradation ratio) and ΔV_{th}. Note: as indicated by the bold arrow in the inset, the fitted short-term ΔV_{th} is below the modelling resolution and is therefore neglected.

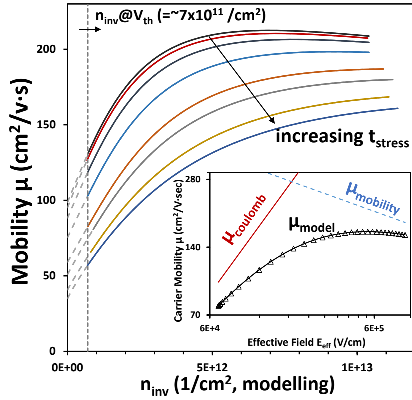

Fig. 7: The modelled mobility in device-A (corresponding to the I-V fits of Fig. 6) is plotted as a function of n_{inv}, for increasing stress times. The inset shows the limiting mechanism of carrier mobility in a pristine device under different effective field E_{eff} using Eqs. (8-10): for low E_{eff}, the mobility is limited by Coulomb scattering; with increasing E_{eff}, the impact of Coulomb scattering is reduced.

Immediately after each I-V measurement, the "in-situ" CP measurement is performed; an example of the results is depicted in **Fig. 8**. The interface state density is evaluated from the peak substrate current ($I_{sub}=qA_gN_{it}f$, where A_G and f are the effective gate area and CP frequency). However, as the "in-situ" CP measurement temperature is compliant to the stress temperature, the temperature dependence of the defect energy level that can be probed by CP measurement has to be considered. To account for this effect, a post-stress ("ex-situ") CP-T measurement is performed, where the temperature is swept from 25-125°C with a 25°C-step. Note that a typical wafer chuck temperature change is finished within ~10min, after which the CP-T measurement is performed again, the tight experimental timing control further suppresses any potential recovery of hot carrier induced interface state [24]. An example of the "ex-situ" CP-T measurement is shown in **Fig. 9**.

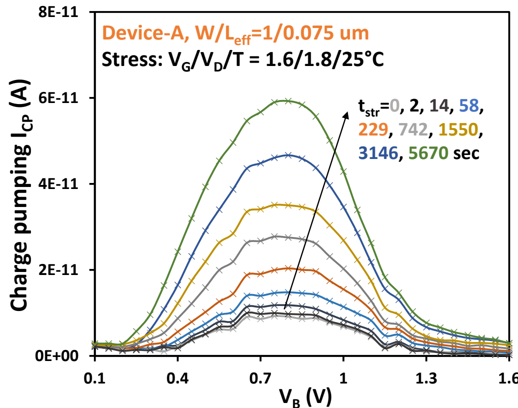

Fig. 8: "In-situ" base-level sweep CP measurement [18,19] used to monitor the degradation kinetics. The CP current I_{CP} is evaluated as the current difference between high-frequency (f=1MHz) and low frequency (f=1KHz) values, to exclude any contribution related to gate leakage.

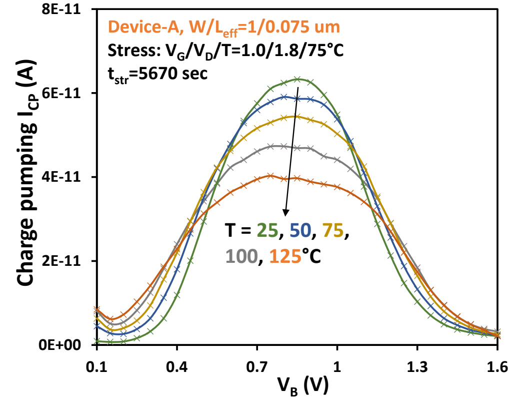

Fig. 9: An example of the "ex-situ" CP-T measurement result. As the measurement temperature increases, I_{CP} decreases.

The "ex-situ" CP-T result is evaluated using the theory proposed in [18,19], where the temperature dependence of the CP current has been described by Eq. (14), with the parameters *a, b, c* defined in Eqs. (15-17):

$$I_{CP}(T) = -aT - bTln(T) + c \tag{14}$$

$$a = 2qkfA_g\overline{D_{it}} \cdot \ln\left[\sqrt{\sigma_n\sigma_p}\sqrt{\frac{3k}{m^*}}K_i\frac{|V_{th}-V_{fb}|}{\Delta V_g}\sqrt{t_rt_f}\right] \tag{15}$$

$$b = 2qkfA_g\overline{D_{it}} \tag{16}$$

$$c = qfA_g\overline{D_{it}}E_g \tag{17}$$

Note $\overline{D_{it}}$ is the average interface state density ($1/cm^2 \cdot eV$) and E_g is the band gap of silicon. After fitting the experimental I_{CP} with Eqs. (14-17), the interface state density ($1/cm^2$) is calculated with Eq. (18). An example of this complete N_{it} extraction can be found in **Fig. 10**.

$$N_{it} = \overline{D_{it}} \cdot E_g \tag{18}$$

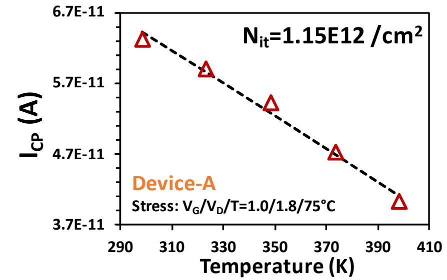

Fig. 10: Extracted N_{it} based on the "ex-situ" CP-T measurement, cf. Eqs. (14-18) [18,19].

The ratio between N_{it} and $N_{it,T}$ (where the latter represents the N_{it} estimated simply by the peak CP current at each temperature during the CP-T measurement) is calculated and summarized in **Fig. 11**. It is important to emphasize that the extraction of "T-rescaling ratio" only involves the data collected during the "ex-situ" CP-T measurement and does not involve any "in-situ" CP results. Such experimental design also helps in improving the robustness against potential recovery of hot carrier induced interface state [24], albeit it is observed to be negligible for the investigated devices. Since the CP-T measurement temperature is a super-set of the stress measurement temperature, only the extracted "T-rescaling ratio" is needed for rescaling the "in-situ" CP measured interface state density.

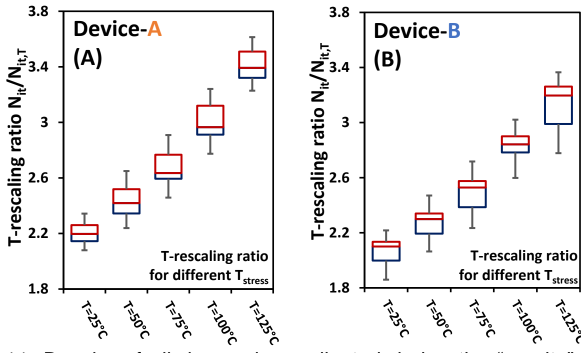

Fig. 11: Boxplot of all data points collected during the "ex-situ" CP-T measurement. Despite the similar trend in temperature dependence, the different "T-rescaling ratio" between device-A (A) and device-B (B) may come from the difference in electron and hole capture cross-sections (σ_n, σ_p) in Eq. (15).

For each measured device, a single "T-rescaling ratio" can be extracted and used to correct the "in-situ" CP results. Based on these procedures, the rescaled N_{it} value ("with T-rescaling") is expected to reflect the total interface state density, i.e., not influenced by the hot carrier stress temperature, and should therefore closely correlate with the mobility degradation ratio K as extracted from the I-V modelling. To examine this point, the time evolutions of the two quantities (K, N_{it}) are plotted in **Fig. 12** and time-exponent n is compared in **Fig. 13** for all ~32 devices that were measured: the two exponents, as extracted using two independent approaches, shows a relative difference no larger than 10%. Such extensive match clearly justifies the experimental design discussed above and enables further numerical treatments.

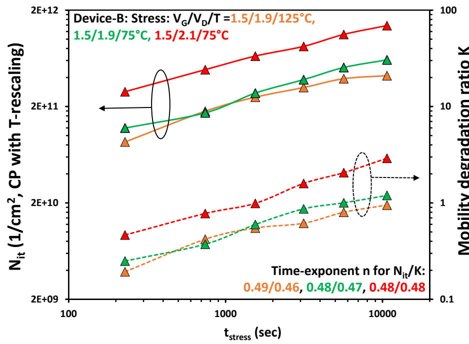

Fig. 12: The temperature-rescaled ("with T-rescaling") N_{it} from CP measurement and the mobility degradation ratio K from I-V modelling are plotted versus the stress time for 3 stress conditions as examples. The power-law time-exponent n is fitted and summarized in Fig. 13. The $N_{it,ref}$ (=N_{it}/K) as defined in Eqs. (11-12) can be further extracted based on these data.

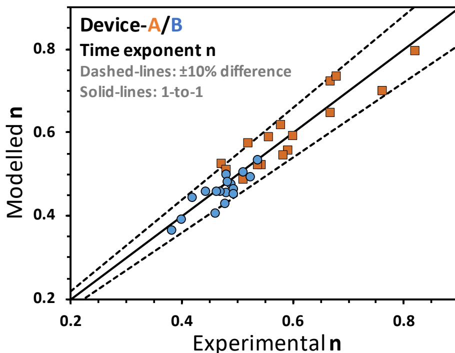

Fig. 13: Comparison between the experimental n, i.e., time-exponent from the CP measured N_{it}, and the modelled n, i.e., time exponent from the modelled I-V mobility degradation ratio K.

By taking the ratio between N_{it} and K, as defined in Eqs. (11-12), the mobility degradation normalization parameter $N_{it,ref}$ can be extracted for each measured device and each stress time. In order to feed back the CP results to the I-V model, as well as to demonstrate the consistency between the CP-measured N_{it} ("with T-rescaling") and the I-V modelled N_{it} (via K ratio), it is important to examine the various dependences of $N_{it,ref}$, i.e., the EOT, the temperature, and the degradation dependence. For this purpose, the $N_{it,ref}$ vs. stress measurement temperature for both device types are plotted in **Fig. 14**-no systematic dependence upon EOT or temperature can be observed. Furthermore, as visualized in **Fig. 15**, no consistent degradation dependence is observed, i.e., the normalization parameter $N_{it,ref}$ does not change with increasing interface state density. Therefore, regarding the mobility degradation normalization parameter $N_{it,ref}$, a constant median value of ~$4.1\text{x}10^{11}/\text{cm}^2$, with a standard deviation of ~$4.7\text{x}10^{10}/\text{cm}^2$, is reported based on the broad experimental evidence discussed in this work. Based on the established $N_{it,ref}$ value, it is possible to accurately evaluate the integrated stress-induced N_{it} based on the compact model of the device I-V, or conversely to convert a given stress-induced N_{it} into mobility (and therefore current) degradation.

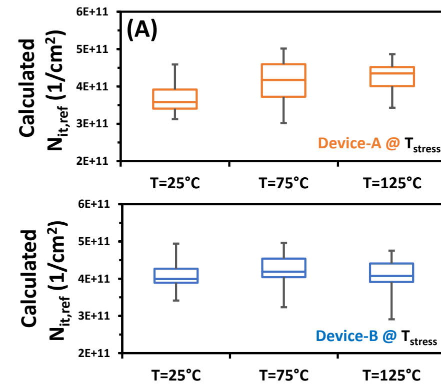

Fig. 14: The EOT dependence [by separating the two device types: (A) device-A; (B) device-B] and the temperature dependence are checked by categorizing the extracted $N_{it,ref}$: no systematic EOT or temperature dependence is observed. Note: the temperatures listed above refer to the stress temperatures (and not the temperature of the "ex-situ" CP-T measurement).

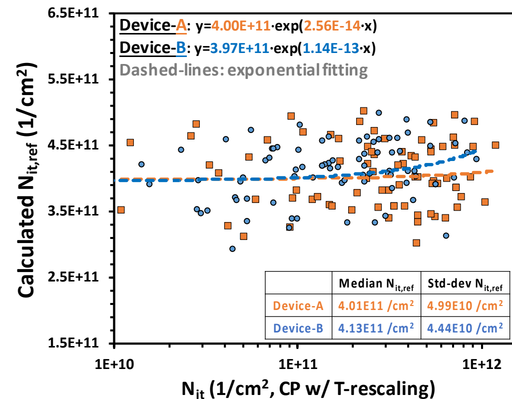

Fig. 15: The degradation dependence of $N_{it,ref}$ is examined: despite the small upwards tail observed in device-B for very large stress-induced

interface state density (which deviates by just ~10% from its median value), no systematic degradation dependence of $N_{it,ref}$ is observed. A constant median value of $N_{it,ref}$ =~4.1x10^{11}/cm^2 with a small standard deviation of ~4.7x10^{10}/cm^2 is therefore reported.

V. SUMMARY

In this work, a comprehensive investigation of the impact of the hot carrier induced interface state on carrier mobility in nMOSFET has been performed. The impact of localization effect under hot carrier stress has been investigated, which indicated that the mobility degradation ratio is not influenced by the localization effect and therefore can be directly probed experimentally and correlated to the total integrated N_{it}. The EKV-based I-V model and the charge pumping measurement were used as independent techniques for probing the interface state density in aged devices. A good agreement in the time-evolution of the degradation as assessed by the two independent techniques was demonstrated, validating the effectiveness of the modelling equations in translating a physical interface defect density into the corresponding carrier mobility. Furthermore, by sampling across a broad range of stress voltages, stress temperatures, and different device technologies, a single mobility degradation normalization parameter ($N_{it,ref}$ =~4.1x10^{11}/cm^2) was reported, with negligible EOTs, stress temperatures or device degradation level-dependences. Based on the combined experimental techniques, and supported by the consistency across a broad range of experimental conditions, the extracted mobility degradation normalization parameter $N_{it,ref}$ is expected to act as an universal constant in the commonly used I-V compact models, to bring improved consistency between the interface state density as estimated from the I-V compact model and the physical interface state density actually present in an aged device.

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