A Compact 26.5-29.5 GHz LNA-Phase-Shifter Combo With 360° Continuous Phase Tuning Based on All-Pass Networks for Millimeter-Wave 5G

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Abstract—This article presents a compact integrated receiver front-end for phased-arrays at 5G n257/n261 band (26.5-29.5 GHz) employing both a low-noise amplifier (LNA) and a novel passive phase-shifter based on variable-phase all-pass networks. The proposed phase-shifter topology is analysed and designed using 0.25 μm BiCMOS achieving continuous tuning capabilities with 360° phase range over a 25-33 GHz frequency range under 0.1 mm^2 of area. The proposed phase-shifter is measured standalone, achieving 8.3 ± 0.55 dB losses at 29 GHz with an RMS gain error below 0.6 dB across the entire frequency range. When quantizing the continuous phase-shift into 6 bits, an RMS phase error $< 3^\circ$ is obtained. To build the LNA-Phase-shifter combo, the phase-shifter is then integrated with an LNA optimized for compactness, which was measured standalone, showing a noise figure below 3.2 dB across the n257/n261 band and 20 dB gain under 0.0625 mm^2 of area. The small size of both the phase-shifter and LNA enables an ultra-compact phased-array receiver front-end under 0.2 mm^2 of area. The front-end is measured, achieving 11.5 ± 0.53 dB of gain, RMS gain error below 0.42 dB and RMS phase error below 3.2° over the entire n257 band, measured input-referred P1dB of -25 dBm and a 15 mW DC power consumption.

Index Terms—n257 band, n261 band, 5G, all-pass networks, phased arrays, receiver front-end, mm-waves, beamforming, phase-shifter, LNA

I. INTRODUCTION

INTEGRATED phased-array transceivers are gaining popularity with the deployment of millimeter-wave (mm-wave) 5G. The need to employ hundreds of antennas to overcome propagation losses, together with the small wavelengths at mm-waves, has led to the full integration of phased-array RF chains in a single die [1]. These chips can drive one to several antennas, have both transmitting and receiving capabilities, and even support multiple polarizations [2]. Fig. 1 shows the block diagram of such a receiver beamforming chip.

One fundamental block of phased-array chains is the phase-shifter. Phase-shifters enable analog beamforming (ABF) ca-

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Fig. 1. Block diagram of an integrated receiver front-end for antenna arrays.

capabilities, a crucial aspect for phased-arrays, which improves signal-to-noise ratio (SNR) in receiving mode and effective isotropic radiated power (EIRP) in transmission mode [3]. Signal phase-shifting can be applied in different parts of the chain [4], with RF-path phase-shifting being widely employed as it allows mitigation of out-of-beam interferers prior to mixing, while simultaneously avoiding LO distribution issues commonly observed in LO-path beamforming [5]. RF phase-shifters themselves can also be implemented using several topologies, such as switched-type phase-shifters (STPS) [6], [7], reflective-type phase-shifters (RTPS) [3], [8] and vector modulators (VMs) [9].

Independently of the phase-shifter topology, All-Pass Networks (APNs) are typically employed in phase-shifters when broadband or multi-band capabilities are desired [7], [9]–[12], trading off other key performance indices, such as area and phase-shifting resolution. For example, a 15-35 GHz VM is presented in [9] using static APNs to generate quadrature paths, and in [7] a 14-50 GHz STPS is introduced employing four parallel static APNs. More recently, we have introduced in [13] a synthesis technique to implement dynamic variable-phase APNs (VP-APNs) at mm-waves. Using silicon technology, the VP-APNs were explored to enable a 14-54 GHz multi-band phase-shifter with continuous tuning, addressing the resolution gap.

As VP-APNs remain rather unexplored, we have proposed an ultra-compact phase-shifter in the 24-30 GHz frequency range [14]. Using a single lower-order network with digitally controlled capacitors, a 2-bit, 45° phase-shift was obtained within an area of 0.028 mm^2 . The design targeted 5G mobile applications in the 24-30 GHz frequency range, and since mobile users have a smaller number of antennas, the coarse

resolution is acceptable [7]. The high-performance achieved under a ultra-small form-factor demonstrated that APNs are not only useful to achieve broad-bandwidth.

However, despite recent works on mm-wave APN based phase-shifters, most of the reported components come with compromises, whether a specific application such as 5G mobile [7], [14] or broadband capabilities costing all other performance indexes [7], [9]. Hence, APN-based phase-shifters are yet to be proven against more typical phase-shifters found in the state-of-the-art, which often targets high-resolution, low-loss and compact form-factor. Therefore, the aim of this article is to present such a phase-shifter based on APNs, extending the work in [14] to address a broader range of phased-array applications, such as base-stations or customer premise equipment (CPE).

The main contributions of this paper are as follows.

- 1) We present a novel analysis of a second-order APN-based phase-shifter, using straightforward expressions to design APNs and VP-APNs, supporting future developments using these circuits. The analysis proposed here is based in transfer functions, hence not topology-dependent as in [15], and does not require numerical synthesis such as in [7], [14].
- 2) A novel phase-shifter design is presented using VP-APNs, extending the work from [14] by addressing its drawbacks against the state-of-the-art, namely its limited resolution and phase-range, required for a broader range of applications. The proposed topology achieves 360° phase-range and continuous phase-tuning capabilities within 25-33 GHz frequency range. In contrary to a single digitally controlled VP-APN from [14], an analog controlled VP-APN stage and an 180° STPS stage are proposed in cascade, with a 2-bit attenuator added to improve magnitude and phase orthogonality.
- 3) To the best of our knowledge, the proposed phase-shifter is the first APN-based phase-shifter at mm-waves to achieve competitive benchmarks against prior art, showcasing the capabilities of the circuit topology. Additionally to 360° continuous tuning, it achieves an average insertion loss (IL) of 8.3 ± 0.55 and a RMS phase error of 1° at 29 GHz, under 0.1 mm^2 of area and zero power, despite the use of a $0.2 \text{ }\mu\text{m}$ node. It contrast with the previous phase-shifters that used APNs [9], [13], where broad bandwidth operation was targeted, sacrificing IL, RMS errors and area.
- 4) To evaluate the phase-shifter performance under a phased-array system, we have combined the proposed phase-shifter with a low-noise amplifier. The LNA-Phase-shifter combo is designed targeting 5G's n257-band [16], from 26.5 to 29.5 GHz, achieving 11.5 ± 0.53 dB of gain at 28 GHz. With the phase-shifter quantized in 6-bits, the RMS gain and phase error are kept below 3.2° and 0.42 dB, respectively, across the entire n257-band frequency range. In addition, a measured noise figure (NF) from 3.4 to 4 dB is achieved. Such performance is achieved under 0.2 mm^2 of area, offering state-of-the-art performance. As phased-array transceivers get more integrated, die size is a growing

Fig. 2. Beamforming architectures: (a) RF-path, and (b) LO-path.

concern among chip manufacturers, and the proposed design demonstrates high-performance under a small silicon area. Furthermore, it is the first mm-wave integrated receiver block reported in literature using a VP-APN based phase-shifter.

The remaining of this paper is organized as follows. Section II reviews phase-shifters for mm-wave beamforming. In Section III we analyse the APN based phase-shifter and describes the phase-shifter design. Section IV shows the LNA design and LNA-phase-shifter combo. Fabrication and measurement results are shown in Section V. Finally a conclusion is given in Section VI.

II. PHASE-SHIFTERS FOR MM-WAVE BEAMFORMING

Phase-shifters are characterized by two aspects: 1) their location in the signal chain (or which beamforming architecture it will be employed); and 2) their circuit topology.

In an array architecture, with the signal going from RF to baseband, phase-shifters can be placed in different locations. This defines the type of beamforming, with the most common architectures found in literature being RF-path and LO-path beamforming [5]. With RF-path phase-shifting in receiver mode [see Fig. 2(a)], the signal would be combined before down-conversion, allowing the spatial filtering to mitigate out-of-beam interferers, and relaxing the requirements of the sub-sequential blocks in the chain. The main drawback of using RF-path phase-shifting is the insertion loss added to the signal by the phase-shifter, which can affect overall system performance. LO-path phase-shifting [see Fig. 2(b)], on the other hand, removes the phase-shifter from the signal path, and places it in the LO-path, which is much less sensitive to magnitude variations. LO-path phase-shifting relaxes the magnitude and phase orthogonality requirements, but it comes with its problems. First, since combining is performed after down-conversion, the mixer must be designed to handle out-of-beam interferers. Additionally, routing the LO between multiple antennas can be very challenging. Finally, each antenna requires its mixer, which increases the overall footprint of the total chain. Since compactness is a major target of this design, RF-path beamforming was selected. However, the phase-shifter presented here could be employed in a LO-path architecture after tuning.

Regarding their circuit implementation, phase-shifters can have an active or passive implementation. Passive phase-shifters have zero static power consumption, are bi-directional, and much less susceptible to non-linearities. Since low-power is a major target of our design, in this work we focus on

Fig. 3. Passive phase-shifter topologies: (a) RTPS and (b) STPS.

Fig. 4. Block diagram of the proposed phase-shifter.

passive topologies. An in-depth discussion on active topologies can be found in [4]. Despite their benefits, passive phase-shifters generally have higher insertion loss (IL) and occupy larger area. Passive phase-shifter topologies can be broadly split into two categories: 1) reflection-type phase-shifters (RTPS) and 2) switched-type phase-shifters (STPS).

RTPS [see Fig. 3(a)] operate by means of splitting the signal with a quadrature hybrid coupler, reflecting the signal using a reactive impedance Z_R and combining both reflected signals at the output. The phase-shift is achieved by varying the reactive impedance Z_R , typically implemented using varactors and inductors. RTPS topologies are excellent for high-resolution phase-shift, with phase-range and bandwidth being a limiting factor. To achieve large phase-range, cascade of multiple stages are often needed [17] or complex loads with multiple control voltages are employed [3], [18], [19]. In both cases, increasing range comes with an increase in IL and overall area. Additionally, the bandwidth operation of RTPS is often limited by the hybrid coupler.

STPS [see Fig. 3(b)] work by switching between different signal paths with a phase-difference between those paths [20]–[22]. STPS are excellent to achieve coarse phase-shift steps. However, the increase in resolution in STPS is achieved by cascading many stages, leading to higher losses and an increase in area. Thus, STPS are more suitable for lower resolution applications. One method often used by STPS to reduce area consumption is to implement the two paths using the same set of inductors, embedding the switch within the paths [20], [21]. Regarding bandwidth, since switches are typically broadband devices [23], the STPS bandwidth is typically limited by the phase-shifting paths.

The topology proposed in this work combines the best properties of both worlds. The coarser phase-shifting steps (180° and 90°) are implemented on a STPS manner, providing two paths for the signal to go, using APNs as paths. To reduce the overall area consumption, the switch is embedded within the network for the 90° step, implementing a digital VP-APN. The high-resolution is achieved using an analog VP-APN with varactors, combining multiple phase-states into a single block, like a RTPS. A 2-bit attenuator is also added to compensate the gain variation introduced by both the digital and analog VP-APNs, improving magnitude and phase orthogonality. The following section analyses and describes the design in detail.

One interesting trade-off often overlooked in phase-shifters is between the overall area and signal processing technique (single-ended or a differential). Although in general differential operation doubles the block area, in a differential phase-shifter the implementation of a 180°-bit stage is much simplified to a sign flipping switch [17], [22], which can be quite small and have low loss. Single-ended topologies in theory occupy less area, but they require a proper phase-shifting stage for the 180° bit as well, which can be rather challenging. It often ends up implemented by cascading two blocks, often doubling the area with a much higher penalty on insertion loss. This work is implemented single-ended to simplify characterization, and it proposes the use of APNs with external switches to implement the 180° bit, avoiding excessive cascading, and achieving low insertion loss with a compact area.

III. ANALYSIS AND DESIGN OF A VP-APN BASED PHASE-SHIFTER

A. Analysis of All-Pass based Phase-Shifters

All-Pass networks are excellent candidates for phase-shifting applications as they decouple the magnitude and phase behaviour, differently than high-pass or low-pass filters. Let $G(s, \omega_o, Q_p)$ be a second order all-pass transfer function (TF) given by

$$G(s, \omega_o, Q_p) = \frac{s^2 - \frac{\omega_o}{Q_p}s + \omega_o^2}{s^2 + \frac{\omega_o}{Q_p}s + \omega_o^2}, \quad (1)$$

where ω_o is the natural frequency, and Q_p is the quality factor of the pole. With $s = j\omega$, the magnitude of $G(j\omega, \omega_o, Q_p) = 1$, and the phase is given by

$$\angle G(j\omega, \omega_o, Q_p) = -2 \tan^{-1} \left(\frac{\omega\omega_o Q_p^{-1}}{\omega_o^2 - \omega^2} \right), \quad (2)$$

To obtain phase-shift, at least a pair of APNs is needed, where one acts as a reference phase. Consider the pair of networks $G_1(s, \omega_{o1}, Q_p)$ and $G_2(s, \omega_{o2}, Q_p)$, defined as in (1), as a phase-shifting pair. Q_p is kept the same between the two networks, to enable the implementation of VP-APNs [13], [14]. Their phase-difference, $\Delta\phi = \angle G_2 - \angle G_1$, is given by

$$\Delta\phi(j\omega) = 2 \tan^{-1} \left(\frac{\omega\omega_{od}\Delta\omega_o Q_p^{-1}(\omega^2 + \omega_{od}^2)}{(\omega_{od}^2 - \omega^2)^2 + \omega^2\omega_{od}^2(Q_p^{-2} - \Delta\omega_o^2)} \right) \quad (3)$$

$$\omega_{od}^2 = \omega_{o1}\omega_{o2}; \Delta\omega_o = \frac{\omega_{o1} - \omega_{o2}}{\omega_{od}} \quad (4)$$

The phase-shift reaches its maximum at $\omega = \omega_{od}$, leading to

$$\Delta\phi_{max}(j\omega_{od}) = 4 \tan^{-1}(\Delta\omega_o Q_p) \quad (5)$$

Fig. 5. Behavior of phase-shift vs. frequency between two second-order APNs.

Fig. 6. (a) Bandwidth vs. Q_p for different values of ϕ_{PS} , with $\delta = \pm 2^\circ$; (b) Bandwidth vs. Q_p for different values of δ , with $\phi_{PS} = 90^\circ$.

1) *Bandwidth of Phase-Shift*: Since the theoretical magnitude of an APN is constant over frequency, the bandwidth is often defined by its phase-behaviour. The phase-shift curve behaves as pictured in Fig 5. A phase-shift ϕ_{PS} is obtained within a bandwidth $BW = (\omega_H - \omega_L)/\omega_{od}$ with a maximum error of $\pm\delta$. At the phase-shift peak frequency ω_{od} , the maximum phase-shift within this error is $\phi_{PS} + \delta$. Applying it to (5), we get

$$\phi_{PS} + \delta = 4 \tan^{-1}(\Delta\omega_o Q_p). \quad (6)$$

Eq. (6) is a simple relationship between the desired inputs - phase-shift (ϕ_{PS}) and maximum allowed error (δ) - and the design variables (Q_p and $\Delta\omega_o$). However, with (6) an infinite set of ($Q_p, \Delta\omega_o$) pairs can be used to implement the same phase-shift. To narrow down the selection of Q_p and $\Delta\omega_o$, we can observe BW . We know that at the bandwidth edges (ω_H and ω_L), the phase-shift achieved is

$$\Delta\phi(j\omega_L) = \Delta\phi(j\omega_H) = \phi_{PS} - \delta \quad (7)$$

Applying (7) to the left side of (3) leads to a quartic equation to find the BW of the phase-shifter. For simplicity, we show in Fig. 6 numerical results for BW in % versus Q_p for different values of ϕ_{PS} and δ . The remaining variable $\Delta\omega_o$ can be found from (6). As expected, the larger the desired phase-shift, the smaller the bandwidth, as it is. Also, the larger the phase-error $\pm\delta$ allowed. But the main takeaway from Fig. 6 is that by decreasing Q_p we can maximize bandwidth, regardless of the other variables, which directs us to select Q_p as low as possible. Although theoretically true, values for Q_p are limited by implementation, as we will see next.

2) *From Transfer-Function to Network*: Towards implementation, the TF values are then mapped to a prototype network (with inductors and capacitors), which are then scaled

Fig. 7. Possible topologies for APN implementation. (a) Prototype component values, (b) Lattice, (c) inductive Bridged-T and (d) capacitive Bridged-T.

Fig. 8. (a) Tuning range vs. Q_p for different values of ϕ_{PS} , with $\delta = \pm 2^\circ$; (b) Tuning range vs. Q_p for different values of δ , with $\phi_{PS} = 90^\circ$.

to the desired center frequency f_{sc} and the desired impedance Z_o . In the case of second-order APNs, different topologies are possible, such as lattice and bridged-T inductors, as pictured in Fig. 7. From a phase-shifter perspective, two approaches are possible: 1) the two all-pass TFs G_1 and G_2 are implemented using separated networks and external switches are used to shift the phase, such as conventional STPS; or 2) embedding the switch in a VP-APN approach, scaling the inductors of both networks to the same value and switching between capacitor values.

The first approach is straight-forward, both TFs follow the standard flow, with switches added externally. Naturally, having two physical networks separately leads to increase in area.

The VP-APN approach requires the condition of both networks having the same Q_p , as we enforced before, to guarantee both networks have *linearly scalable inductors* [13]. We map the components of the prototype networks, then proceed with scaling to the desired frequency. However, the impedance scaling is done such that $L_{a1} = L_{a2}$ and $L_{b1} = L_{b2}$, which means scaling G_1 to $Z_1 = Z_o \sqrt{\omega_{o1}/\omega_{o2}}$ and G_2 to $Z_2 = Z_o \sqrt{\omega_{o2}/\omega_{o1}}$. With such impedance scaling, the inductors reach the same value, but the capacitors values diverge further, with the maximum capacitor increasing and the minimum decreasing. We can define the tuning ratio TR between maximum and minimum capacitors, and applying the definitions in (4) we get

$$TR = \frac{C_{max}}{C_{min}} = \left(\frac{\omega_{o2}}{\omega_{o1}} \right)^2 = \left(1 + \frac{\Delta\omega_o}{\sqrt{1 + \frac{\Delta\omega_o^2}{4} - \frac{\Delta\omega_o}{2}}} \right)^2 \quad (8)$$

in which (6) can be applied, to obtain

Fig. 9. Schematic of the second-order VP-APN. (b) Table with All-pass networks' synthesis values

Fig. 10. Simulated results of the ideal VP-APN for both 0° and 90° phase-states. (a) S_{11} . (b) Phase-shift. (c) Group delay.

$$TR = \frac{C_{max}}{C_{min}} = \left(1 + \frac{\tan\left(\frac{\phi_{PS} + \delta}{4}\right)}{\sqrt{Q_p^2 + \frac{1}{4} \tan\left(\frac{\phi_{PS} + \delta}{4}\right) - \frac{1}{2} \tan\left(\frac{\phi_{PS} + \delta}{4}\right)}} \right)^2 \quad (9)$$

From (9), one can notice that the tuning ratio C_{max}/C_{min} is inversely proportional to Q_p . Fig. 8 plots Q_p versus tuning ratio for given amounts of phase-shift. Although from a bandwidth point of view Q_p should be maximized, it also mean a larger tuning ratio is required. Moreover, when implementing variable capacitors using silicon technology, TR is often constrained to a maximum of around 3. This means that VP-APN implementations with a very low Q_p can be unfeasible, and its choice depend on technology. By manipulating (9) we can find the minimum Q_p allowed:

$$Q_p \geq \tan\left(\frac{\phi_{PS} + \delta}{4}\right) \sqrt{\left(\frac{1}{2} + \frac{1}{\sqrt{TR_{max}} - 1}\right)^2 - \frac{1}{4}} \quad (10)$$

3) *Implementation Flow*: Based on the analysis, a simple implementation flow is proposed:

- Specify desired phase-shift ϕ_{PS} and maximum allowed error δ , center frequency f_c and characteristic impedance Z_o .
- Use (10) to find the minimum Q_p , given a maximum TR of the technology used.
- Find $\Delta\omega_o$ using (6) and make $\omega_{od} = 1$, thus finding ω_{o1} and ω_{o2} using (4).
- With the transfer function, create the prototype networks [see Fig. 7].
- Scale both networks in frequency by $2\pi f_c$.

Fig. 11. Variable capacitor implementation for: (a) 90° bit, using switched capacitors; (b) 90° analog using differential varactors.

Fig. 12. Simulated results for the 90°-bit section. (a) S_{21} , (b) phase-shift, (c) S_{11} , and (d) group-delay.

Fig. 13. Simulated results for the 90° analog section. (a) S_{21} , (b) phase-shift, (c) S_{11} , and (d) group-delay.

- Scale the impedance of G_1 to $Z_1 = Z_o \sqrt{\omega_{o1}/\omega_{o2}}$ and of G_2 to $Z_2 = Z_o \sqrt{\omega_{o2}/\omega_{o1}}$, such that $L_{a1} = L_{a2}$ and $L_{b1} = L_{b2}$.
- The resulting capacitors should fall within the maximum tuning range specified.

B. Implementation of 90° bit and 90° analog blocks

Using the proposed implementation flow, we proceed to design both 90° sections, implemented using the same VP-APN architecture, whose schematic is pictured in Fig. 9(a). The inductive bridged-T topology was selected due to compactness, as it can be implemented using a single center-tap inductor. The phase-shift is then provided by the use of variable capacitors, which is the main distinction between analog and digital block - their variable capacitor implementation. The 90° digital is implemented using digital capacitor bank, and the 90° analog using a varactor. The maximum tuning range we

Fig. 14. Complete schematic of the proposed phase-shifter, with each block highlighted.

used was $TR = 2.65$, mostly limited by the varactor, which is slightly lower than the maximum allowed by the technology, allowing some slack for PVT variations. Using $\phi_{PS} = 90^\circ$ and $\delta = \pm 2^\circ$, we obtain $Q_p \geq 0.862$. We then follow the implementation flow proposed, with $Z_o = 50 \Omega$ and $f_c = 28$ GHz, obtaining the component values in Fig. 9(b).

The ideal VP-APN was simulated using SPICE, and the result is shown in Fig. 10. Although the networks are mismatched on purpose, S_{11} is kept below -13 dB from 22 to 32 GHz, and the phase-shift is mostly unaffected, as proven in [13]. The use of linear-phase APNs enables a small variation in group delay, shown in Fig. 10(c). At the center frequency of the phase-shift, both networks have the same group delay.

The digital capacitor bank is implemented as shown in Fig. 11(a). When M_{sw} is off, the node capacitance is given by the parallel capacitor C_o plus the parasitic components of the MOSFET in parallel. In cases where the off-state capacitance is small, C_o may not be used. When M_{sw} is turned on, the capacitance seen by the node is given by $\approx C_1/2$. Since triple-well MOSFETs are not available in the selected process, we used a deep-on/off technique to improve the switch's performance. By biasing both drain and source with $V_b = 2.5$ V and switching v_{sw} from 0 to 5 V, we guarantee $V_{gs} = \pm 2.5$ V in both on and off states.

The analog implementation of variable capacitors is shown in Fig 11(b), where an anti-series varactor configuration was selected for the following reasons: first, it enables bias isolation for the tuning voltage, containing it within the 90° analog block; secondly, the anti-series configuration has shown greater linearity capabilities [24]; finally, a multi-finger layout of the anti-series configuration enables higher quality factor.

Using Cadence Spectre, we simulated both the 90° bit and 90° analog sections. Inductors and transmission lines were EM-simulated in ADS Momentum. Simulated results for the 90° bit are plotted in Fig. 12, where a phase-shift close to the ideal VP-APN is obtained, with S_{11} kept below -13 dB over the whole range. Due to the on-resistance of the switch, a large variation in S_{21} is seen between both phase-states, which will be compensated by the 2-bit attenuator.

Simulated results for the 90° analog are shown in Fig. 13, where the tuning voltage was swept from 0 V to 5 V in 1 V steps. From the simulations, it seems the analog section would not be able to cover the full 90° phase range. This effect occurs since the varactor models provided are extrapolated above 10 GHz, underestimating the capacitance tuning range and overestimating losses. However, from our previous experiences with varactors models in the same process, the tuning range of 2.65 is achieved comfortably at 28 GHz. This will become clear with the phase-shifter measurements, where a full 360° coverage of phase-states is obtained. The VP-APNs final implementation is pictured in the complete phase-shifter schematic, shown in Fig. 14.

C. 180° bit

Introducing 180° phase-shift using VP-APNs becomes unfeasible as it would require a very large tuning range, leading to a large impedance mismatch. A viable option is to cascade two 90° sections, however the combined losses of two single VP-APN and large magnitude variation between on and off states would not be ideal. Therefore, a STPS section using external SPDTs was implemented using passive APNs, as shown in Fig. 14. The implementation procedure follow the proposed flow, however since these are passive networks, no tuning range is used to select Q_p . Although technically a small Q_p can be used to increase bandwidth, due to the large phase-shift desired, it might lead to unfeasible components. With some trial and error, we selected $Q_p = 0.84$ and $\delta = \pm 3^\circ$ to achieve both feasible components and sufficient bandwidth. The resulting schematic is shown in Fig. 14.

Taking advantage of both switched paths, the SPDT design could be simplified when compared to conventional switches. Since the high and low-state are 180° out of phase, the isolation requirements of the switch are further reduced. The leakage from the off-path would be combined 180° phase-shifted, subtracting itself from the on-path, only leading to a small S_{21} drop. This slack in isolation requirement allow us to remove shunt switches, simplifying the matching network as well. The deep-on/off technique used for the 90° -bit switch

Fig. 15. Simulated results for the 180°-bit section. (a) S_{21} , (b) phase-shift, (c) S_{11} , and (d) group-delay.

was also used here to reduce further switch losses and power handling capabilities.

The 180°-bit section was also simulated using Cadence Spectre, with the inductors and transmission lines simulated in ADS Momentum. The results are plotted in Fig. 15. A phase-shift swing around 180° is obtained at the frequency range of interest with an S_{11} kept below -10 dB across the simulated band. The use of APN with linear phase for both high and low phase networks minimizes the group delay variations, and both states have the same group delay in mid-band. Additionally, by using passive networks instead of internally switched VP-APNs, the S_{21} variation between phase states is minimized, which reduces the requirements for the attenuator.

D. Attenuator and Final Phase-Shifter

Due to the Q-factor variation between the states of the VP-APNs, a 2-bit attenuator was added to introduce extra losses to compensate for the Q-factor variation. Large insertion loss differences between phase-states lead to higher gain variation and RMS gain error, which key performance indices of phase-shifters, and therefore should be minimized. The attenuator schematic is pictured in Fig. 14, with 2-bit resolution, introducing attenuation in 0.7 dB steps. Due to small attenuation levels, the effect into the phase behavior is minimal. Nonetheless, since continuous phase-tuning is available via analog control, any extra phase-shift introduced by attenuation stages could be compensated by co-designing the settings.

The final schematic of the proposed Ka-band phase-shifter, combining all building blocks from Fig. 4, is pictured in Fig. 14. The layout was implemented in a compact manner, to reduce overall area. The phase-shifter was placed on-wafer as a standalone device for individual characterization. The resulting design's on-wafer photograph is depicted in Fig. 17(a), with a core area of $0.303 \times 0.33 \text{ mm}^2 \approx 0.1 \text{ mm}^2$.

IV. LNA DESIGN AND COMBO WITH PHASE-SHIFTER

The phase-shifter proposed here is integrated with an LNA targeting phased-array applications. The targeted frequency range is the 5G NR n257 band, from 26.5 to 29.5 GHz. To compensate the approx. 8 dB loss introduced by the phase-shifter, the amplifier requires at least 18 dB of gain to obtain

Fig. 16. Low-noise amplifier schematic.

a minimal 10 dB gain for the front-end. By introducing the LNA before the phase-shifter, the overall receiver noise figure (NF) is set by the amplifier, therefore an optimized design for low-noise is needed. The SiGe process used in this work has bipolar transistors optimized for low-noise performance [25], which allows us to go for a simplified LNA design, targeting minimal area and low-power.

The schematic of the implemented LNA is depicted in Fig. 16. Although differential solutions are often used for beamformer chips, LNAs are typically implemented single-ended since antennas are often implemented single-ended. Having at least the first stage single-ended helps to achieve low NF, avoiding the first block in the chain to be a balun [26], [27]. Hence, our proposed schematic is a single-ended LNA. Due to the high-gain transistor available, a single-stage cascode with an emitter-follower is sufficient to deliver the desired gain for the LNA-Phase-shifter combo. The biasing current of the first stage is set at 4 mA as a trade-off between low-power, NF and sufficiently linearity. A higher bias current would increase linearity and lower NF, sacrificing the overall power consumption, while a lower current would save power but sacrifice the NF and linearity, hence the choice. The input transistor width is selected to optimize the current density for low NF_{min} and a equivalent noise resistance close to 50 Ω [28]. The input matching is designed for simultaneous noise and power matching, with the degeneration inductor L_e obtained using the $\Gamma_{opt,in}$ procedure from [29]. The input base inductor L_b is added to tune-out the input reactance and to bring the input impedance to 50 Ω .

Instead of doubling the first stage, we used an emitter follower with ohmic matching to reduce the overall number of inductors, further reducing the area consumption. For the output emitter follower design, its biasing current is set equal to the input stage through resistor R_o , simultaneously matching the output to 50 Ω . Using a resistor avoids additional inductors, leading to overall reduced area when compared to cascading two cascode stages. One drawback is a higher variation over corners when compared to inductors. Also, another drawback is a lower gain since the voltage gain of the emitter follower is ≈ 1 . To obtain power gain using the emitter follower, the inter-stage network $R_{is} - L_{is} - C_{is}$ is designed at a higher impedance, namely around 200 Ω . The impedance ratio of

Fig. 17. On-wafer photo of: (a) standalone phase-shifter, (b) standalone LNA and (c) LNA-Phase-shifter combo.

≈ 4 enables an extra 6 dB in S_{21} . Furthermore, this interstage matching avoids excessive peaking of the amplifier when compared to pure reactive matching, enabling a wider 3-dB bandwidth. Finally, a DC-block capacitor isolates the LNA's DC voltage, with its total parasitics (C_o) bringing the reactive impedance to an improved conjugate matching between LNA and phase-shifter.

The LNA was placed on wafer as a stand-alone device to be characterized, and its on-wafer photograph is depicted in Fig. 17(b). The core area is $0.25 \times 0.25 \text{ mm}^2 = 0.0625 \text{ mm}^2$. It consumes 8 mA from a 1.8 V rail, resulting in 15 mW power consumption. Both LNA and phase-shifter were combined into a single receiver front-end, and its on-wafer image is depicted in Fig. 17(c). The resulting core area of the LNA-Phase-shifter combo is $0.6 \times 0.33 \text{ mm}^2 = 0.198 \text{ mm}^2$.

V. FABRICATION AND MEASUREMENTS

The proposed phase-shifter, LNA and combo were fabricated using NXP's $0.25 \mu\text{m}$ SiGe BiCMOS technology with a peak f_T/f_{max} of 216/177 GHz [30]. The technology supports six metal layers, Metal-oxide-Metal (MIM) capacitors and varactors. On-wafer photos of the fabricated devices are shown in Fig. 17. Despite having larger channel lengths, which leads to higher losses in the phase-shifter, the selected process also has high-gain low-noise NPN HBJ transistors [25]. The benefits of the selected technology will be highlighted in the LNA-Phase-shifter combo measurements. The devices were measured using Agilent's 67 GHz PNA E8361A network analyzer for S-parameter measurements. To characterize non-linearities and NF, we utilized Keysight's 67 GHz PNA-X N5247B network analyzer. On-wafer probing was performed through G-S-G probes with $125 \mu\text{m}$ pitch, which were calibrated up to probe-tips using a short-open-load-through approach. To control the phase-shifter, a dc probe-card was used. Simulations per-

Fig. 18. Measured S-parameters of the standalone phase-shifter, with different colors representing different coarse settings.

Fig. 19. Effect of the attenuator in the average S_{21} (average value of S_{21} between all phase-states) and the S_{21} variation over that average S_{21} of the phase-shifter.

formed in ADS Momentum together with Cadence Spectre were used to compare with the measurements.

A transition from probe to transmission line (a grounded coplanar waveguide) was designed and placed back-to-back on-wafer. Since the measured back-to-back S_{21} was above -0.15 dB and the S_{11} was below -30 dB at the frequency range of interest, the transition was not de-embedded from the results.

A. Continuous-Tune Phase-Shifter

The S-parameters measurement results are plotted in Fig. 18. The results shown here are for all discrete phase states, with different colors indicating different coarse settings. The analog section was biased from 0 to 5 V with 50 voltage points, leading to 200 phase-states measured. The attenuation level selected was optimized to reduce the gain variation while sacrificing the average insertion loss as little as possible. The average S_{21} varies from -8 to -8.7 dB across the 25 – 33 GHz frequency range. The mid-band S_{21} is -8.34 ± 0.55 dB, showing a very small gain variation over the 200 measured phase-states. The contributions of each stage were estimated from simulation, with the 180° stage adding 3 dB, both analog and digital VP-APNs adding around 2.5 dB each, and the remaining 0.3 dB from the attenuator. The small variation is reflected in the RMS gain error, kept below 0.6 dB across the 25 – 33 GHz frequency range.

The return losses S_{11} and S_{22} show reasonable matching but not excellent. Especially the S_{22} , which sees the analog

Fig. 20. Measured (a) insertion phase, (b) group delay, and (c) phase-shift of the standalone phase-shifter. The phase-shift curves are obtained by subtracting the reference phase state (0° coarse, $V_b = 5V$).

Fig. 21. Measured S_{21} and phase-shift vs. voltage at 28 GHz of the phase-shifter.

VP-APN first, the mismatch is accentuated. This effect occurs due to the purposely mismatched networks. In some phase states, the low-impedance state of the digital VP-APN might encounter a high-impedance state from the analog VP-APN, leading to a higher mismatch than expected for the standalone networks. Nonetheless, S_{22} is kept below -7 dB.

To highlight the effect of adding the attenuator, we plotted in Fig. 19 the average S_{21} and the variation over that average with and without attenuation. The addition of attenuation reduces the maximum variation over average from ± 2 dB to ± 1.1 dB, greatly improving the RMS gain error. The drawback is the reduction in the average S_{21} , which sees an extra 0.5 dB loss.

Insertion phase and phase-states are shown in Fig. 20, in which the phase-shift curves are obtained by subtracting the reference phase state (0° coarse, $V_b = 5V$). A full 360° coverage with continuous phase-control can be observed. Another achievement of this design, due to being based on linear-phase APNs, is the phase-state flatness over frequency, shown by the measured group delay. A variation of ± 6 ps around the average is observed. Furthermore, it is important to highlight that each phase-state are plot over frequency for a fixed setting, without reoptimizing for a different frequency.

To observe the phase-shifter behavior versus voltage, we fixed the frequency at 28 GHz and plotted both S_{21} and phase-shift, as shown in Fig. 21. For the phase-shift, the continuous tuning capability is well observed here, with some overlap between the discrete states. The S_{21} versus voltage at 28 GHz is bounded between -7.8 dB and -8.9 dB, showing a ± 0.55 dB variation over the mean. The sharp jumps in the S_{21} curves between two adjacent points are due to the use of attenuation. This effect is not observed in the phase curve, showing that

Fig. 22. Measured results considering a 6-bit quantization of the proposed phase-shifter. (a) S_{21} vs. frequency. (b) Phase-shift vs. frequency, some states omitted for clarity. (c) S_{21} vs. phase-shift at 29 GHz. (d) RMS gain and RMS phase-errors vs. frequency. Meaning of different colors as described before in Fig. 18.

the attenuator has negligible effect on the phase.

B. 6-bit quantization of the Phase-shifter and Discussion

To better compare with state-of-the art phase-shifters, the proposed design, although capable of continuous phase-shifting, was quantized to a 6-bit resolution phase-shifter using an external 8-bit digital-to-analog converter (DAC). This allows us to evaluate RMS phase errors, a typical metric in phase-shifter design. The selection of phase-states was performed in order to minimize RMS gain and phase error, and they were selected from the already measured phase-states. It is important to highlight that the use of a DAC with redundant bits (since it is a 6-bit phase-shifter) is a typical approach found in RTPS [3], [18], [19], and it can be useful to not only optimize performance but also as a tool to compensate possible PVT variations on the system.

Fig. 22 shows the phase-states for a 6-bit quantization level, which means a 5.625° phase-shifting step. The RMS phase error was calculated as in [7]. Notice that the RMS phase error was kept below 2° from 25.5 GHz to 31.5 GHz, and below 3° across the whole 25 – 33 frequency range.

Table I compares the proposed phase-shifter's performance with the state-of-the-art. When compared to other STPSs, where improvement in resolution comes by cascading sections, the proposed design achieved a smaller area while having a higher resolution and competitive losses with smaller nodes.

One limitation of the proposed design is the requirement of two voltage domains. These domains were employed here to overcome technology limitations, enabling switches with a better performance in order to compete much smaller nodes such as 45nm SOI. However, the topology could be implemented with a single voltage rail. Despite using these techniques, the reported IL is more on the higher end of the spectrum when compared to other designs, which is expected due to the higher switch losses that come from larger nodes. Another downside here is the requirement of one DAC to allow digital control of the phase. Nonetheless, as discussed in [3], the DAC speed

TABLE I
STATE-OF-THE-ART MM-WAVE PASSIVE PHASE SHIFTERS

	Garg [3] TMTT'17	Gu [19] TMTT'19	Tousi [31] RFIC'16	Elkholy [22] TMTT'18	Kodak [21] RFIC'17	Shin [20] MWCL'16	Xia [17] RFIC'19	This work Continuous	This work 6-b Quant.
Process	65 nm CMOS	65 nm CMOS	0.13 μ m BiCMOS	40 nm CMOS	45 nm SOI	65 nm CMOS	45 nm SOI	0.25 μ m BiCMOS	
Approach	RTPS	RTPS	Tunable TL	STPS	STPS	STPS	RTPS	STPS + VP-APN	
Signal Proc.	Single ended	Single ended	Diff.	Diff.	Single ended	Single ended	Diff.	Single ended	
Control	Analog, four voltages	Analog, one voltage	Digital	Digital	Digital	Digital	Digital	Analog, one voltage	
Freq. Range (GHz)	28	29	26 – 30	22 – 36	25 – 33	27.5 – 28.4	29	25 – 33	
Phase Range ($^{\circ}$)	360 $^{\circ}$	373 $^{\circ}$	180 $^{\circ}$	360 $^{\circ}$	360 $^{\circ}$	360 $^{\circ}$	360 $^{\circ}$	360 $^{\circ}$	
Phase Resol. ($^{\circ}$)	11.25 $^{\circ}$	22.5 $^{\circ}$	5 $^{\circ}$	45 $^{\circ}$	11.25 $^{\circ}$	22.5 $^{\circ}$	5.6 $^{\circ}$	Cont.	5.6 $^{\circ}$
RMS Phase Err. ($^{\circ}$)	1.5 $^{\circ}$	N/A	< 0.6 $^{\circ}$	< 12.8 $^{\circ}$	< 5 $^{\circ}$	< 8.98 $^{\circ}$	0.3	N/A	< 3 $^{\circ}$
RMS Gain Err. (dB)	N/A	N/A	< 0.2	< 0.6	< 0.8	N/A	0.1	< 0.6	
Loss mid. band (dB)	7.75 $\pm$ 0.3	8.3 $\pm$ 1.05	9.3 $\pm$ 0.25	5.6 $\pm$ 0.5	7 $\pm$ 1	6.6 $\pm$ 1	6.8 $\pm$ 0.1	8.3 $\pm$ 0.55	
Power (mW)	0	0	0	0	0	0	0	0	
Area (mm 2)	0.16	0.076	0.18	0.132	N/A	0.23	0.065	0.1	

should be high enough to allow beam training, in the order of tens of MHz, and a 8-bit DAC with 20-mV resolution was used. The low speed and moderate resolution should enable low power and low area implementations.

When compared to other reported RTPS, it is important to highlight that the works in [3], [17], [19] highly optimize their performance for a single frequency, changing settings when moving to a different frequency. This allows them to optimize the numbers for a given frequency and report low errors. In the proposed phase-shifter, settings are kept constant throughout the band. The phase-flatness of linear-phase APNs contributes to less variations over frequency, keeping the RMS phase-error below 3 $^{\circ}$ and the RMS gain error below <0.6 dB across the whole frequency range without changing settings. This is a crucial advantage in mm-wave 5G applications, where signal bandwidth goes up to 800 MHz.

C. Standalone LNA

The S-parameters of the LNA are plotted in Fig.23. The LNA exhibits a measured peak gain of 19.8 dB, with 3-dB bandwidth from 24.5 GHz to 31 GHz. The measured S_{11}/S_{22} also show reasonable matching, with an S_{11} below -13 dB over the 3-dB band, and a slightly higher S_{22} to improve the matching to the phase-shifter, as discussed in Section IV. A measured reverse isolation above 30 dB is observed over the whole measured frequency range. The measured group delay is between 55 and 65 ps around from 26.5 to 29.5 GHz. Measurement results follow close the simulation trends.

To evaluate LNA linearity, a gain-compression analysis (GCA) was performed by sweeping the input power at 28 GHz, with the results plotted in Fig. 24(a). A measured input-referred 1-dB compression point (IP1dB) of -24.5 dBm was observed, with a linear-region gain of 19.8 dB. The same GCA was performed at different frequencies, with the IP1dB results shown in Fig. 24(b). The IP1dB show small variations around the -24.5 dBm value over the frequency range from 26.5 to 29.5 GHz.

A two-tone measurement was also performed for several frequency points to observe intermodulation distortion. The

Fig. 23. Simulated and measured (a) S_{21} , (b) group delay, (c) S_{11}/S_{22} , and (d) S_{12} /Isolation of the standalone LNA.

Fig. 24. Non-linear measurements for the standalone LNA. (a) Measured output power and gain with respect to input power at 28 GHz. (b) Measured IP1dB and IIP3 versus frequency.

measured input-referred third-order interception point (IIP3) is plotted over frequency in Fig. 24, showing a small variation over -15 dBm at the frequency range of interest, from 26.5 to 29.5 GHz.

NF measurements were performed using the PNA-X cold-source method [32] and compared with simulations from

Fig. 25. Simulated and measured Noise Figure (NF) of the standalone LNA.

Fig. 26. Measured S-parameters and RMS gain error of the LNA-Phase-shifter combo, with different colors indicating different coarse settings.

Fig. 27. Measured (a) insertion phase, (b) group delay, and (c) phase-shift of the LNA-Phase-shifter combo. The phase-shift curves are obtained by subtracting the reference phase (0° coarse, $V_b = 5V$).

Spectre, as pictured in Fig. 25. Measurement results were obtained using 200 sample average and a 3 points smoothing. A measured NF from 3 to 3.4 dB was obtained over the n257 frequency band. An extra 0.3 dB is observed in the measurement result, most likely due to modelling imperfections or due to the pre-amplifier used in the measurement path.

D. LNA-Phase-shifter Combo Module

The S-parameters of the LNA-Phase-shifter combo are plotted in Fig. 26, with similar settings as the phase-shifter measurements from Section V. Once again, results are shown for 200 phase-states, with attenuation choice optimized for the n257 frequency band. A peak average gain of 11.55 dB was obtained at 28 GHz, with a ± 0.53 dB variation over

Fig. 28. Measured S_{21} and phase-shift vs. voltage at 28 GHz for the LNA-Phase-shifter combo.

Fig. 29. Measured input-referred 1 dB compression point (IP1dB) and input-referred third order intercept point (IIP3) of the LNA-Phase-shifter combo vs. frequency to illustrate the effect of changing settings of the phase-shifter. Each plot shows the effect of changing a single block and keeping the others fixed.

that average. The average gain curve also achieved a 3-dB bandwidth from 24-31 GHz, successfully covering the n257 frequency band. Large variation is observed below the n257 band, due to sub-optimal attenuation choices for that region. An RMS gain error below 0.5 dB was measured within the n257 band, and below 1 dB over the 3-dB bandwidth range. S_{11} results show small variation with respect to phase-states, mainly due to high reverse isolation of the LNA, and it is kept below -13 dB over the 3-dB bandwidth. The S_{22} , on the other hand, exhibits similar poor behavior as the stand-alone phase-shifter with a upper limit of -6 dB.

The measured insertion phase, group delay, and phase-shift for the combo are plotted in Fig. 27, where the phase-shift curves are obtained by subtracting the reference phase state (0° coarse, $V_b = 5V$). For clarity, some phase-states are omitted. A full 360° coverage is achieved over the 3-dB band, with overlap between discrete states. The measured group delay varies from 105 to 130 ps in the n257 band, with a maximum variation of ± 7.5 ps over average. At 28 GHz, the measured group delay is 122 ± 5.5 ps.

S_{21} and phase-shift variation versus voltage are shown in Fig. 28 at 28 GHz. Continuous phase-shifting is observed, with S_{21} varying from 11 dB to 12.1 dB. The effect of attenuators is well visible in the S_{21} , seen by the large jumps. However their effect in the phase-shift is almost negligible.

TABLE II
COMPARISON WITH PREVIOUSLY REPORTED INTEGRATED LNA-PHASE-SHIFTER

	Garg [3] TMTT'17	Min [6] JSSC'08	Kalyoncu [33] TCASII'20	Shakib [34] TMTT'19	Kodak [35] RFIC'16	Gao [36] TMTT'20	Kadam [37] TCASII'20	This work
Process	65 nm CMOS	0.12 μ m BiCMOS	0.13 μ m BiCMOS	40 nm CMOS	45 nm SOI	45 nm SOI	65 nm CMOS	0.25 μ m BiCMOS
Bandwidth (GHz)	27 – 29	30 – 40	22 – 27	27 – 30	25 – 33	22 – 44	27 – 29	26.5 – 29.5
Phase Range ($^{\circ}$)	360 $^{\circ}$	360 $^{\circ}$	180 $^{\circ}$	360 $^{\circ}$	360 $^{\circ}$	360 $^{\circ}$	180 $^{\circ}$	360 $^{\circ}$
Phase Resol. ($^{\circ}$)	11.25 $^{\circ}$	22.5 $^{\circ}$	5.6 $^{\circ}$	45 $^{\circ}$	5.6 $^{\circ}$	11.25 $^{\circ}$	11.25 $^{\circ}$	5.6 $^{\circ}$
RMS Phase Err. ($^{\circ}$)	< 4 $^{\circ}$	< 12.5 $^{\circ}$	< 6 $^{\circ}$ [†]	< 10 $^{\circ}$	< 4 $^{\circ}$	< 6 $^{\circ}$	< 2.8 $^{\circ}$	< 3.2 $^{\circ}$
Gain (dB)	9.5 $\pm$ 0.4	11 $\pm$ 1.5	28.5 $\pm$ 1.5	16.8 $\pm$ 0.5	12.2 $\pm$ 1	26	-6.5 $\pm$ 0.53	11.5 $\pm$ 0.53
RMS Gain Err. (dB)	N/A	N/A	N/A	N/A	< 0.7	1.9	N/A	< 0.42
Gain Control (dB)	N/A	N/A	6	8	6	16	3	N/A
IP1dB (dBm)	-22	-28	-28	-16	0	-25.4	-16.2	-25
Noise Figure (dB)	< 5.5	< 3.4	< 4	< 6.5*	< 4.7	< 3.6	< 6.5	< 4
Power (mW)	10	11	48	32	42	112	19.2	15
Area (mm ²)	0.32	0.3	1.33	0.99*	1.75	1.89	0.4	0.2

[†] Estimated from plot for 6b uncal; * NF results include TRx switches, area includes PA and TRx switches;

Fig. 30. Measured NF of the LNA-Phase-shifter combo for different phase-shifter settings. Different colors represent different coarse settings, as described before in Fig. 18.

Fig. 31. Measured results of the LNA phase-shifter combo, considering a 6-bit quantization. (a) S_{21} vs. frequency. (b) Phase-shift vs. frequency, some states omitted for clarity. (c) S_{21} vs. phase-shift at 29 GHz. (d) RMS gain and RMS phase-errors vs. frequency.

Non-linear measurements were also performed for the combo. Although the IP1dB and IIP3 points are mostly set by the LNA, we tried to observe the influence of each building block of the phase-shifter into both of these metrics. Therefore, we vary each block individually while keeping the other blocks fixed, and measured both the IP1dB and IIP3 across frequency, resulting in Fig. 29. It can be seen that both the attenuator and the 180 $^{\circ}$ -bit blocks' influence on IP1dB and IIP3 is almost negligible. On the other hand, the 90 $^{\circ}$ bit and analog sections

effect are quite considerable. This occurs mostly due to the impedance variation issue. As both 90 $^{\circ}$ bit and analog blocks are based on a purposely impedance mismatch, the load seen by the LNA slightly changes, which causes an impact in the IP1dB and IIP3 of the LNA. Nevertheless, the minimum values obtained were close to the standalone LNA, above -25 dBm for IP1dB and -16.5 dBm for IIP3.

Using the same method as described for the LNA, the NF of the integrated combo was measured, with results shown in Fig. 30. The measurements were performed for multiple phase-shifter settings, representing different load conditions for the LNA. The measured NF for the combo varies from 3.4 to 4 dB across the whole n257-band frequency range, with an average of 3.6 dB. An average 0.6 dB difference between simulated and measured could be explained by the pre-amplifier used in the measurement path as well as modelling imperfections.

E. 6-bit quantization of the LNA-Phase-shifter combo

Once again, to better assess the proposed LNA-Phase-shifter combo with respect to the state-of-the-art, we quantized our continuous phase-shifter into a 6-bit resolution using an external 8-bit DAC. This allows us to evaluate the RMS gain and phase error of the system. For the quantization, we focused into the n257 5G NR band, ranging from 26.5 GHz to 29.5 GHz.

Quantization results are shown in Fig. 31, with all 64 phase-states plotted. The RMS phase-error is kept below 3.2 $^{\circ}$ across the whole n257 band, with a maximum RMS gain error of 0.42 dB, exhibiting state-of-the-art performance. When the single frequency of 28 GHz is considered, the RMS phase-error is 0.7 $^{\circ}$, with an RMS gain error of 0.23 dB. Table II compares the proposed LNA-Phase-shifter combo with the state-of-the-art. The proposed LNA-Phase-shifter combo achieves very competitive performance in every aspect, achieving low gain variation and phase variation under a small area.

VI. CONCLUSION

This article demonstrated the capabilities of VP-APNs to implement high-resolution, large phase-range, and ultra-compact phase-shifters phase-shifters. We analysed the APN

phase-shifting approach, which was used to implement both analog and digitally controlled VP-APNs. In addition to APN based STPS 180° bit section, 360° phase-range with continuous tuning capabilities was demonstrated from 25 to 33 GHz. The addition of attenuators enabled an RMS gain error below 0.6 over the whole frequency range. We then combine the phase-shifter with an LNA to demonstrate the phase-shifter performance within a front-end, achieving 11.5 ± 0.53 dB gain, RMS gain error below 0.42 dB, and RMS phase-error below 3.2° over the n257 band. With a compact area of 0.2 mm² and DC power consumption of 15 mW, the proposed LNA-Phase-shifter combo is suitable for integration in a multi-channel transceiver.

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