A Fast Locking 5.8 - 7.2 GHz Fractional-N Synthesizer with Sub-2 μ s Settling in 22 nm FDSOI

Jeffrey Prinzie, Shuja Andrabi, Christophe Beghein, Changhua Cao, HsinHua Chen, Xiaochuan Guo, Jon Strange and Bernard Tenbroek

Abstract—This letter presents a fast frequency hopping all-digital fractional-N synthesizer with linear frequency tuning word estimation and aggressive type-I and type-II loop settling. It has a linearized DCO allowing wide-band and closed-loop operation and employs digital zero-phase reset to reduce phase transients during switch over due to type-I settling. The DCO gain is equalized by exploiting routing inductances and a hybrid binary-thermometric segmentation provides improved DNL performance for closed loop operation in a 5.8-7.2 GHz range. The circuit was processed in a 22 nm FDSOI technology and achieves a settling time below 2 μ s in a 200 MHz hopping range.

Index Terms—All-Digital PLL, Digitally Controlled Oscillator, Lock Time, Fractional-N Synthesizer

I. INTRODUCTION

LTE and 5G-NR systems dynamically allocate resource blocks (RBs) to each user which change between consecutive sub-frames (2x 500 μ s) resulting in a change in required bandwidth and center frequency. In the past, it has not been possible to switch the Local Oscillator (LO) to the RB mid band frequency between sub-frames since insufficient time is available. The required switching time needs to be less than the Cyclic Prefix (5.2 μ s in LTE). To allow other parts to settle, a <2 μ s synthesizer settling time to a 2.5° accuracy is targeted. The main challenge is to achieve the stringent phase error requirements for LTE and 5G-NR standards within the settling time and tune the hierarchical LC-DCO banks consecutively. This work aims for fast hopping in a 200 MHz or 400 MHz band.

In All-Digital PLLs (ADPLLs), the loop filter is implemented digitally providing real-time digital phase and frequency information allowing enhanced algorithms to assist settling, which was limited in analog counterparts. Early techniques such as divider Zero Phase Reset (ZPR) and loop filter and order gear-shifting have allowed to push settling times towards sub-10 μ s [1]. For fast hopping, DCO tuning word estimation enhances the settling time by presetting the DCO frequency close to target. In [2], estimation with cubic nonlinear compensation has been proposed for Bluetooth systems. This paper however addresses non-linearities in the DCO itself and aims for higher settling accuracy.

Eventually, the settling time can be improved by aggressive loop dynamics scaling which requires accurate phase and

Fig. 1: ADPLL architecture.

Fig. 2: ADPLL settling steps: DCO control values and TDC output phase (post ZPR).

frequency information to limit residual errors when gear-shifting. Hence DTC and ADC assisted TDC based ADPLLs have become popular for fast locking synthesizers. [3]–[5].

II. ADPLL ARCHITECTURE

A. Fast Hopping Method

The architecture of the synthesizer is shown in Fig. 1. It uses a 5 ps Time-to-Digital Converter (TDC) based on two 31-stage ring oscillators coupled together [6], [7] and a 3rd order $\Sigma\Delta$ modulator for fractional synthesis with digital $\Sigma\Delta$ noise cancellation and adaptive TDC gain tracking (LMS). The DCO has 2 banks, a coarse Hopping bank (HOP) and a fine Tracking bank (TRK) with 0.9 MHz and 60 kHz resolution respectively. The process of fast switching between two frequencies is shown in Fig. 2. On power-up, a on-time 2-point calibration is done to estimate the reciprocal HOP bank DCO gain ($K_{DCO} = \Delta HOP / \Delta F_{TW}$) in the targeted band. Upon fast frequency hopping, a linear estimation is made for the next HOP word by calculating $\Delta HOP = \Delta F_{TW} \times K_{DCO}$. However, a correction is required due to non-linearities and drift. A high-bandwidth (20 MHz) type-I loop quickly recovers

J. Prinzie is with KU Leuven, Department of Electrical Engineering (ESAT), Belgium, (e-mail: jeffrey.prinzie@kuleuven.be).

S. Andrabi, C. Beghein, J. Strange and B. Tenbroek are with Mediatek, UK. C. Cao, H. Chen and X. Guo are with Mediatek, Austin (TX), USA.

HOP estimation errors but results in a static phase offset after settling. Before switching to the TRK bank, the TDC phase and HOP words are averaged (16 samples) and a digital offset ZPR is done to prevent transients in the next phase due to the accumulated offsets and phase noise in type-I. The HOP code is also rounded. In a next step, the TRK bank is tuned in a type-I loop with similar averaging and digital ZPR at the end. Upon switch over to low bandwidth (700 kHz) type-II dynamics, the mean TRK word is loaded in the accumulator and a 2nd order IIR filter is activated (4 MHz) to suppress the TDC- and reference noise. Phase averaging and digital ZPR upon switch over limits phase transients (due to offsets) to ensure a smooth transition between all stages, which is essential for high accuracy. Calculating ΔHOP for estimation rather than relying on a lookup table allows to track DCO drifts if hopping occurs regularly. The remaining transients occur due to noise and TDC quantization errors in high-bandwidth operation that result in imperfections during averaging and thus residual errors during loop switching. During fast settling, adaptive TDC gain tracking (LMS) is disabled but $\Sigma\Delta$ noise cancellation is still active.

B. Initial Calibration

Initially, several calibration steps are required. An open loop frequency search is performed to find the mid-band HOP code. Next, the synthesizer locks to the high and low ends of the fast hopping band (FTW_H and FTW_L). The corresponding HOP codes are used to calculate

$$K_{DCO} = \frac{HOP_H - HOP_L}{FTW_H - FTW_L}. \quad (1)$$

A bandwidth (ΔFTW) of 2 or 4 $\times f_{\text{ref}}$ facilitates division. Subsequently, $\Sigma\Delta$ cancellations is enabled and the TDC gain is calibrated through LMS. $\Sigma\Delta$ cancellation is not activated prior to phase lock for clock domain synchronization. Calibration takes 140 μs but is only required once, hence not impacting the fast hopping performance afterwards.

III. DCO CIRCUIT

In order to hop between 2 frequencies, a wide range, linear DCO with fast settling behavior is required. The DCO is based on an active PMOS cross coupled pair with a resonant tail inductor at $2f_0$. For final tracking, fine capacitor cells (TRK) are based on series capacitive degeneration (Fig. 3a) [8]. The cells contain 3 single wire metal fringe field capacitors to achieve small capacitance, extracted through EM simulations, and achieve a 60 kHz resolution but suffer from low $\Delta C/C_{\text{off}}$. Therefore, wide band operation cannot be implemented with fine grained Capacitor DACs (CDACs). The tracking bank has 300 unit cells (18 MHz) to cover drifts.

A. HOP bank frequency control

Wide band frequency tuning is commonly implemented with with CDAC unit cells as shown in Fig. 3b [9]. Larger capacitors often result in improved $\Delta C/C_{\text{off}}$, hence improving the tuning range of the DCO. Two Resistors are required to bias the source/drain nodes to maximize V_{gs} (maximize Q)

Fig. 3: a) Tracking Cells b) Conventional wide tuning range capacitor tuning cells c) Proposed fast settling capacitor tuning cells.

Fig. 4: DCO CDAC segmentation scheme.

when enabled and prevent unwanted activation due to negative voltages ($V_{\text{drain}} < -V_t$) when disabled. This circuit however has an important trade-off between settling time (due to the RC time constant) and off-state quality factor (hence phase-noise).

To avoid this trade-off, a different unit cell was used, as shown in Fig. 3c. The capacitors and center switch are identical but 4 assisting devices are added to drastically improve the switching time without compromising the quality factor of the cell. Two Pull-down NMOS devices are activated when the cell is switched on and quickly pull-down the source/drain voltages of the main switch to maximize V_{gs} . When the cell is deactivated, 2 Pull-up NMOS devices rapidly pull-up the source/drain voltage until the waveform's minimum is $V_{\text{bias}} - V_t$. V_{bias} is chosen between 0 and V_t such that the central switch cannot turn on parasitically due to negative voltages. Once settled, the pull-up devices operate in sub-threshold region and do not degrade the quality factor of the cell. Minimum sized ultra-low V_t devices were used to limit the (nonlinear) assisting device capacitances and 1/f FM noise up-conversion. Furthermore, compared to the conventional unit cell, the device stress when inactive is significantly reduced [10].

B. CDAC segmentation

To provide adequate linearity for the HOP bank to operate closed loop, an optimized segmentation scheme is chosen. The CDAC consists of 13 rows, as shown in Fig. 4. Two Unit cells are used: 1C and 4C cells. Each row contains a 3-bit binary weighted array. Thermometric coding is used from 8C (8C unit = 2 $\times$ 4C cells). The binary array is repeated in each row since the gain ($\Delta f/\text{code}$) still varies across the array which would result in poor DNL performance. Hence, placing repetitive binary weighted cells close to each thermometric coded array significantly improves the DNL of the CDAC and

Fig. 5: CDAC series inductance equalisation.

thus reduces limit cycle noise in closed loop type-I operation. A decoder selects the correct row for the binary weighted cells based on up to which row the thermometric cells are active.

C. DCO gain equalisation

Without considering any series inductance between the CDAC rows, the frequency of the LC tank is

$$f = \frac{1}{2\pi\sqrt{L \cdot (C_0 + n \cdot \Delta C)}} \quad (2)$$

with L the main inductance, C_0 the CDAC off-state capacitance and ΔC the CDAC resolution. The DCO gain is

$$K_{dco} = \frac{\Delta f}{\Delta n} = 4\pi^2 L \cdot \Delta C \cdot f^3 \quad (3)$$

indicating a reduction of K_{DCO} at lower frequencies proportional to f^3 . Hence, a capacitance change ΔC at f_{max} results in a larger Δf than at f_{min} . This intrinsic non-linearity results in large errors during frequency hopping if simple linear interpolation is used, especially if the frequency range is wide. To improve the INL, the series inductance of the top routing between CDAC rows was exploited to linearize the tuning curve forming a distributed inductance (Fig. 5). For capacitor cells furthest away from the main inductor, extra series inductance from the top metal leads is added such that the effective Δf increases which cancels the intrinsic K_{DCO} reduction, if sized appropriately. This excess series inductance was optimized through Electromagnetic simulation by sizing the spacing (mutual inductance, M) of the CDAC routing to control the effective differential series inductance.

IV. MEASUREMENTS

The DCO has a center frequency of 6.3 GHz and a 1.5 GHz tuning range. The DNL and INL error of the DCO and K_{DCO} variability are shown in Fig. 6. The distinct DNL steps are due to the different CDAC rows with excess series inductance. The INL plot shows the deviation from a linear fit, respectively for the entire range and the targeted 200 MHz and 400 MHz calibrated band. The results show a 2.5x - 3x improvement using the proposed equalization method. A similar improvement can be seen for K_{DCO} variability. The DCO gain varies less than 25 % as opposed to 50 % without equalization. Fig. 7 shows the open loop settling behavior of the DCO HOP cells (Fig. 3c) for a 500 MHz HOP bank frequency step. Both rising and falling frequency measurements are shown. The frequency settles to a 35 ppm accuracy within 500 ns after a 500 MHz frequency jump, (63 ppb per LSB), which is sufficiently fast

Fig. 6: DCO DNL error; INL deviation across HOP bank and within 200 MHz and 400 MHz calibrated range; K_{DCO} across the entire tuning range.

Fig. 7: DCO frequency settling time for 500 MHz step.

Fig. 8: Time-domain lock-time measurement.

TABLE I: Comparison Table

	This work	ISSCC14 [3]	JSSC18 [4]	JSSC17 [5]	VLSI19 [1]	ISSCC2018 [2]
CMOS	22 nm	40 nm	65 nm	14 nm	65 nm	16 nm
Ref. Freq. (MHz)	104	32	26	26	100	0.032
Tuning Range (GHz)	5.8-7.2	2.1-2.7	2.0-2.8	2.7	4.7-5	2.1-2.5
In band PN (dBc/Hz)	-108	-90	-103	-113	-110	NA
Integrated PN	115 fs	1.7 ps	530 fs	137 fs	800 fs	1.39 ps
PLL FOM (dB)	-243.9	-236	-245.6	-246	-227	-237.5
Power (mW)	31.1	0.86	0.98	13.4	30	0.92
Bandwidth (MHz)	0.7	0.2	0.6	0.5	2	0.0013
Settling Time (μ s)	1.3 / <0.8 ($\Delta\phi=2.5^\circ$ / $\Delta f=25$ ppm)	16	4.2	20	1.5	<0.1

for the targeted architecture although not limited by the 3.5 ns equivalent intrinsic Q-limited settling time of the tank ($Q \approx 20$).

ADPLL phase settling was measured by switching the synthesizer randomly in a 200 MHz band. No difference is observed for a 400 MHz hopping range since the HOP type-I correction corrects for most of the prediction errors. The settling behavior of the phase and frequency error (at $f_0/2$) is shown in Fig. 8 and a corresponding lock time histogram in Fig. 9, indicating a mean lock time of 1.3 μ s to a 2.5° target (average lock time to 15 ppm frequency error is 0.8 μ s). The time for each consecutive locking state was 0.46 μ s (Type-I HOP) and 0.66 μ s (Type-I TRK). The open and closed loop phase noise of the synthesizer is shown in Fig. 10 ($f_0=6.3$ GHz) with an integrated phase noise (10 kHz-10 MHz) of 115 fs and -108 dBc/Hz in band phase noise, operating at a 104 MHz reference clock. The worst case fractional spur is < -55 dBc. The ADPLL consumes 31.1 mW at a 0.8 V supply voltage achieving a -243.9 dB FOM. A comparison table is shown in Table I with a die photo in Fig. 11.

V. CONCLUSION

A fast settling, low phase noise fractional-N synthesizer was presented with 1.3 μ s lock time. Settling relies on a series of type-I and -II locks with digital ZPR to minimize phase transients between gear-shifting. A gain equalized DCO was presented that uses the excess series inductance in the HOP CDAC to compensate for K_{DCO} variability in order to limit HOP-bank INL estimation errors. A hybrid thermometric-binary segmentation limits HOP bank DNL errors to operate the it in closed loop tuning during fast type-I recovery. The synthesizer has an integrated phase noise of 115 fs and a -243.9 dB FOM.

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Fig. 9: Lock time histogram to a 2.5° target.

Fig. 10: Open and closed loop phase noise at 6.3 GHz.

Fig. 11: Chip photomicrograph.