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The properties, effect and extraction of localized defect profiles from degraded FET characteristics

Michiel Vandemaele^{*†}, Ben Kaczer[†], Stanislav Tyaginov^{†‡§}, Jacopo Franco[†], Robin Degraeve[†], Adrian Chasin[†], Zhicheng Wu^{*†}, Erik Bury[†], Yang Xiang^{*†}, Hans Mertens[†] and Guido Groeseneken^{*†}

^{*}ESAT, KU Leuven, Leuven, Belgium

Email: michiel.vandemaele@imec.be

[†]imec, Leuven, Belgium

[‡]Institute for Microelectronics, TU Wien, Vienna, Austria

[§]Ioffe Physical-Technical Institute, St.-Petersburg, Russia

Abstract—We report simulations of localized defect profiles (DPs), typical for hot-carrier degradation (HCD), with exponential- and step-like shapes. First, we analyze how these localized DPs affect the transistor I - V and model the complex relation between DP and FET degradation by considering the degraded FET as a series circuit of an undegraded transistor (the source side) and a degraded one (the drain side). We also compare how the same DP causes different degradation for changes in the device structure. Second, we use the DP simulations to qualitatively understand the DP dependence on stress voltages in measured FETs and assess how uniquely a DP can be extracted from degraded I - V metrics. The results are of interest for HCD modeling.

Index Terms—Hot-carrier degradation, interface defects, simulations, TCAD.

I. INTRODUCTION

At the microscopic level, MOSFET ageing due to electrical stress is caused by charging of existing and/or creation of new defects in the gate dielectric and at the dielectric/semiconductor interface. For some ageing mechanisms, e.g. bias-temperature instability (BTI), the defects are uniformly distributed along the transistor channel, while for other mechanisms, e.g. hot-carrier degradation (HCD), the defects are typically localized at the drain side. The degree of localization can differ depending on the stress point in the (V_g, V_d) bias space (V_g and V_d are the gate and drain voltage, respectively) [1], [2]. Damage localization complicates the study of HCD.

The degree of HCD localization is often quantified using the apparent localization $L_{app} = (\Delta I_{d,sat,rev} - \Delta I_{d,sat}) / \Delta I_{d,sat}$, a metric which compares the change in saturation drain current in forward mode ($\Delta I_{d,sat}$) to the change in saturation drain current in reverse mode ($\Delta I_{d,sat,rev}$). Forward (reverse) mode means that the source and drain contact are the same (are swapped) in the sense phase as compared to the stress phase, i.e. $V_g = V_d = V_{dd}$, $V_s = 0$ V ($V_g = V_s = V_{dd}$, $V_d = 0$ V), with V_s and V_{dd} the source voltage and supply voltage, respectively. It is easy to see that L_{app} equals 0 for uniform defect profiles (DPs), while values > 0 (< 0) indicate localization at the drain (source). Indeed, the pinch-off region in saturation is located at the drain (source) in forward (reverse) mode and

defects above the pinch-off region do not contribute to first order to the current degradation.

As HCD becomes an increasingly severe MOSFET ageing problem [3], [4], it is important to understand how a localized DP influences a transistor current-voltage (I - V) characteristic for scaled devices. In transistors lacking a bulk contact (e.g. nanowire (NW) FETs), I - V -curves are one of only few characterisation techniques available (e.g. no charge pumping), as noted by Wu *et al.* [5].

Different studies investigated the aspect of localization in electrical degradation. Gautam *et al.* examined the effect of localized charges on NW FETs using simulations with a focus on RF figures of merit [6] and on the circuit impact for a CMOS inverter [7]. Kaczer *et al.* [8] identified lateral defect localization as a source of the increased time-dependent variability for HCD as compared to BTI in the case of nFinFETs. Bottini *et al.* [9] simulated the ΔV_{th} versus charge relation for different step DPs for a particular FET as part of a time-dependent variability study. Haddara *et al.* [10] proposed to interpret the channel of a locally damaged FET as consisting of a lumped defect-free and defective region. Based on this, they presented a method to characterize both regions, relying on ohmic conductance measurements for long ($L_g \sim 1$ μ m) channel FETs. More recently, other lateral defect profiling techniques were developed to extract DPs induced by hot-carriers (HCs) from an I_d - V_d (Mamy Randriamihaja *et al.* [11] and Wang *et al.* [12]) or multiple I_d - V_g s (Yun *et al.* [13]). Exploiting the information in time-dependent variability, Yu *et al.* [14] identified typical locations of different HC-induced traps in finFETs, both along the device width (position in the top or side wall of the fin) as well as along the lateral channel direction.

We study the relation between localized DPs and changes in the I - V for scaled devices ($L_g = 40 - 200$ nm) and we assess how uniquely a DP can be extracted from degraded I - V metrics. To this end, we perform TCAD (technology computer-aided design) simulations of idealized profiles and compare them to measured degradation. The obtained understanding is of interest for distribution function-based modeling of HCD [15]–[17].

Fig. 1. Exponential defect profiles (DPs) used as input in the simulations for different values of γ (DP extent from the drain), plotted here for a device with gate length $L_g = 76$ nm. The DPs in the figure are normalized by their average charge density $\langle N_{it} \rangle$.

II. METHODOLOGY

We simulate exponential (Fig. 1, analytical expression from Kasemsuwan *et al.* [18]) and step (Fig. 2) interface DPs N_{it} , described respectively by:

$$N_{it}(x) = N_{it,0} \exp\left(\frac{x - L_g}{\gamma}\right) \quad (1)$$

$$N_{it}(x) = \begin{cases} N_{it,0} & \text{for } x \geq L_g - \gamma \\ 0 & \text{otherwise.} \end{cases} \quad (2)$$

Here, L_g is the gate length, x the coordinate in the channel direction ($x = 0$ being the source and $x = L_g$ being the drain), γ the localization parameter characterising the DP extent from the drain and $N_{it,0}$ the height of the DP. Following Bottini *et al.* [9], we do not vary $N_{it,0}$, but the average charge density $\langle N_{it} \rangle$ of the DP. This allows assessing the influence on FET degradation of the localization only by varying γ . Indeed, DPs with the same $\langle N_{it} \rangle$ and varying γ have the same total charge, which is not true for DPs with the same $N_{it,0}$ and varying γ . Expressing $N_{it,0}$ as function of $\langle N_{it} \rangle$ (and γ), we obtain:

$$N_{it,0} = \frac{\langle N_{it} \rangle}{\frac{\gamma}{L_g} \left(1 - \exp\left(-\frac{L_g}{\gamma}\right)\right)} \quad (3)$$

$$N_{it,0} = \frac{L_g}{\gamma} \langle N_{it} \rangle, \quad (4)$$

for the exponential (3) and the step (4) DPs respectively.

We simulate both virtual planar nFETs and a fabricated NW nFET. The virtual FETs are used to gain understanding of how a localized DP influences the FET I - V (Section III-A), while the fabricated FET is used to determine the HC-induced DP from measured degradation (Section III-B).

The virtual FETs have a structure consisting of a channel region covered by SiO_2 as gate oxide and connected to the source/drain contact via a source/drain extension region (Fig. 3a). Three types of virtual FETs (vFET1-vFET3) were created,

Fig. 2. Step DPs used as input in the simulations for different values of γ (DP extent from the drain), plotted here for a device with gate length $L_g = 76$ nm. The DPs in the figure are normalized by their average charge density $\langle N_{it} \rangle$.

TABLE I
OVERVIEW OF DIFFERENT PROPERTIES OF THE SIMULATED PLANAR VIRTUAL FETs (vFETs).

Name	L_g (nm)	t_{ox} (nm)	N_A (cm^{-3})	$N_{A,halo}$ (cm^{-3})
vFET1	76	2.5	10^{18}	2×10^{18}
vFET2	76	1	$10^{17}/10^{18}/10^{19}$	NA
vFET3	40/55/76/ 105/145/200	2.5	10^{18}	NA

differing in oxide thickness t_{ox} and the presence/absence of halo doping $N_{A,halo}$ (Table I). In vFET2 and vFET3, the channel doping and the gate length were varied respectively, to investigate how these properties influence the sensing of the DP. The fabricated NW nFET has a gate length of 28 nm and a channel diameter of 8 nm (Fig. 3b-c). The fabrication of the NW FET is described in Mertens *et al.* [19], [20]. HC measurements of the NW FET were done by Chasin *et al.* [1] for many $(V_{g,stress}, V_{d,stress})$ bias combinations in the range $V_{g,stress} \in [0.4, 1.9]$ V and $V_{d,stress} \in [0.1, 2.2]$ V, i.e. over the full $(V_{g,stress}, V_{d,stress})$ bias space.

TCAD simulations are done in Minimos-NT [21] using the drift-diffusion scheme. The simulated structure is 2D for the virtual FETs (they are planar) and 3D for the NW FET. For the virtual FETs, the Minimos-NT “MM6” mobility model [22] was employed, while for the NW FET the simulated I - V s of the defect-free device were calibrated to the measured ones. The interface defects are modeled as permanently, negatively charged in the simulations and their electrostatic influence and mobility degradation are taken into account. We simulate full I - V s in linear ($V_d = 0.05$ V), saturation ($V_d = 0.9$ V) and saturation reverse ($V_s = 0.9$ V) modes. We study the apparent localization L_{app} (evaluated at $V_g = 0.9$ V) and the threshold voltage shift ΔV_{th} . The threshold voltage is extracted using the max- g_m method for the pristine device ($V_{th,0}$) and using the constant current method at the current of $V_{th,0}$ to extract ΔV_{th} for the degraded devices. Simulations were done at $T = 25$ °C for the virtual devices and at $T = 125$ °C for the NW FET.

Fig. 3. a) Simulated structure of the virtual planar transistor (vFET1-vFET3). b)-c) TEM image and simulated structure of the fabricated nanowire FET ($L_g = 28$ nm, $\phi = 8$ nm).

III. RESULTS AND DISCUSSION

We first study theoretically how a localized DP influences a transistor I - V and then use the simulations to estimate the DP in FETs subjected to HC stress.

A. Understanding localized defect profiles

We start with simulations of the threshold voltage shift ΔV_{th} caused by the step (Fig. 4) and the exponential (Fig. 5) interface DPs in vFET1 for different values of γ and $\langle N_{it} \rangle$. Symbols of the same color in Figs. 4 and 5 are for profiles of constant interface states charge and the dashed lines give the degradation for the same interface states charge, but uniformly distributed along the channel. For both DPs, we observe that for constant interface states charge the degradation depends on the localization (γ) of the charge. For small γ and $\langle N_{it} \rangle$, the DP causes almost no ΔV_{th} . With increasing $\langle N_{it} \rangle$, the threshold voltage shift of the localized profile becomes higher than for the same charge with a uniform profile. This effect is more pronounced for the step DP compared to the exponential DP. The herewith observed trends for $\Delta V_{th}(\gamma, \langle N_{it} \rangle)$ are similar to those reported by Bottini *et al.* (Fig. 5 in [9]).

To better understand the $\Delta V_{th}(\gamma, \langle N_{it} \rangle)$ function, we use the EKV compact model [23] and consider the degraded FET as a series combination of two EKV FETs (upper part of Fig. 7), similar to Haddara *et al.* [10], Wu *et al.* [5] and Chen *et al.* [24]. For simplicity, we focus on the step DP. The left (right) FET of the series combination then corresponds to the undegraded (degraded) part of the step with gate length $L_g = L_{total} - \gamma$ ($L_g = \gamma$). We determine the voltage V_x of the node connecting the drain of the left FET to the source of the right FET by requiring that the current through both FETs is equal. From the fit of the I - V of the pristine device (inset of Fig. 6), the three EKV parameters n (subthreshold swing factor), V_{th} and β ($\beta = \mu C_{ox} W / L_g$) are obtained (μ is the mobility, C_{ox} the oxide capacitance per unit area and W the

Fig. 4. Simulated threshold voltage shift ΔV_{th} for the step interface DP in vFET1 as a function of the DP parameters γ and $\langle N_{it} \rangle$. Symbols of the same color have equal interface states charge in the channel and the dashed lines represent the degradation caused by the same interface states charge uniformly distributed over the channel. The full lines model the simulated data using a series circuit of two EKV FETs. The letters a-d refer to Fig. 7. For a localized interface DP, the same charge leads to different degradation (ΔV_{th}) depending on the localization (i.e. γ).

Fig. 5. Simulated threshold voltage shift ΔV_{th} for the exponential interface DP in vFET1 as function of the DP parameters γ and $\langle N_{it} \rangle$. Symbols of the same color have equal interface states charge in the channel and the dashed lines represent the degradation caused by the same interface states charge uniformly distributed over the channel. The lines connecting the symbols are a guide to the eye only. For a localized interface DP, the same charge leads to different degradation (ΔV_{th}) depending on the localization (i.e. γ).

device width). The EKV parameters for the left (L) and the right (R) FETs follow then from the pristine EKV parameters:

$$V_{th,L} = V_{th} \quad V_{th,R} = V_{th} + \frac{qN_{it,0}}{C_{ox}} \quad (5)$$

$$\beta_L = \frac{L_{total}}{L_{total} - \gamma} \beta \quad \beta_R = \frac{L_{total}}{\gamma} \beta \quad (6)$$

$$n_L = n_{\infty} + \frac{C}{(L_{total} - \gamma)^2} \quad n_R = n_{\infty} + \frac{C}{\gamma^2} \quad (7)$$

These transformations correspond to a threshold voltage shift caused by uniform charge in the right FET and an increase of the β -factor due to the geometrical shrinkage of the left

Fig. 6. Dependence of the subthreshold swing factor n in the EKV model on the gate length L_g for vFET1. The line is a fit to the simulated (TCAD) data using the model $n = n_\infty + C/L_g^2$ [25]. The inset shows the EKV-fit for the simulated I - V for $L_g = 76$ nm.

and right FETs compared to the total device length [10]. Additionally, the n -factor of both FETs increases because of geometrical reasons. The dependence of n on L_g was obtained by simulating I - V s of vFET1 for different L_g and fitting the obtained n using the relation $n = n_\infty + C/L_g^2$ following Pouydebasque *et al.* [25], with C and n_∞ treated as fitting parameters (Fig. 6).

The above series model reproduces the shape of the $\Delta V_{th}(\gamma, \langle N_{it} \rangle)$ function for the step DP well (Fig. 4, full lines). For small γ , the right FET is very short, has a large subthreshold swing and almost no gate control (Fig. 7a). Because it is short, its β -factor is also high, meaning that it can conduct a lot of current. Despite the fact that the right FET is degraded, the current is limited by the left, undegraded FET and as a consequence we observe almost no ΔV_{th} . With increasing γ , the subthreshold swing of the right FET improves and the current it can conduct decreases because its β -factor decreases (Fig. 7b-c). The degraded I - V is now dominated by the left FET at low V_g , by the right (degraded) FET at higher V_g and a threshold voltage shift is observed. For large γ , the degraded I - V is completely dominated by the right FET (Fig. 7d). The left FET is now very short, has a large subthreshold swing factor, conducts a high current and consequently does not influence the I - V of the full device. The ΔV_{th} is now given by $qN_{it,0}/C_{ox}$ as for the case of uniform interface states charge.

Using the TCAD simulations, we also study the influence of changes to the device structure on the sensing of the DP. First, we simulate ΔV_{th} for different values of γ and $\langle N_{it} \rangle$ for a step DP in three vFET2-instances which are, except for their channel doping, identical (Fig. 8). For small values of γ , we observe that the same DP leads to higher degradation for a higher channel doping and this effect is more pronounced for larger $\langle N_{it} \rangle$. For large values of γ , the difference between the three channel dopings disappears. Note that the ΔV_{th} values in

Fig. 7. Modeling of the degraded I - V of the planar FET with step defect profile in Fig. 4 using two EKV models placed in series (one for the undegraded and one for the degraded part of the FET). The $(\gamma, \langle N_{it} \rangle)$ values corresponding to the four panels are indicated with letters (a-d) in Fig. 4.

vFET2 (Fig. 8) are smaller than in vFET1 (Figs. 4-5) because the gate oxide is thinner in the former. This thinner gate oxide was used in vFET2 to have sufficient electrostatic gate control for the three channel dopings.

Second, we simulate ΔV_{th} for different values of γ and $\langle N_{it} \rangle$ for a step DP in six vFET3-instances with different gate length L_g . In reality, FETs with varying L_g fabricated in the same technology might differ in e.g. oxide thickness to optimize the electrostatics for every L_g . Such optimizations were not applied in our simulation to be able to isolate the effect of the L_g scaling only on the ΔV_{th} sensing. In other words, the six vFET3-instances in our simulation are, except for their gate length, identical. The same step DP (with same γ) was used for every L_g , meaning that the charge was identical for the six devices (but not $\langle N_{it} \rangle$). We observe that a same localized charge leads to more degradation for shorter L_g (Fig. 9). This effect is most pronounced for the smaller values of γ and decreases for larger values of γ .

Fig. 8. Simulated ΔV_{th} caused by step DPs for three instances of vFET2 with different channel doping (otherwise identical). For small values of γ , the same DP leads to more degradation if the channel doping is higher.

Fig. 9. Simulated ΔV_{th} caused by step DPs for six instances of vFET3 with different channel length (otherwise identical). The microscopic localization γ (and so the total interface charge Q_{it}) was identical in the six devices. The same DP leads to more degradation if the channel length is smaller. This effect is most pronounced for the smaller values of γ and decreases for larger values of γ .

B. Extraction of localized defect profiles

We now investigate how the DP simulations from the previous section can be used to comprehend DPs in real devices measured after HC stress. The DP simulations constitute a map from microscopic DP parameters (e.g. γ , $\langle N_{it} \rangle$) to macroscopic, measurable quantities (e.g. ΔV_{th}). This map can be built for any fabricated device by simulating DPs with a certain analytical form for a wide value range of the microscopic DP parameters and extracting the resulting macroscopic degradation from the I - V . These simulations can then be used as a look-up table to find back the best DP for a certain measured degradation.

We built this look-up table for the measured NW FET by using the step DP shape. For every stress condition ($V_{g, stress}$, $V_{d, stress}$), we then selected the DP which best reproduces both the measured ΔV_{th} and L_{app} by minimizing the squared difference between their measured and simulated values (Figs. 10 and 11). The evolution of the extracted microscopic DP parameters γ and $\langle N_{it} \rangle$ as function of the stress voltages can be visualized as a result (Figs. 12 and 13). We see that the

Fig. 10. Fit of simulated to measured ΔV_{th} for a fabricated nanowire (NW) nFET. For every bias point ($V_{g, stress}$, $V_{d, stress}$), the step DP was selected which best reproduces the measured ΔV_{th} and apparent localization (see Fig. 11).

Fig. 11. Fit of simulated to measured apparent localization ($L_{app} = (\Delta I_{d, sat, rev} - \Delta I_{d, sat}) / \Delta I_{d, sat}$) for a fabricated NW nFET. For every bias point ($V_{g, stress}$, $V_{d, stress}$), the step DP was selected which best reproduces the measured ΔV_{th} (see Fig. 10) and apparent localization.

average defect density increases for increasing $V_{d, stress}$ and $V_{g, stress}$. We observe a decrease in γ (i.e. a more localized DP) for increasing $V_{d, stress}$.

We tried to obtain an idea of how unique the selected step DPs in Figs. 12 and 13 are. To this end, we set up a range of typical measured values for ΔV_{th} and L_{app} in the fabricated NW FET. For all these (ΔV_{th} , L_{app}) combinations, we selected the step DPs which reproduce this ΔV_{th} and L_{app} within a certain tolerance, namely $|\Delta V_{th} - \Delta V_{th, step DP}| < 3$ mV and $|L_{app} - (L_{app})_{step DP}| < 0.2$ (i.e. we selected more than only the best match between the input and simulated $\Delta V_{th}/L_{app}$). The standard deviation of the $\langle N_{it} \rangle$ and γ of the selected DPs then give a measure for the spread in step DPs resulting in the same ΔV_{th} and L_{app} .

Following this procedure, we observe the largest standard

Fig. 12. Evolution of the average defect density $\langle N_{it} \rangle$ versus $V_{g, stress}$ and $V_{d, stress}$ for the fabricated NW nFET as obtained from the fit in Figs. 10 and 11

Fig. 13. Evolution of the microscopic localization γ versus $V_{g, stress}$ and $V_{d, stress}$ for the fabricated NW nFET, as obtained from the fit in Figs. 10 and 11.

deviation of $\langle N_{it} \rangle$ for small values of ΔV_{th} and L_{app} (Fig. 14). The largest standard deviation of γ is observed for small values of L_{app} (Fig. 15). These observations imply that it is most difficult to uniquely determine $\langle N_{it} \rangle$ and γ of a step DP for the above combinations of ΔV_{th} and L_{app} . Fig. 15 helps to understand the scatter in the extraction of γ for $V_g = 1.9$ V and low V_d in Fig. 13. From Fig. 11, we see that these stress conditions have a small L_{app} and therefore a larger uncertainty (σ) for the extraction of γ . Note that the white regions in Figs. 14 and 15 are $(\Delta V_{th}, L_{app})$ combinations for which there exists no suitable step DP. We conclude it is not possible to have a step DP leading to a large ΔV_{th} and a large L_{app} at the same time. This trend is also observed in the measured data, which are represented by the black dots in the figure.

Fig. 14. Standard deviation σ of the $\langle N_{it} \rangle$ -values of all $(\gamma, \langle N_{it} \rangle)$ pairs for step DPs in the fabricated NW nFET producing the given ΔV_{th} (up to 3 mV) and the given apparent localization (up to 0.2). This gives an idea of the uniqueness or non-uniqueness of a step DP leading to a certain $(\Delta V_{th}, L_{app})$. The black dots are the measured values for the NW nFET.

Fig. 15. Standard deviation σ of the γ -values of all $(\gamma, \langle N_{it} \rangle)$ pairs for step DPs in the fabricated NW nFET producing the given ΔV_{th} (up to 3 mV) and the given apparent localization (up to 0.2). This gives an idea of the uniqueness or non-uniqueness of a step DP leading to a certain $(\Delta V_{th}, L_{app})$. The black dots are the measured values for the NW nFET.

IV. CONCLUSIONS

We performed simulations of localized defect profiles (DPs) in virtual planar nFETs and in a nanowire (NW) nFET calibrated against a fabricated structure. We observe that a given interface states charge leads to different degradation depending on its localization and we modeled the relation between DP and I - V -degradation using a series circuit of two FETs represented by the EKV model. We used the simulations to estimate DPs in a fabricated and hot-carrier (HC) stressed NW FET. We found that uniquely determining the average defect density of the DP is the most difficult for small values of the measured threshold voltage shift ΔV_{th} and apparent localization L_{app} and that uniquely determining the extent of

the DP from the drain is the most difficult for small values of the measured L_{app} . The results are of importance for (distribution function-based) modeling of HC degradation.

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