A Near-Infrared Enhanced Silicon Single-Photon Avalanche Diode with a Spherically Uniform Electric Field Peak

Edward Van Sieleghem[1,2], Andreas Süss[3], Pierre Boulenc[4], Jiwon Lee[1],
Gauri Karve[1], Koen De Munck[1], Celso Cavaco[1], Chris Van Hoof[1,2]

[1]Imec, 3001 Leuven, Belgium

[2]Department of Electrical Engineering, Katholieke Universiteit Leuven, 3001 Leuven, Belgium

[3]OmniVision Technologies, Santa Clara, CA 95054 USA

[4]Gpixel NV, 2018 Antwerpen, Belgium

Abstract

A near-infrared (NIR) enhanced silicon single-photon avalanche diode (SPAD) fabricated in a customized 0.13 µm CMOS technology is presented. The SPAD has a depleted absorption volume of approximately 15 µm × 15 µm × 18 µm. Electrons generated in the absorption region are efficiently transported by drift to a central active avalanche region with a diameter of 2 µm. At the operating voltage, the active region contains a spherically uniform field peak, enabling the multiplication of electrons originating from all corners of the device. The advantages of the SPAD architecture include high NIR photon detection efficiency (PDE), drift-based transport, low afterpulsing, and compatibility with an integrated CMOS readout. A front-side illuminated device is fabricated and characterized. The SPAD has a PDE of 13% at wavelength 905 nm, an afterpulsing probability $< 0.1\%$ for a dead time of 13 ns, and a median dark count rate (DCR) of 840 Hz at room temperature. The device shows promising performance for time-of-flight applications that benefit from uniform NIR-sensitive SPAD arrays.

Keywords: Single-photon avalanche diode (SPAD), CMOS integrated circuit, near-infrared enhanced SPAD, spherically uniform field peak, time-of-flight (ToF).

Corresponding author: Edward.Vansieleghem@imec.be

1 Introduction

Single-photon avalanche diodes (SPADs) can resolve individual photons with high temporal accuracy. In recent years, various imaging systems exploiting the time-resolving features of SPADs have been demonstrated with increasing spatial resolution. Prominent application domains of SPADs include time-of-flight (ToF) imaging [1–3] and biophotonics [4–6]. In particular, the use of ToF SPAD imagers for range-finding has gained increased interest from the automotive and mobile industries [7, 8]. The application benefits from the integration of SPADs into uniform arrays. Infrared illumination
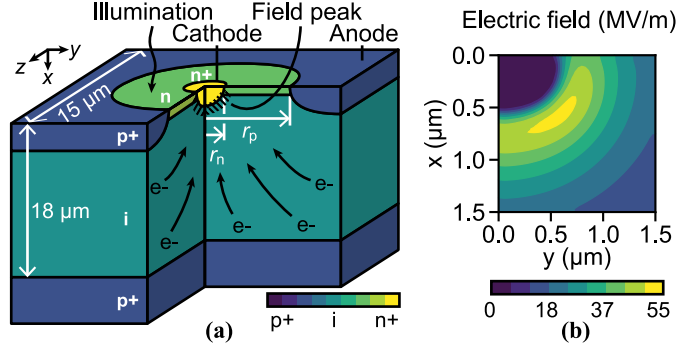
Figure 1: (a) Doping profile schematic of the SPAD. Electrons (e-) move towards the field peak (dashed area) by drift. (b) Numerical simulation of the electric field near the cathode for $V_e = 3.5$ V. The top interface and centerline coincide with $x = 0$ µm and $y = 0$ µm, respectively.

is preferred for the reduction of solar background noise and for complying with eye-safety regulations [9].

Silicon manufacturing technologies provide a well-established and inexpensive platform for the integration of SPADs. A disadvantage of silicon is the low absorption coefficient in the near-infrared (NIR) spectrum. To optimize the photon detection efficiency (PDE), red and NIR-enhanced silicon SPADs incorporate thick absorption regions using standard [8, 10–18] or customized [19–21] technologies. Carriers generated in the absorption volume move towards an electric field peak where they can trigger avalanche breakdown.

Depleting a thick absorption volume in a SPAD potentially results in a high operating voltage, a high excess bias, and sensitivity to fabrication process nonuniformity [19]. Such depleted SPAD may require a large guard ring or suffer from junction-edge effects, making integration into dense arrays difficult [22, 23]. Alternatively, if the absorption volume is not depleted, charge diffusion degrades the timing performance.

In this work, we present a front-side illuminated (FSI) NIR-enhanced silicon SPAD with a depleted absorption volume and an electric field peak enforced by field-line crowding [24]. The depleted SPAD can be integrated into arrays with high PDE and low sensitivity to process nonuniformity.

2 SPAD device

The doping profile of the NIR-enhanced SPAD is presented in Fig. 1(a). The SPAD is formed in an 18 µm-thick intrinsic epitaxial (epi) layer on top of a p+ substrate by using a customized 0.13 µm silicon CMOS technology. The cathode consists of an n+ region in the shape of a half-sphere with radius $r_n = 0.6$ µm. The anode is formed by a p+ region concentrically enclosing the cathode with an inner radius $r_p = 5$ µm. A shallow n-type implantation is present between the cathode and the anode. The device has a pitch of 15 µm.

The SPAD operates at a reverse bias equal to the sum of the excess bias V_e and the breakdown voltage V_{bd}. At the operating voltage, the epi layer and the shallow n-type region are fully depleted. As a result, the SPAD contains a depleted absorption volume of nearly 15 µm × 15 µm × 18 µm in which an electric field is present. Electrons generated in the absorption region move efficiently towards the cathode by drift, without requiring additional assistance [25]. The significant thickness of the absorption volume and the drift-based transport enhance the NIR sensitivity and timing performance of the detector, respectively. The presented FSI SPAD is not isolated from the substrate, and diffusion from the substrate affects the timing performance. Besides, the device has no physical isolation to prevent crosstalk.

A spherically uniform electric field peak is present near the cathode, as visualized in Fig. 1(b) for $V_e = 3.5$ V. The active high-field region has a diameter of $d_{act} = 2$ µm. Most electrons entering the uniform field peak have a high probability of triggering avalanche breakdown. This feature resembles
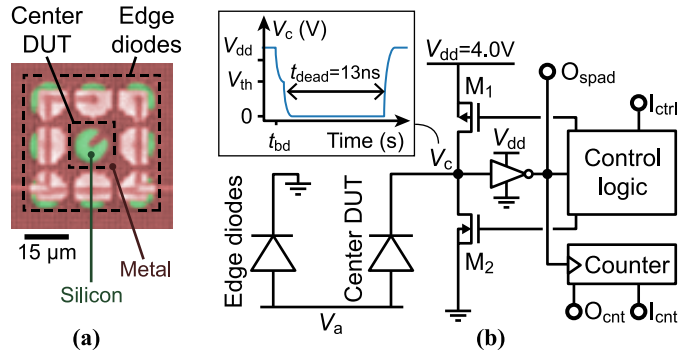
2

Figure 2: (a) Micrograph of the diode array. Silicon and metal are artificially colored green and red, respectively. (b) Digital SPAD module. The inset shows the nominal V_c response for an avalanche event.

electrical microlensing and greatly enhances the PDE [26, 27]. Additionally, the small active volume enables a low afterpulsing probability. The field peak is enforced by field-line crowding as opposed to ionized doping atoms. As a result, the device uniformity across a wafer has a low sensitivity to doping nonuniformity. The cathode has the shape of a halve-sphere to achieve the spherical uniformity of the field. The radius r_n of the cathode largely determines V_{bd} and the magnitude of the field in the epi at V_{bd}. In this work, the radius is $r_n = 0.6$ µm, resulting in $V_{bd} > 60$ V and a sufficient field in the 18 µm epi to achieve 300 ps NIR timing resolution. The breakdown voltage is relatively high and can lead to significant power consumption. Reducing V_{bd} is possible by making r_n smaller at the cost of slower electron transport, which is acceptable if the epi thickness is reduced.

The field peak is locally reduced on the top interface by the shallow implantation. Carriers generated on the interface have a lower probability of multiplying, reducing the dark count rate (DCR). This feature resembles the field redistribution techniques used in power semiconductor devices [28]. The dose of the shallow implant is high enough to redistribute the field on the interface but low enough to not negatively affect the PDE.

3 Test system

The device is integrated into a 3×3 array, as illustrated in Fig. 2(a). The cathodes are electrically isolated by potential barriers, whereas the anodes and substrate are electrically connected. The central diode is the device under test (DUT). Two types of test modules are considered. Firstly, wired-out modules are used for current-voltage (IV) characterization. Herein, the DUT cathode is directly connected to a source measurement unit. Secondly, digital SPAD modules are used for avalanche event characterization. Herein, the DUT cathode is connected to an integrated circuit as discussed further.

Fig. 2(b) illustrates the monolithic integrated circuit of a digital SPAD module. The circuit is isolated from the substrate by a buried n-well process. The cathode of the DUT is connected to two transistors and a CMOS inverter. The output of the inverter is connected to a quench/recharge control circuit, a 30-bit asynchronous counter, and a buffered output pad O_{spad}. The control circuit determines whether the cathode voltage V_c is pulled to the supply voltage $V_{dd} = 4.0$ V or ground by turning on transistor M_1 or M_2, respectively. In the idle state, both M_1 and M_2 are off, and the relative sizing of the transistors ensures $V_c \approx V_{dd}$.

The anode voltage V_a is configured such that the reverse bias of the DUT idles above the breakdown voltage. The excess bias is defined as $V_e = V_a + V_{dd} - V_{bd}$. During nominal operation, V_e is selected between $V_{dd} - V_{th}$ and V_{dd}, with inverter threshold voltage $V_{th} = V_{dd}/2$. The inset of Fig. 2(b) shows the nominal cathode response for an avalanche event at time t_{bd}. Initially, transistor M_1 is off and acts as a quenching load. When an avalanche event triggers a breakdown current, V_c reduces below V_{th} due to passive quenching. The output of the inverter flips, and transistor M_2
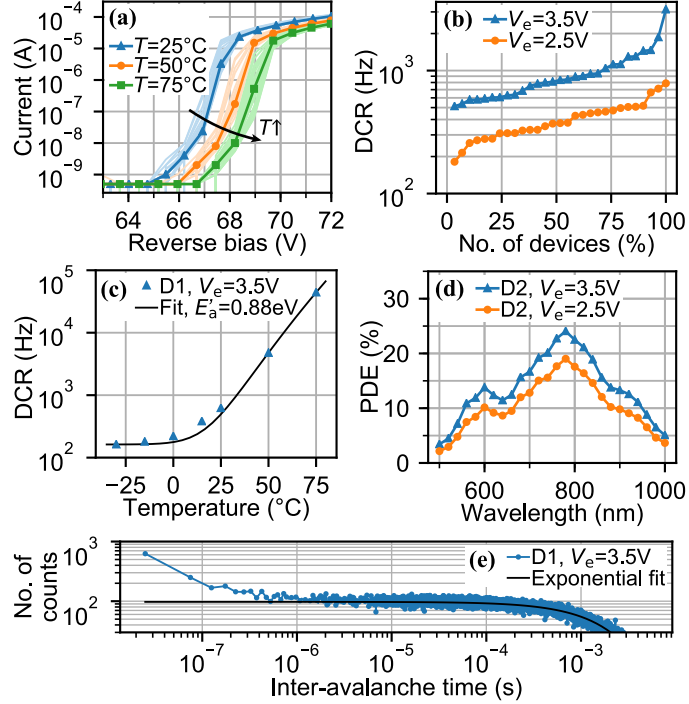
Figure 3: Characterization results of the SPAD. (a) IV characteristics in the dark versus T with a resolution of 1 nA. The median IV is highlighted. (b) DCR distribution for $T = 25$ ˚C. (c) DCR versus T for device D1. (d) PDE versus wavelength for device D2 and $T = 25$ ˚C. (e) Inter-avalanche time histogram with time-bin 50 ns obtained from 3.5×10^6 events in device D1.

is turned on by the control circuit. Consequently, the cathode is pulled to the ground, quenching the avalanche current. After a fixed dead time of $t_{\mathrm{dead}} = 13$ ns, M_1 is briefly turned on and M_2 is turned off by the control circuit. These actions pull the cathode back to V_{dd}. Each rising edge of the inverter output increments the counter value at O_{cnt} and produces a signal at O_{spad}. The counter is only incremented if $V_e > V_{\mathrm{dd}}/2$. This boundary condition is used for calibrating V_e. Throughout this work, the edge diodes are biased below V_{dd}. Crosstalk is prevented since these diodes are not in breakdown and contain a similar field as the DUT.

4   Results

The quasi-static IV characteristics of 29 devices on a wafer have been measured. Fig. 3(a) presents the median dark current as a function of the reverse bias and temperature T. The median breakdown voltage is 67.25 V for $T = 25$ ˚C with a temperature coefficient of 34 mV/K. The breakdown voltages of all devices vary by less than 1% from the median. The median dark current activation energy is $E_{\mathrm{a}} = 0.67$ eV near V_{bd} and $T = 25$ ˚C, which is consistent with Shockley-Read-Hall generation and diffusion. The median reverse resistance above breakdown equals $R_{\mathrm{r}} = 44$ kΩ for $T = 25$ ˚C. The resistance is higher than typical SPADs, and likely results from space-charge and substrate resistances. Numerical simulations predict a junction capacitance < 0.5 fF, enabling a moderate overall RC-delay constant for quenching.

Fig. 3(b) shows the cumulative DCR distribution of 29 devices for $T = 25$ ˚C. The median DCR is 840 Hz for $V_e = 3.5$ V. Devices D1 and D2 with near-median DCR are characterized further. Fig. 3(c) shows the DCR temperature dependence of device D1 for $V_e = 3.5$ V. The data are fitted by the sum of two terms. The first term is constant and equal to 162 Hz, which is consistent with trap-assisted tunneling. The second term is exponential and given by $A \times \exp(-E'_{\mathrm{a}}/(k_{\mathrm{b}}T))$ with activation energy $E'_{\mathrm{a}} = 0.88$ eV, Boltzmann constant k_{b}, and fitting parameter A. This term is

Table 1: Comparison of NIR-sensitive silicon SPADs.

	This work	[19] 2021	[8] 2020	[14] 2016	[18] 2012
Technology	130nm	custom	90nm	180nm	90nm
$V_{\mathrm{bd}}+V_{\mathrm{e}}$ (V)	67.3+3.5	30+20	20+3	20.5+5	15+2.4
DCR (Hz)	840	3300	3	125	1000
PDE@905nm (%)	13	20‡	20.5	4.3	13‡
Pitch/d_{act} (µm)	15/2	250/50	10/5	25/14	-/6.4
P_{ap} (%)	< 0.1	2	0.1	-	0.4
Jitter FWHM @λ (ps@nm)	300* @905	95 @820	173 -	- -	51 @470†

*Predicted by Monte-Carlo simulations,
†Not representative for NIR applications,
‡Assuming fill-factor = 1.

consistent with SRH generation and diffusion, and it is dominant for $T > 0$ °C. The inequality $E_{\mathrm{a}} < E_{\mathrm{a}}'$ indicates that the dark carriers generated by SRH on the interface have a lower probability of contributing to the DCR due to the locally redistributed field. The DCR related to diffusion can be reduced by optimizing the doping profile and by removing the substrate.

Fig. 3(d) illustrates the PDE obtained by illuminating device D2 with a homogeneous monochromatic source. The PDE at wavelength $\lambda = 905$ nm is 13% for $V_{\mathrm{e}} = 3.5$ V. The large depletion region and uniform field peak enable the high NIR sensitivity. Dummy metal layers, serving no functional purpose in the FSI device, limit the PDE by reflecting approximately half of the incident light on the DUT.

The afterpulsing probability P_{ap} of device D1 is calculated based on the time difference between consecutive avalanche events [29]. Fig. 3(e) shows an inter-avalanche time histogram for $V_{\mathrm{e}} = 3.5$ V, $T = 25$ °C, and $t_{\mathrm{dead}} = 13$ ns. The histogram is fitted by an exponential function corresponding to Poisson distributed events. The area above the fit corresponds to afterpulsing with $P_{\mathrm{ap}} < 0.1\%$. Very few carriers are trapped in the small active region during avalanche events.

The charge transport in the absorption volume is based on drift. However, electrons generated in the substrate can also diffuse towards the cathode. Numerical simulations predict a NIR full width at half maximum (FWHM) timing resolution < 300 ps and a diffusion tail < 2 ns. The resistance R_{r} may negatively affect the timing performance. Besides, due to the lack of physical isolation between neighboring devices, crosstalk is significant. However, the edge diodes and DUT contain similar electric fields during operation, and there is no indication that the presented results are biased by crosstalk.

5 Conclusion

Table. 1 provides a comparison of NIR-sensitive silicon SPADs. Despite the degradation of the PDE by metal reflections, the presented FSI device achieves a competitive NIR PDE. Additionally, P_{ap} exceeds the state-of-the-art [8] due to the small active region. Unlike typical SPADs with thick depleted absorption volumes [19], the device is compatible with a standard CMOS readout (enabled by $V_{\mathrm{e}} = 3.5$ V), and the pitch is not limited by a guard ring. The lack of isolation negatively affects the NIR timing resolution and crosstalk of the FSI SPAD, as is the case for other nonisolated SPADs [14,18]. However, since the absorption volume is depleted, back-side illumination (BSI) and deep-trench isolation (as in [8]) can greatly improve isolation while enhancing the PDE and timing resolution. Additionally, $V_{\mathrm{bd}} < 40$ V and a lower R_{r} can be obtained when reducing the epi thickness and optimizing the doping. All considered, the presented device shows promise for ToF applications. The fabrication of a BSI device with a monolithic readout circuit is ongoing. The timing jitter and crosstalk will also be characterized in the future.

5

References

[1] K. Morimoto, A. Ardelean, M.-L. Wu, A. C. Ulku, I. M. Antolovic, C. Bruschini, and E. Charbon, "Megapixel time-gated SPAD image sensor for 2D and 3D imaging applications," *Optica*, vol. 7, no. 4, pp. 346–354, Apr. 2020, doi: 10.1364/OPTICA.386574.

[2] R. K. Henderson, N. Johnston, S. W. Hutchings, I. Gyongy, T. Al Abbas, N. Dutton, M. Tyler, S. Chan, and J. Leach, "A 256× 256 40nm/90nm CMOS 3D-stacked 120dB dynamic-range reconfigurable time-resolved SPAD imager," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2019, pp. 106–108, doi: 10.1109/ISSCC.2019.8662355.

[3] Y. Hirose, S. Koyama, M. Ishii, S. Saitou, M. Takemoto, Y. Nose, A. Inoue, Y. Sakata, Y. Sugiura, T. Kabe, M. Usuda, S. Kasuga, M. Mori, A. Odagawa, and T. Tanaka, "A 250 m direct time-of-flight ranging system based on a synthesis of sub-ranging images and a vertical avalanche photo-diodes (VAPD) CMOS image sensor," *Sensors*, vol. 18, no. 11, art. no. 3642, Oct. 2018, doi: 10.3390/S18113642.

[4] C. Bruschini, H. Homulle, I. M. Antolovic, S. Burri, and E. Charbon, "Single-photon avalanche diode imagers in biophotonics: review and outlook," *Light Sci. Appl.*, vol. 8, art. no. 87, Sep. 2019, doi: 10.1038/S41377-019-0191-5.

[5] A. C. Ulku, C. Bruschini, I. M. Antolović, Y. Kuo, R. Ankri, S. Weiss, X. Michalet, and E. Charbon, "A 512 × 512 SPAD image sensor with integrated gating for widefield FLIM," *IEEE J. Sel. Top. Quantum Electron.*, vol. 25, no. 1, art. no. 6801212, Jan. 2019, doi: 10.1109/JSTQE.2018.2867439.

[6] I. Gyongy, N. Calder, A. Davies, N. A. Dutton, R. R. Duncan, C. Rickman, P. Dalgarno, and R. K. Henderson, "A 256×256, 100-kfps, 61% fill-factor SPAD image sensor for time-resolved microscopy applications," *IEEE Trans. Electron Devices*, vol. 65, no. 2, pp. 547–554, Dec. 2017, doi: 10.1109/TED.2017.2779790.

[7] Yole Développement, "LiDAR for automotive and industrial applications," Oct. 2020 [Online] Available: https://www.i-micronews.com/products/lidar-for-automotive-and-industrial-applications-2020/?utm_campaign=PR_LiDAR_MarketUpdate_Livox_LiDAR_YOLE GROUP_August2020.

[8] K. Ito, Y. Otake, Y. Kitano, A. Matsumoto, J. Yamamoto, T. Ogasahara, and H. Hiyama, "A back illuminated 10μm SPAD pixel array comprising full trench isolation and Cu-Cu Bonding with over 14% PDE at 940nm," in *Int. Electron Devices Meeting Tech. Dig.*, Dec. 2020.

[9] M. Beer, J. F. Haase, J. Ruskowski, and R. Kokozinski, "Background light rejection in SPAD-based LiDAR sensors by adaptive photon coincidence detection," *Sensors*, vol. 18, no. 12, art. no. 4338, Dec. 2018, doi: 10.3390/S18124338.

[10] I. Vornicu, F. Bandi, R. Carmona-Galán, and Á. Rodríguez-Vázquez, "Low-noise and high-efficiency near-IR SPADs in 110nm CIS technology," in *Proc. ESSDERC 49th Eur. Solid-State Device Res. Conf. (ESSDERC)*, Krawkow, Poland, Sept. 2019, pp. 23–29, doi: 10.1109/ESSDERC.2019.8901757.

[11] M. Sanzaro, P. Gattari, F. Villa, A. Tosi, G. Croce, and F. Zappa, "Single-photon avalanche diodes in a 0.16 μm BCD technology with sharp timing response and red-enhanced sensitivity," *IEEE J. Sel. Top. Quantum Electron.*, vol. 24, no. 2, art. no. 3801209, Mar. 2018, doi: 10.1109/JSTQE.2017.2762464.

[12] S. Lindner, S. Pellegrini, Y. Henrion, B. Rae, M. Wolf, and E. Charbon, "A high-PDE, backside-illuminated SPAD in 65/40-nm 3D IC CMOS pixel with cascoded passive quenching and active recharge," *IEEE Electron Device Lett.*, vol. 38, no. 11, pp. 1547–1550, Nov. 2017, doi: 10.1109/LED.2017.2755989.

[13] T. Al Abbas, N. A. W. Dutton, O. Almer, S. Pellegrini, Y. Henrion, and R. K. Henderson, "Backside illuminated SPAD image sensor with 7.83μm pitch in 3D-stacked CMOS technology," in *Int. Electron Devices Meeting Tech. Dig.*, Dec. 2016, pp. 8.1.1–8.1.4, doi: 10.1109/IEDM.2016.7838372.

[14] I. Takai, H. Matsubara, M. Soga, M. Ohta, M. Ogawa, and T. Yamashita, "Single-photon avalanche diode with enhanced NIR-sensitivity for automotive LIDAR systems," *Sensors*, vol. 16, no. 4, art. no. 459, Mar. 2016, doi: 10.3390/S16040459.

[15] C. Veerappan and E. Charbon, "A low dark count p-i-n diode based SPAD in CMOS technology," *IEEE Trans. Electron Devices*, vol. 63, no. 1, pp. 65–71, Jan. 2016, doi: 10.1109/TED.2015.2475355.

[16] J. M. Pavia, M. Scandini, S. bner, M. Wolf, and E. Charbon, "A 1 × 400 backside-illuminated SPAD sensor with 49.7 ps resolution, 30 pJ/sample TDCs fabricated in 3D CMOS technology for near-infrared optical tomography," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2406–2418, Oct. 2015, doi: 10.1109/JSSC.2015.2467170.

[17] E. A. Webster, L. A. Grant, and R. K. Henderson, "A high-performance single-photon avalanche diode in 130-nm CMOS imaging technology," *IEEE Electron Device Lett.*, vol. 33, no. 11, pp. 1589–1591, Nov. 2012, doi: 10.1109/LED.2012.2214760.

[18] E. A. Webster, J. A. Richardson, L. A. Grant, D. Renshaw, and R. K. Henderson, "A single-photon avalanche diode in 90-nm CMOS imaging technology with 44% photon detection efficiency at 690 nm," *IEEE Electron Device Lett.*, vol. 33, no. 5, pp. 694–696, May 2012, doi: 10.1109/LED.2012.2187420.

[19] A. Gulinatti, F. Ceccarelli, M. Ghioni, and I.Rech, "Custom silicon technology for SPAD-arrays with red-enhanced sensitivity and low timing jitter," *Opt. Express*, vol. 29, no. 3, pp. 4559-4581, Jan. 2021, doi .10.1364/OE.413821.

[20] Laser Components, "COUNT® NIR," Oct. 2020 [Online] Available: https://www.lasercomponents.com/de-en/product/count-nir/

[21] Excelitas Technologies, "SPCM-AQRH," Oct. 2020 [Online] Available: https://www.excelitas.com/product/spcm-aqrh

[22] K. Morimoto and E. Charbon, "High fill-factor miniaturized SPAD arrays with a guard-ring-sharing technique," *Opt. Express*, vol. 28, no. 9, pp. 13068–13080, Apr. 2020, doi: 10.1364/OE.389216.

[23] F. Acerbi, G. Paternoster, A. Gola, N. Zorzi, and C. Piemonte, "Silicon photomultipliers and single-photon avalanche diodes with enhanced NIR detection efficiency at FBK," *Nucl. Instrum. Methods. Phys. Res. B*, vol. 912, pp. 309–314, Dec. 2018, doi: 10.1016/J.NIMA.2017.11.098.

[24] E. Van Sieleghem, A. Süss, P. Boulenc, M. Rosmeulen, and C. Van Hoof, "A NIR-enhanced silicon BSI SPAD with low sensitivity to process fluctuations and 15 μm pitch," in *Single Photon Workshop 2019 Book of Abstracts*, Milan, Italy, Oct. 2019, pp. 149.

[25] G. Jegannathan, T. Van den Dries, M. Kuijk, "Current-Assisted SPAD with Improved pn Junction and Enhanced NIR Performance," *Sensors*, vol. 20, no. 24, art. no. 7105, Dec. 2020, doi: 10.3390/S20247105.

[26] J. Iwata, K. Morimoto, Y. Kuroda, T. Goden, T. Sasago, Y. Ota, K. Ota, M. Shinohara, Y. Fukuchi, A. Chiba, M. Furuta, H. Takahashi, and T. Ichikawa, "A 0.16e-rms temporal noise 0.015Hz/μm2 dark count rate charge focusing SPAD image sensor for low light imaging," *ITE Tech. Rep.*, vol. 44, no. 11, pp. 73-76, Mar. 2020.

[27] C. Veerappan, Y. Maruyama, and E. Charbon, "Silicon integrated electrical micro-lens for CMOS SPADs based on avalanche propagation phenomenon," in *Proc. Int. Image Sensor Workshop*, vol. 4, 2013.

[28] A. W. Ludikhuize, "A review of RESURF technology," in *Proc. 12th Int. Symp. on Power Semicond. Devices & ICs*, May 2000, pp. 11-18, doi: 10.1109/ISPSD.2000.856763.

[29] M. W. Fishburn, "Fundamentals of CMOS single-photon avalanche diodes," Ph.D. dissertation, University of Technology, Delft, 2012, doi: 10.4233/UUID:7ED6E57D-404E-4372-8053-6B0B5C7FA0FE.