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Welcome to the World of Single-Slope Column-Level Analog-to-Digital Converters for CMOS Image Sensors

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ABSTRACT

This monograph introduces the reader into basic and advanced aspects of single-slope analog-to-digital converters (SS-ADC) applied in solid-state image sensors. It is based upon the developments that took place over the last three decades in this field. Already in the very early days of CMOS image sensors (CIS), the very first SS-ADC was implemented. The architecture of the SS-ADC is an appealing concept for column-level ADCs in a CIS. Especially the small silicon area occupied by the ADC and the low power consumption are very attractive features. Unfortunately the SS-ADC, as it originally was developed, is relatively slow. This monograph describes all advantages and limitations of the SS-ADC, as well as the various improvements mainly focusing on increasing the conversion speed. On academic as well as on industrial level various optimizations were proposed to make the devices not only faster, but also to increase their performance in terms of noise. Implementation of a digital

correlated sampling technique or the application of multiple correlated sampling (without any hardware change) are a couple of examples how SS-ADCs contribute to improved image quality of the CIS.

Before diving into various architectures of a SS-ADC, the monograph starts with an overview of some basic building blocks of a CIS. Conceptual improvements are described, finally coming to the so-called “counting SS-ADC”. A relatively large section is devoted to the theoretical analysis of the latter architecture, because this device has a unique combination of speed and low noise, two critical performance parameters for a CMOS image sensor.

1

Introduction

CMOS image sensors (CIS) have come a long way from the late 1980s and early 1990s up to where they are today. However, already since the very first developments in the field, column-level single-slope analog-to-digital converters (SS-ADC) were incorporated [7]. The combination of an image sensor with on-chip column-level ADCs demonstrates exceptional performance as far as speed and power are concerned. It is not only the imaging array that went through a lot of new developments, so did the SS-ADC configuration. This monograph gives an overview and background of the various developments of the SS-ADCs.

In Section 2 of this monograph, some background information is given about the general CIS architecture, the CIS pixels and the noise sources present in a CIS. Part of this general technical information is used in the remaining section of the monograph. Section 3 describes the various architectures used in a SS-ADC, starting with the most simple and earliest device described to the more complex architectures that include additional features in the ADC. After the description of the overall structure of the SS-ADCs, in Section 4 more details are studied about the various building blocks that are used in the SS-ADCs, such as amplifiers, comparators, ramp generators and counters. The monograph concludes with a future outlook, included in Section 5.

2

Nice to Know and Need to Know

In Section 2 of this monograph a few subsections are included that highlight some basic components that are going to be of use in the rest of the monograph. Especially in Section 3, in which the SS-ADC architectures are being described, several structures rely on the material that will be discussed in Section 2. (Experienced CMOS image sensor engineers can skip Section 2. For them, hopefully nothing new will be described.)

2.1 CMOS Image Sensor Architecture

A CMOS image sensor contains several major building blocks that can be found in almost every device, irrespective of its application, design, or foundry. Figure 2.1 is an illustration of a more generic architecture of a 2-dimensional CMOS image sensor.

The various blocks of the device depicted in Figure 2.1 are:

- the imaging or pixel array, consisting of a 2D matrix of pixels (1D image sensors or linear imagers are also being used in the industry, but the majority of the fabricated devices are 2D image sensors),

Figure 2.1: Basic architecture of a 2D CMOS image sensor.

- the vertical addressing circuitry to address the rows of the array. This circuitry generates and distributes row select pulses, reset pulses and transfer pulses (see further),
- the column busses, that transfer the pixel signals to the (column-level) electronic circuitry outside the pixel array,
- the horizontal addressing circuitry to address the columns of the array. This circuitry generates and distributes column select pulses and any other pulses needed in the column circuitry,
- the column circuitry, which receives the pixel signals through the column busses. The column circuitry is used to pre-process the pixel information. Examples of this pre-processing are: noise cancellation, extra amplification in the analog domain, analog-to-digital conversion, etc.,
- the output buffer, which can be analog or digital circuitry. In the case the column circuitry does not include an analog-to-digital convertor, the latter can be part of the output buffer, in the case the column circuitry includes an analog-to-digital convertor, the

buffering or the coding of the digital output data will take place in the output buffer.

2.2 CMOS Pixels

Over the last three decades many different CMOS pixels are being proposed, ranging from:

- passive pixels with a single transistor included (next to the photodiode), to,
- active pixels with three transistors, to,
- pinned-photodiode pixels with four transistors, to,
- shared pixels, based on the pinned-photodiode pixels, but in which several photodiodes share the same output structure. In this way the average number of transistors per pixel is reduced to a number below two (e.g., 2×4 sharing results in 11 transistors per eight photodiodes, or 1.375 transistor per pixel).

In modern CMOS image sensors, most pixel designs rely on the concept of the pinned-photodiode or PPD [34] in combination with an intra-pixel charge transfer [12]. The PPD has several very attractive advantages over all other pixel configurations, such as:

- capability of removing several noise sources by means of correlated-double sampling (see further),
- low dark current,
- low image lag,
- high light sensitivity.

Figure 2.2 shows the circuit diagram of the pinned-photodiode pixel or 4T pixel.

Figure 2.2: Schematic diagram of a pinned-photodiode or 4T pixel.

Its working principle can be summarized as follows:

- at the start of a new exposure time, the pixels need to be reset. This is done by simultaneously activating the transfer gate (TG) and the reset (RST). In this way all electrons that were still in the pinned-photodiode (PPD) will be drained and a new exposure cycle can be started once the transfer gate (and the reset) is de-activated,
- during the exposure time, photons can penetrate into the photodiode, and generate electron-hole pairs. The electrons are stored in the photodiode, while the holes are being drained through the grounded substrate,
- at the end of the exposure time, the pixel is being prepared for the readout cycle. This is done by first activating the reset (RST), to make sure that the input capacitance (C_{FD}) of the in-pixel buffer (SF) is being reset (the input capacitance of the in-pixel buffer is often referred to as floating diffusion capacitance, output node capacitance or conversion node capacitance),
- once the reset (RST) is de-activated again (and as will be described later), a first measurement of the voltage on the “empty” input capacitor (C_{FD}) of the in-pixel buffer is performed. The in-pixel buffer “copies” the voltage at its input node to its output node. By activating the row selection (RS) switch this output voltage becomes available on the column bus,

- next the transfer gate (TG) is pulsed, and the electrons generated and stored in the photodiode are transferred to the input capacitor (C_{FD}) of the in-pixel buffer,
- finally, the voltage at its input is “copied” by the in-pixel buffer to its output, and the latter is still connected to the column bus,
- the readout cycle of the pinned photodiode pixel is ended by deactivating the row selection switch (RS).

2.3 Noise Sources in a CMOS Pixel

Although the pixels of a CMOS image sensor contain “only” four transistors (or even less), the pixels are complex structures if it comes down to their noise behaviour. It should be noted that when designing pixels that are sensitive to a single photon-generated electron, the same pixel is also sensitive to a single noise electron. Thus, noise is a very important parameter in the performance discussion of an image sensor. The noise determines the lowest light level at which an imager still can capture images with a decent quality. The various noise sources present in an image sensor can be split in two major groups: noise that is time variant but spatially invariant (temporal noise), and noise that is spatially variant but time invariant (fixed-pattern noise).

The major temporal noise sources that can influence the performance of the pixels, are:

- Johnson noise, present in resistors and channels of MOS transistors,
- kTC noise, being the uncertainty of the voltage level on a capacitor after that capacitor is charged or discharged through a resistor,
- $1/f$ noise, being a low-frequency noise component present in MOS transistors,
- RTS (random telegraph signal) noise, which can originate from the MOS transistors, but also from the leakage current in the photodiodes (blinking pixels),

- dark-current shot noise: statistical variation of the number of generated dark-current electrons,
- photon shot noise: statistical variation of the number of photons arriving at the pixel within an exposure time slot,
- quantization noise/error: a small variation in analog input signal does not necessarily result in a variation of the digital output signal of an ADC, and vice versa,
- phase noise and/or timing jitter due to interference of various clocks,
- signal cross-talk: signal degradation by resistive signal-dependent voltage drops and capacitive or inductive coupling of clocks or other unrelated signals to the pixel signal.

The major spatial noise sources in relation to the pixels are:

- dark fixed-pattern noise, which can be dark current related (dark-current non-uniformity of DCNU) or electronic circuitry related (dark-signal non-uniformity or DSNU),
- light fixed-pattern noise or Photo Response Non-Uniformity (PRNU), due to variations in gain or quantum efficiency of individual pixels,
- hot spots (or warm pixels, or leakers, or bright stars), due to pixels and pixel clusters with excessive dark current, temperature defects, silicon crystal defects or defects at the silicon surface,
- defect and sick pixels,
- cosmetic defects (dust, moisture, scratches, stains, ...).

Besides the long list of noise sources that can play a (negative) role in the generation of images, the overall noise discussion is extra complicated by the fact that the noise can be generated in the pixels themselves, but also by the circuitry “around” the pixels. For instance, the column-level analog column circuitry can introduce noise on column level (e.g., all

Figure 2.3: Illustration of the perception of column noise, for respectively (from left to right), the ratio of pixel noise over column noise is equal to 0 dB, 5 dB, 10 dB, 15 dB and 20 dB.

pixels of one column pass through the noisy circuit present on that column). Or the $1/f$ noise and Johnson noise present in the on-chip circuitry to generate bias and reference voltages for the column circuitry can result in noise on row level. Both column noise (mostly spatial noise) and row noise (mostly temporal noise) are very easy to perceive by the human visual system. As a rule of thumb: column and row noise should be 20 dB or more below the pixel noise, otherwise the column and/or row patterns are noticeable and non-acceptable. This statement is illustrated in Figure 2.3, where an (artificial) image is shown with an average value of 127 DN (8-bit image) and a constant noise value on pixel level of $\sigma_{pix} = 3.5$ DN. From left to right, column noise σ_{col} is added such that the ratio $\sigma_{pix}/\sigma_{col}$ is equal to 0 dB, 5 dB, 10 dB, 15 dB and 20 dB.

2.4 Correlated-Double Sampling

Correlated-double sampling (CDS) is a very efficient method to cancel/correct various noise sources [38]. The possibility to apply CDS in relation to the use of a pinned-photodiode pixel is the key success factor of today's CMOS image sensors. Figure 2.4 illustrates the timing of a classical 4T or pinned-photodiode pixel.

Figure 2.4: Timing diagram of a 4T pixel to illustrate CDS.

From the top down, one can recognize the following pulses:

- the RS pulse to select a particular row of pixels (without RS being active, the pixel is not read out),
- the RST pulse to reset the floating diffusion (output node, conversion node) capacitance,
- the TG pulse needed to transfer the charges from the pinned photodiode to the floating diffusion node,
- the V_p output voltage of the pixel, present on the column bus.

When the reset action is completed, a first sample of output signal V_p in frame number i , or sample 1_i is taken. This first measurement (called “reference” level/signal) contains the following noise components (index i is referring to frame i):

- $(kTC)_i$ after the reset action of the floating diffusion node,
- $(1/f)_i$ originating from the source-follower,
- $(offset)_i$ being the offset signal originating from the source-follower.

After the transfer of the charges to the floating diffusion, a second sample of the output signal V_p (still in frame i), or sample 2_i is taken.

This second measurement (called “active” level/signal) contains the following noise components (index i is referring to frame i):

- $(kTC)_i$ after the reset action of the floating diffusion node, which is 100% correlated to the kTC noise present in the first sample,
- $(1/f)_i$ originating from the source-follower, which is nearly 100% correlated to the $1/f$ noise present in the first sample, given the short time between both samples,
- $(offset)_i$ being the offset signal originating from the source-follower, which is 100% correlated to the offset measured in the first sample.

Of course the second sample also contains the signal that is photon-generated in the pixel. After subtraction of signal 2_i minus signal 1_i only the active signal is left. This way of cancelling kTC noise, $1/f$ noise and offset of the source follower is known as Correlated Double Sampling (CDS) [38].

It should be noted that:

- both samples (sample 1_i and sample 2_i) are also containing Johnson noise, mainly generated by the source follower as well. The Johnson noise in both samples is not correlated, and after CDS, the Johnson noise content in the output signal is increasing by $\sqrt{2}$ compared to the Johnson noise present in the original two samples,
- after a complete charge transfer from the pinned-photodiode to the floating diffusion, the pinned-photodiode is completely empty and fully depleted. This is translated in zero kTC noise at the pinned-photodiode level. In the opposite case, a non-complete charge transfer (due to potential wells/pockets, too long pinned-photodiode, too short transfer time), is resulting in image lag in combination with excess noise.

2.5 Motivation to Use a Column-Level Analog-to-Digital Converter

One of the key advantages of CMOS image sensors (CIS) over Charge-Coupled Devices (CCD) is their ability to co-integrate electronics as

on-chip circuitry. In the first place CMOS technology was developed to fabricate transistors used for low-power, fast analog and digital circuitry.

The extra electronic circuitry for a CIS can be implemented on chip level (e.g., analog programmable gain amplifier), on column level (correlated-double sampler) or on pixel level (global shutter capacitors and transistors). So it should not be surprising that also analog-to-digital converters (ADC) are part of a CIS. The ADC can be implemented on all three levels: on chip, on column, or even on pixel level. In this way the device is converting photons IN into digital numbers OUT. A digital output signal of the CIS is ideally suited for any further processing in the image signal processor (ISP).

Tons of different ADC architectures can be added to the design of a CIS, and are described in the technical literature, such as a successive-approximation ADC (SAR) [21], a sigma-delta ADC ($\Sigma\Delta$) [6], flash converter [5] (very seldom used on an image sensor chip), cyclic ADC [2], folding ADC [15], pipeline ADC [1], single-slope ADC (SS-ADC), etc., and various combinations of the aforementioned configurations. Criteria to choose for one or another can be speed, power consumption or area [14]

Consider the following situation:

- a CIS with $k(H) \times l(V)$ pixels,
- the time needed to convert a single pixel value from the analog to the digital domain is t_c ,
- the time needed to readout the digital data of a single pixel is t_r (all bits of a single pixel are readout in parallel),

then the time it takes to convert a complete image by means of a single ADC will be equal to:

$$k \cdot l \cdot (t_c + t_r). \quad (2.1)$$

Or, in the case the speed of the ADC is the limiting timing factor, the maximum frame rate (not taking into account any other time-consuming action) will be given by:

$$1/(k \cdot l \cdot (t_c + t_r)). \quad (2.2)$$

For example, with a sensor of $1k$ by $1k$ pixels, a conversion time of $1\ \mu s$, and a readout time of $0.01\ \mu s$, the maximum frame rate is equal to $1/1.01\ \text{fr/s} = 0.99\ \text{fr/s}$. (Remark: also the charging/discharging of the long column busses of a CIS takes time, this extra time is not included in the aforementioned calculation. If this time is dominant or limiting the speed of the device, the readout cycle can be pipelined: while one line of information is converted in the ADC, the pixels of the next line of information are being addressed and their signals are being sampled to be ready for the analog-to-digital conversion [4].)

A very simple and efficient solution to speed up the image sensor, is the concept of using multiple ADCs in parallel, for instance providing every column with an ADC, in a so-called column-level ADC architecture. In that case the calculation of the total conversion time is:

$$l \cdot t_c \tag{2.3}$$

in combination with the serial readout of the digital data the frame rate becomes:

$$1/(k \cdot l \cdot t_r + l \cdot t_c). \tag{2.4}$$

With the same numbers as used earlier, the maximum frame rate of the CIS will be $1/0.011\ \text{fr/s} = 90.91\ \text{fr/s}$. Due to the massive parallelism of the architecture, the frame rate is increased drastically, even in combination with a high pixel resolution. In the abovementioned example, the part that limits the frame rate is the readout time of the digital data. Of course multiple parallel readout paths can be created instead of a single one as applied in the example. In a real device the number of parallel readout paths can be optimized such that the readout time is no longer the limiting factor, but the ADC conversion time determines the maximum speed.

If the column-level ADCs are all designed and have their lay-out such that they are located at the same side of the imager, then it should be clear that design and lay-out wise, a column-level ADC should fit into the horizontal pixel pitch of the imager. If the horizontal pixel pitch is too small, a solution for the ADC can be found in:

- making use of shared pixels, e.g., in a $2H \times 2V$ shared concept, this will allow a doubling of the ADC pitch compared to the pixel pitch,

- placing half of the column-level ADCs located at the bottom of the light-sensitive part of the imager, and the other half of the column-level ADCs at the top of the light-sensitive part of the imager.

The pitch of the column-level ADC needs to be pretty small, but the height of the component can be relatively large. So a series of column-level ADCs can add some extra silicon to the CMOS image sensor chip. Having two rows of ADCs is adding almost twice this amount of extra silicon. This drawback limits the amount of ADC rows on the chip. Most commercially available CMOS imagers have maximum two rows of ADCs, although for scientific applications many more rows of ADCs have been reported as well [10]. High speed CIS often employ large pixel sizes for sensitivity reasons. In that case, the pixel pitch can be a multiple of the ADC pitch and several rows are converted in parallel in one ADC cycle. The pixels have multiple parallel output busses in this case. On the other hand, if the frame rate is less of a concern, a single ADC can also serve several columns, for instance up to 32 columns per ADC. But in the latter case the conversion of a complete row of pixels will take a time equal to 32 ADC conversion cycles and will have a serious impact on the row readout time and frame rate. A fast ADC architecture is required in such case, faster than a single-slope ADC. Also matching of the ADCs becomes a critical characteristic, since any gain or offset mismatch would show up as a block non-uniformity pattern in the image. Block patterns are even more visible than a column pattern.

One can go even one step further and provide every pixel with its own ADC. In that case the maximum frame rate will be given by the conversion time t_c summed to the readout time of all pixels, being:

$$1/(k \cdot l \cdot t_r + t_c). \quad (2.5)$$

With the numbers from the example used, the maximum frame rate to the CIS will be $1/0.010001 \text{ fr/s} = 99.99 \text{ fr/s}$. The increase in frame rate by going from a column-level ADC to a pixel-level ADC is not that large in the example. The influence of the readout time t_r is becoming too important. Together with the implementation of the pixel-level

ADC, one should also increase the number of parallel bit lines to further increase the frame rate. Not just all bits of a single-pixel code, but multiple pixel codes in parallel would be the solution.

The very first publication about in-pixel ADC did include an 8 bit ADC in the pixel, but it can be easily understood that, or a very large pixel is needed, or the pixel will have a relatively small fill factor [18]. But more recently and based on stacking technology, the ADC can be physically located beneath the pixel on the processing layer instead of having the in-pixel ADC on the photosensitive layer [27].

3

Single-Slope ADC Architectures

3.1 Concept of the Single-Slope Analog-to-Digital Converter

Focussing on the column-level implementation of the ADC, an architecture based on the single-slope concept is very attractive because both the power dissipation as well as the occupied area can be kept low. As will be shown, also the lay-out implementation of a single ADC per column is relatively simple in the case of a SS-ADC configuration. The very first CIS relying on a column-level SS-ADC was published already in 1990 [7]. The concept of this solution is shown in Figure 3.1.

The working principle of the SS-ADC can be explained as follows:

- After addressing a single line of pixels in the active array, those pixels “copy” their analog value from their conversion node to the column busses, shown in Figure 3.1. All these column busses, perform a sample-and-hold action on these analog values during the conversion cycle of the ADC, and feed the signals into the negative input of a comparator.
- Every column is provided with its own comparator.
- The core of the SS-ADC is a digital counter (indicated in Figure 3.1 as an n -bit counter, today ADCs on a CIS chip are employing

Figure 3.1: Concept of the column-level SS-ADC for a CMOS image sensor.

12-bit ... 14-bit ADCs). The output of the counter is fed into a ramp generator. So while the counter is counting up, the output of the ramp generator will be a monotonically increasing (stairway) ramp signal. The latter is equally distributed to all positive inputs of the comparators.

- In the case that the ramp crosses the analog voltage of (for instance) column i , the comparator associated with column i will toggle and will change state at its output. As mentioned, this happens when the ramp input signals crosses the pixel signal: at that moment the analog to-be-converted input signal is equal to the ramp signal that is the analog equivalent of the digital code of the counter. In other words, the analog signal on column i can be represented by the digital code of the counter. Next, the latter is latched in an n bit RAM memory that is provided at each column. Because all column signals of the CIS need to be converted in one complete ADC cycle, the ramp continues to increase after the conversion of column i to allow also the other analog column signals to be converted. Once the counter

reaches the value $11 \dots 11$, all analog column signals should have been converted, and each n bit RAM memory cell on each column should hold the digital equivalent of the analog signal on its column bus. In a next step the digital memory is read out, before the conversion of the next row of pixels can start. In case when the readout is pipelined with the AD conversion, the memory registers are copied to a second memory bank, which is read out in parallel with the next conversion cycle [39].

A “closer look” to the working principle of the SS-ADC of Figure 3.1 is also shown in Figure 3.2. At the moment that the ramp and the to-be-converted analog-input signal are equal to each other, the comparator toggles. The latter is used to latch the digital code of the ramp generator in the memory.

As can be learnt from Figure 3.1, the architecture of the ADC is relatively simple: a single comparator and an n bit memory cell per column, the digital counter and the ramp generator are common for all columns. That is the explanation why this ADC is low in power consumption and low in area occupancy.

Figure 3.2: Working principle of the single-slope ADC.

Despite of these attractive features, a major drawback of the SS-ADC is its speed limitation. The digital counter has to count from its lowest to its highest value, and this will take time. For example, with an ADC clock $f_{cl} = 100$ MHz and 8 bit data conversion, it will take $2^8 \cdot 10^{-9} \text{ s} = 0.256 \text{ } \mu\text{s}$ to convert a complete row of pixels. This may seem a reasonable conversion time, but 8 bit is more than old fashioned. With a bit count of 12 bits, the theoretical conversion time will increase to $2^{12} \cdot 10^{-9} \text{ s} = 8.2 \text{ } \mu\text{s}$. Another kind of speed issue can be found in the RC time constant of the output lines of the digital counter that are connected to the digital memory cells. These lines have to run along the total focal plane array, and for large area devices, these RC time constants can put a serious limitation on the SS-ADC speed. The distributed capacitor of the metal lines need to be charged and discharged at every clock cycle, resulting in clock skew issues at the memory circuitry.

For both issues solutions are being developed:

- multiple ramps, multiple slopes, making use of the noise characteristics of an image sensor,
- replacing the digital memory cells by counters in the columns.

In the remaining part about the architecture of the SS-ADC, several of those developments will be highlighted.

3.2 Photon Shot Noise in an Image Sensor

Like every electronic component, also image sensors suffer from noise. A lot of work is being done in the field of noise reduction. But there is one major noise contributor that cannot be reduced (in a single image), being the photon shot noise. The signal in an image sensor is the result of the conversion of a number of incoming photons. These incoming photons, although their average number can be constant in time, are sampled within a specific exposure time. For that reason, the amount of photons captured by the imager within the exposure time is a stochastic process and is obeying Poisson statistics. As a result,

if the number of incoming photons per exposure cycle is given by N_{ph} , then the noise on this number will be $N_{ph}^{0.5}$. The story also holds for the number of electrons: if the number of generated and collected electrons in a pixel during a specific exposure time is represented by N_e , the “photon shot noise” on this number will be $N_e^{0.5}$.

A result of the ever-decreasing noise generated by the electronic components in an imager, is the fact that the photon shot noise is becoming more important than ever before. For example, in a pixel of an image sensor that can hold 20,000 e^- at saturation and with an overall noise level in dark of 5 e^- (also known as the noise floor in dark), the photon shot noise will be equal to this noise floor in dark when the pixel holds only 25 e^- . Actually for every output signal larger than 25 e^- , the photon shot noise will be dominant over all other noise sources (known as a photon shot noise limited operation of the sensor).

In Figure 3.3 the analog output signal (red curve, left axis) as well as a few noise sources (blue curves, right axis) are shown as a function

Figure 3.3: Output signal (red curve, left axis) and noise components (blue curves, right axis) of an imager as a function of the output signal’s digital code or number of clock cycles.

of the digital value of the output signal, expressed in DN or digital number. The graphs are based on the following assumptions:

- the maximum output swing of the pixels as well as the maximum input value for the ADC: 1 V,
- the full well capacity of the pixels: 20 ke⁻,
- the conversion gain: 50 $\mu\text{V}/\text{e}^-$ ($=1 \text{ V}/20 \text{ ke}^-$),
- noise floor in dark: 5 e⁻,
- number of ADC bits: 12,
- the voltage represented by the least-significant bit: 0.244 mV ($=1 \text{ V}/(2^{12} - 1)$), equivalent to 4.88 e⁻,
- the quantization error/noise of the ADC: 0.070 mV ($=0.244 \text{ mV}/12^{0.5}$), equivalent to 1.40 e⁻,
- number of electrons needed so that the photon shot noise is equal to quantization noise of the ADC: 1.96 e⁻.
- number of electrons needed so that the photon shot noise is equal to the noise floor in dark: 25 e⁻.

As can be seen on Figure 3.3, as well as based on the numbers mentioned above, the noise floor in dark (blue dashed line) of the sensor is the dominant noise component only for very small output signals (0 DN...25 DN). As soon as the output signal reaches a value of 25 DN (or higher), the photon shot noise (blue solid line) takes over the role of dominant noise source. And this specific characteristic of an imager (where the photon shot noise is the dominant noise source) can be successfully used in the design and optimization of the column level ADC. This will be illustrated in the next subsection.

3.3 Multi-Slope ADC

The conversion speed of the SS-ADC is defined by the ramp speed. A conversion cycle can only be started when the ramp has its lowest

value (00...000) and can only be completed once the ramp has reached its maximum value (11...111). Depending on the accuracy of the ADC, this takes a certain amount of time, and especially a higher conversion resolution of the ADC will slow down the conversion cycle time of the SS-ADC.

Taking into account the presence of photon shot noise in every image sensor's output signal, it can be concluded that the lowest signal-to-noise ratios are obtained in the low-light level or darker parts in an image. The highest signal-to-noise ratios in an image are available for regions that get the highest illumination levels. To keep the ADC quantization noise/error to an acceptable level, the conversion step needs to be as low as possible in the darker areas of an image. But on the other hand, this conversion step can be much higher in the case the sensor signal is larger as well. The principle of the multi-slope ADC is based on this conclusion. For very small values of the analog input signal, the finest conversion possible is applied, but if the analog input signal is larger, the conversion step is enlarged as well. The implementation of this idea is very simple in a ramp ADC [30]. For very small digital output numbers of the counter that generates the ramp, the counter is increased in steps of 1 digit. Once the counter has reached a certain value, it can be increased at every clock cycle by 2 digits. For even larger value of the digital output, increasing in steps of 4 digits and even 8 digits can be considered. The knee points to switch from 1 to 2 digits, from 2 to 3 digits and from 3 to 4 digits, is depending on the setting of the ADC, number of bits in the ADC, maximum output voltage of the sensor, quantization noise/error, etc. In Figure 3.4 the situation of Figure 3.3 is re-sketched with the option of the multiple slope concept. The digital counter that generates the ramp is increased in steps of 1 DN from 0 DN till 128 DN, in steps of 4 from 128 DN till 1024 DN and finally in steps of 16 from 1024 DN till 4096 DN.

The red curve indicates the multi-slope ramp, the solid blue line shows the photon shot noise and the dashed blue line corresponds to the noise floor in dark, including the quantization noise. The overall conversion cycle of the multi-slope ramp is completed after 512 clock cycles instead of 4096 clock cycles in the case of the single-slope ramp

Figure 3.4: Output signal and noise components for the example taking into account the multiple slope configuration (the horizontal axis is the same as the one used in Figure 3.3).

indicated in Figure 3.3 (the horizontal axis of Figure 3.4 is the same as the one used in Figure 3.3).

It should be clear that increasing the digital counter in steps of 1 (quantization noise/error = 1.4 e^- , total noise floor in dark = 5 e^-), in steps of 4 (quantization noise/error = 5.6 e^- , total noise floor in dark = 7.4 e^-), or even in steps of 16 digits (quantization noise/error = 22.4 e^- , total noise floor in dark = 22.9 e^-) will speed up the overall conversion time, without loss of any signal-to-noise ratio of the output signal. The quantization noise/error introduced by the larger increments of the digital code will always be much lower than the photon shot noise. If the ratio of both noise levels is large enough ($>10 \text{ dB}$), the transition from one quantization level to a larger one will not become visible/noticeable in an image. And the overall job of the multi-slope ADC is done in $1/8$ part of the time needed by the original single-slope SS-ADC. Figure 3.5 shows an image with sparse coding of the pixel values in highlight areas to visualize the impact on image quality. The left image uses a quantization level below the shot noise limit, and the visual impact is negligible. The image at the right side utilizes too coarse quantization steps. The effect hereof is noticeable in the picture, mainly in the sky where the pattern of clouds changes. It can help to

Figure 3.5: Images with sparse ADC codes for shot-noise limited pixel values; left: Quantization below shot noise limit; right: Too coarse quantization (mostly noticeable in the clouds).

dither the missing codes in the shot-noise limited part of the response where ADC codes are skipped. Random noise is added in that case around the missing digital codes.

3.4 Multi-Ramp SS-ADC

Another solution to the speed limitation of a SS-ADC can be found in the usage of multiple parallel ramps, instead of a single ramp. This solution is very similar to the folding principle that is also used in combination with other ADC principles.

The conversion with a multi-ramp SS-ADC, starts with a very simple coarse conversion of, for instance, the two most significant bits. This coarse conversion can be done by means of the same hardware that will be used for the fine conversion that will follow later. By means of the 2-bit coarse conversion, for every analog column value, it will be decided in which quarter of the input range the analog sensor output value fits: between $000 \dots 000$ and $010 \dots 000$; between $010 \dots 000$ and $100 \dots 000$; between $100 \dots 000$ and $110 \dots 000$ or between $110 \dots 000$ and $111 \dots 111$. The two most significant bits for each to-be-converted voltage will be stored in the digital memory present in the column circuitry, and this information will be re-used in the definition of the SS-ramp for the fine conversion. The architecture of a multi-ramp SS-ADC is illustrated in Figure 3.6.

Figure 3.6: Architecture of a multi-ramp SS-ADC in which the four parallel ramps are offered via the ramp bus to the select circuits.

In the case of the multi-ramp ADC, the digital ramp needed will be a factor of 4 shorter/smaller in the time domain (the number 4 is coming from 2^2 , in which the exponent is equal to the number of bits that are already converted in the coarse conversion cycle) than the one used in the standard SS-ADC [31]. But this short and small ramp (for the fine conversion) will get an extra offset that can change for every column of the sensor and that will depend on the content of the two most significant bits. For a 12-bit ADC, the offset for the ramp will be 000...000 if the two most significant (and already converted) bits are equal to 00; the offset for the ramp will be 010...000 if the most significant (and already converted) bits are equal to 01; the offset for the ramp will be 100...000 if the most significant (and already converted) bits are equal to 10; the offset for the ramp will be 110...000 if the most significant (and already converted) bits are equal to 11.

This multi-ramp SS-ADC offers four parallel ramps to the input of the converters. All four ramps have the same slope but they differ due to their offsets. Of course, every comparator needs to be connected to only one-out-of-the-four ramps. Which of the four ramps needs to be

Figure 3.7: Output signal and noise components for the example taking into account the multiple ramp configuration (the horizontal axis is the same as the one used in Figure 3.3).

selected and connected to the comparator is determined by the outcome of the coarse conversion of the first two most significant bits.

With the parallel-running multi-ramps, the fine conversion of the least significant bits can be completed. After the conversion is completed, the digital content of the memories can be (serially) read out. If the conversion time of the coarse conversion is neglected, the multi-ramp ADC shortens the conversion time of the classical SS-ADC by a factor defined to the number of ramps, equal to 2^p , where p is the number of bits involved in the coarse conversion. This effect on shortening the conversion time is schematically shown in Figure 3.7: the original single ramp is split into ($p=$) four shorter ramps (1)(2)(3)(4), each with a specific offset (red curves). Also shown in Figure 3.7 are the various noise components on the same time scale as the multiple ramps (blue solid curves for the photon shot noise, blue dashed curve for the noise floor in dark).

To make a quick comparison possible, the horizontal axis in Figure 3.7 is not changed compared to Figure 3.3. It is clear that the total conversion is a factor of four faster in the case of the multi-ramp architecture.

3.5 Multi-Slope, Multi-Ramp ADC

This architecture combines the two foregoing concepts into one ADC, resulting in the most optimum conversion speed possible with an ADC using a ramp [31]. The timing is sketched in Figure 3.8.

The same conventions as in Figure 3.7 are being used, the four ramps with different slopes (1)(2)(3)(4) are shown, each with a specific offset. The same holds for the noise components. (The quantization error/noise that goes together with ramp (3) and ramp (4) coincide.) As can be seen in Figure 3.8, the conversion job is done in 128 clock cycles instead of the 4096 original ones (a factor of 32 faster).

It needs to be mentioned that this multi-slope, multi-ramp ADC is, unfortunately, very sensitive to fixed-pattern noise. Not just the offset of the comparators will show up as fixed-pattern noise, but also the introduction of the knee points in the multi-slope concept and the addition of the offsets to the ramps in the multi-ramp concept can give rise to extra column-level fixed pattern noise. Because the human visual system is immediately triggered by column- or row-wise (fixed-pattern) noise (as illustrated in Figure 2.3), these issues absolutely need to be

Figure 3.8: Output signal and noise components for the example taking into account the multiple-ramp multiple-slope configuration (the horizontal axis is the same as the one used in Figure 3.3). The insert is the magnification of the lower left corner of the curve.

prevented. In the multi-slope, the multi-ramp or the multi-slope multi-ramp ADC the column fixed-pattern noise originating from tricks in the ramp generation can be minimized by so-called “overranging” [26]. With this overranging architecture, the various ramps do overlap each other within the transition region, and in that case the switch from one ramp to the next one can be done in a smooth way. This limits the fixed-pattern noise at the transition points.

3.6 Counting Single-Slope ADC

A key advantage of the SS-ADC architecture is its limited circuitry in every column. Besides the comparator, only a set of (SRAM-) memory cells is needed. But the drawback can be found in the distributed capacitance of the inputs of the memory cells. All cells need to be connected in parallel to the outputs of the digital counter, being the heart of the SS-ADC. As already mentioned, the long interconnect metal lines slow down the overall conversion process and the charging/discharging of these lines consume power. Furthermore, delays on each of the counter bit lines may be slightly different. But when a comparator toggles, the signal on the parallel lines need to be latched simultaneously in the memory. Within one bit step of the ramp signal, the toggling point and speed of the comparator will vary with the difference between the ramp signal and the pixel signal. Process, temperature and supply variations will further increase the spread of this toggling point. A clocked comparator or D-flipflop is required to reduce these signal-independent and signal-dependent variations and allow the memory to latch the data from the counter bit lines. This puts strong timing constraints on the comparator, latch logic, ramp generation and its distribution. Figure 3.9 shows that the ramp itself needs a settling time t_{ramp} , the comparator has a delay t_{comp} , which, worst case, could be starting to toggle right after the settling of the ramp, and the column latch needs a set-up time $t_{l,s}$ before the rising clock edge, and a hold time $t_{l,h}$ after the rising clock edge. During the setup and hold time of the latch, the address bus needs to be stable. To avoid latching the wrong digital code from the counter bit line bus, it is required that the sum of the delays is smaller

Figure 3.9: Timing delay constraints of latch-based ADC.

than one clock period:

$$t_{ramp} + t_{comp} + t_{l,h} < t_{cl}. \quad (3.1)$$

This relation must be fulfilled in the presence of mismatch, temperature and supply voltage variations, and can hamper high speed operation of the ADC.

In Section 3, the comparator response time will be calculated and it will be shown that this comparator delay exceeds 50 ns for a realistic comparator design. This severely limits the maximum speed of this ADC architecture with latches and a stairway ramp signal.

This speed limitation of the SS-ADC can be overcome by the use of a counter instead of a column memory [24]. This in-column counter runs fully in parallel with the main counter that is generating the ramp for the comparators' reference voltages. When the main counter starts at 0 to generate the ramp, also all the in-column counters are being reset. When a particular comparator toggles, the clock of the corresponding in-column counter is disabled, and the count at the toggle point is automatically latched in the counter. After the ramp has reached its

Figure 3.10: Architecture of SS-ADC with digital counters in the column circuitry.

maximum value, the data present in the in-column counters is readout, and the conversion cycle of a next row can start.

Figure 3.10 shows the basic configuration of the SS-ADC with the counters in the column circuitry.

The advantage of this counting SS-ADC architecture is that only one clock needs to be distributed along the horizontal bank of ADCs. Only the (high-speed) main clock is fed to all counters, including the main counter needed to generate the ramp reference signal. With an appropriate clock-tree design, this can relative easily be done for a single clock. Furthermore, with this architecture the comparator delay can exceed multiple clock periods as will be shown in the next paragraph.

Besides the simplification of the distribution of the digital signals, the presence of counters in the columns opens new options and sophistications for the SS-ADC, as highlighted in the next subsections.

3.7 Counting SS-ADC with Digital Correlated Double Sampling

If the in-column counter is designed as a counter with an up/down option, a digital correlated double sampling technique can be implemented [24], [39]. First the conversion of the pixels' reset or reference levels is done

by means of the counting SS-ADC. During this conversion cycle, the in-column counter is set in the count-down mode. When the ramp has reached its maximum value, the digital content of the counters is not read, neither are the counters reset. Next the conversion of the pixels' signal level is done by means of the counting SS-ADC. During this conversion cycle, the in-column counter is set in the count-up mode. When the ramp has reached its maximum value the digital content of the counters is read out. Because the counter did not start from 0 for the second part of the conversion cycle but started from the “negative” value of the reset level, they automatically perform a correlated double sampling in the digital domain. Moreover, because the conversions of the reset level and of the signal level both involve the same comparator, also the offset of the comparator is cancelled out by this concept.

Figure 3.11 illustrates the configuration in which the counter are provided with the feature of up/down counting.

Figure 3.11: Architecture of SS-ADC with digital up-/down-counters in the column circuitry.

Because a complete conversion with this ADC does involve two ramp cycles, it may suggest that the ADC will become slower, but the opposite is true:

- instead of two full-length ramps, a smaller/shorter ramp for the reference level can be used in combination with a full-length ramp for the active signal. The reference levels are always much smaller in amplitude than the active signal levels of the pixels. This concept of combining a short and a long ramp is illustrated in Figure 3.12,
- but most important, since the digital CDS compensates the comparator delay, the ADC can be clocked $5\times$ to $10\times$ faster and the conversion time ultimately is much faster than a single ramp ADC. Where the upper speed limit for a SS-ADC with memory cells was around 100 MHz, the architecture of the SS-ADC with counters in the column circuitry can go up to 1 GHz or more [4].

Figure 3.12: Timing chart in the case a combination of short and long ramp are used.

From the top to the bottom the following graphs are shown in Figure 3.12:

- first graph: the output signal of the sensor (red curve), with its typical sequence of reset level, reference level (containing offset, kTC noise, $1/f$ noise) and the active signal level (containing offset, kTC noise, $1/f$ noise, photon-generated signal),
- second graph: the output signal of the sensor after amplification and inversion (red curve) in relation to a first, short ramp to convert the reference level and a second, long ramp to convert the active signal level,
- third graph: the toggling output of the comparator,
- fourth graph: the clock of the ADC,
- fifth graph: the count value in the up/down counters. Down counting during the conversion of the reference level, up counting during the conversion of the active signal level.

An alternative to the up/down concept of the in-column counter can be the implementation with only a single up-counter. After firstly performing the conversion of the reference signal with the up-counter, the digital content of the counters is converted to their 2's complement by means of a bit-wise inversion or BWI operation [8]. As a consequence, the “negative” values of the reset levels are latched in the counter. Secondly the pixels' signals are converted, keeping the counters in the up-counting mode, automatically a correlated double sampling is performed.

It is also possible to just invert the comparator output during the signal conversion phase to achieve the subtraction [3], [37]. In that case, the counters count during the reference conversion cycle from the start of the ramp until the comparator toggles, and in the active signal conversion cycle from the comparator toggle until the end of the ramp. The counters count in the alternating phase during reference and active

Figure 3.13: Timing chart with inverted counting phase during reset and signal conversion.

signal conversion. Figure 3.13 shows the timing chart in that case:

- first three graphs represent the same waveforms as in Figure 3.12,
- fourth graph shows when the column counter is enabled, and is based upon the comparator output. It is shown that the counter only starts counting when the ramp signal crosses the reference signal, and the counter stops clocking when the ramp crosses the active signal,
- fifth graph shows the counter clock, and
- sixth graph shows the code in the column counter. At the end of the conversion cycle, the counter contains the difference between the active signal and reference signal plus a fixed offset. This offset is equal to the amount of clock cycles during the conversion of the reference signal and can be subtracted in the output stage of the image sensor.

The digital CDS ramp ADC architecture also cancels the offset mismatch of the comparators. In single-slope converters, the comparator

offset needs to be corrected by calibration techniques like auto-zero offset calibration, or by a digital calibration. This is not required with digital CDS ADCs, as the offset mismatch is a common-mode error for both conversion cycles. That is also an important reason why for bit resolutions of 12 bits and more, ADCs with digital CDS is the preferred choice.

This double conversion cycle process with two counting ramps has another beneficial side effect. The spread of comparator delay times is also compensated during the CDS process. If a comparator is too slow, it counts a few cycles extra during reference conversion phase and a few cycles less during active signal conversion phase, if the counting scheme of Figure 3.13 is used. Also with up/down counters (as in Figure 3.12), this comparator delay mismatch is compensated because in case of a slow counter, the counters count down during a few extra cycles during the first conversion step and up during the second conversion step. This means that with counting ramp converters which include digital CDS, the delay constraints which were shown in Figure 3.9 are gone. With a continuous “sawtooth” ramp signal instead of a “stairway” ramp, as shown in Figure 3.14, the settling time of the DAC (t_{ramp}) is also eliminated. The delay of the comparator can even be longer than one clock period. Furthermore, delay variations of the comparators due to mismatch, supply variation or temperature are cancelled by the double ramp CDS operation. This allows comparator designs with response times that are several clock periods long. This will be elaborated in Section 4, when the comparator circuit is discussed in more detail.

Due to this delay compensation, the clock frequency can be drastically increased, even up to 1 GHz. The distribution of the fast clock can be further simplified by generating the clock locally, which allows even higher clock frequencies [4].

3.8 Counting SS-ADC with Correlated Multiple Sampling

A next sophistication step in SS-ADC is the addition of Correlated Multiple Sampling (CMS). As mentioned above, the correlated double sampling is realized by first sampling the reference level, and next the active signal level. But with the in-column counters, it is also possible

Figure 3.14: Timing delay constraints on comparator for counter-based ADC with continuous ramp.

to multiple sample the reference level. Every time the reference level is sampled, the in-column counter is adding more counts without being reset between the samples. In this way r samples of the reference level can be aggregated in the digital domain. In the same way, r samples of the pixels' active signal can be sampled and converted in the digital domain. By means of the up/down counters or up/BWI counters r samples of the reference signal will be subtracted from r samples of the active signal values [8]. Dividing the end result by r performs the correlated multiple sampling for the imager. If r is equal to a power of 2, the division by r can be very easily performed in the digital domain simply by adding a different weighting coefficient to the bits in the final digital code.

This digital correlated multiple sampling technique is fully independent of the hardware implemented in the ADC, the number r of oversampling is only defined by the clocking sequence. The same design and lay-out of the ADC can be used for any number r . The only restriction: if the ADC is designed for n bits, and an oversampling of r is applied, the end result present in the counters is still limited to n bits. After dividing by r only $n - r$ effective bits are left. So if the correlated

multiple sampling needs to result in n effective bits, a total of $n + r$ bits need to be present in the hardware implemented in the columns.

3.9 Counter-Based ADC with Sawtooth Reference Signal

In a counting ramp column ADC, the ramp reference signal can in principle still be generated by a voltage DAC, driven by a counter, which clocks synchronously with the clock that is distributed to the columns. The ramp is in that case a staircase pattern. However, since the ADC clock speed has to be increased, the distribution of this fast staircase waveform needs to be distributed with higher speed as well. This would become problematic due to RC delays and power consumption. A staircase pattern would be needed if the comparator and staircase waveform have to settle within less than one clock period as was required for a memory latch based design and shown in Figure 3.9. But, as already explained, comparator delays are corrected by the column counters. Consequently, it is also possible to distribute a sawtooth voltage waveform rather than a staircase waveform. This waveform can be generated with simpler circuitry, at higher speed, with better (differential) linearity and more uniformity along the columns. As shown in Figure 3.14, the settling requirement for the waveform is not relevant for the column counters, and the comparator delay can be even longer than the clock period of the counter clock.

The sawtooth voltage spans the interval when the counters are active during each conversion cycle, both for reference and active signal conversion. For the reference conversion, the range of the sawtooth and the amount of clock cycles can be limited, based upon the expected signal variation during that cycle and the comparator response time (as will be explained later). In case when an analog CDS pre-amplifier is used, the reference conversion range includes the offset variation, thermal drift and temporal noise of the pre-amplifier and the residual noise after CDS of the pixel. Without pre-amplifier, the reference conversion range includes the pixel fixed-pattern noise, thermal noise and thermal drift of the pixel output.

The sawtooth waveform may be a small change at first sight, but it offers quite a particular extra benefit. In fact, the comparator output

Figure 3.15: Quantization errors during reference and active signal conversion for a counting ramp ADC with a continuous ramp generation.

signal has now become a time-encoded signal of which the length is proportional to the signal to be converted. The AD conversion task has now become a time-to-digital (TDC) conversion of the comparator output (Figure 3.15). The actual quantization – and quantization error – happens after the comparator output, at a flipflop that registers the comparator output at a clock edge. This flipflop then enables or disables the counter, and it can also be the first stage of a ripple counter. In the latter case, the clock and comparator output are logically AND-ed. In both cases, the quantization error occurs at the relevant clock edge of the flipflop.

Going forward, the ADC counter principle of Figure 3.13 is assumed. An equivalent analysis can be made for the scheme with up/down counters as in Figure 3.12 or up-counters with intermediate bit-wise inversion. Figure 3.15 illustrates the quantization error during the conversion of the reference level and active signal level. The first waveform is the counter enable signal, which is derived from the comparator output. The third waveform is the ADC clock. These two signals are logically AND-ed to obtain the counter clock, shown as the second waveform. On every rising edge of the counter clock, the counter increments by one. The distance between the edge of the count enable signal and the relevant last/first clock edge is representative for the quantization error. The advantage of the sawtooth ramp generator is that, combined with

double ramp correlated double sampling, the quantization noise will be 1st order noise shaped. To calculate the quantization error after CDS, consider the situation when there are no other noise sources and when no carriers are collected in the pixel, as is the case in dark. If we ignore temporal noise in the readout chain for a moment, the reset and signal samples from the pixel, V_{reset} and V_{signal} respectively, are exactly equal. The comparator toggles at exactly the same moment after the ramp started for both samples. In absence of other noise sources, the phase shift between the comparator edge and the first or latest counter clock edge for both samples, shown as e_{reset} and e_{signal} in Figure 3.15, are correlated. The phase shifts add up to exactly one clock period:

$$e_{reset} + e_{signal} = t_{cl}. \quad (3.2)$$

The output $y[u]$ of the ADC for an u th conversion cycle can be written as:

$$y[u] = x_{signal}[u] + e_{signal} - x_{reset}[u] - e_{reset} + C \quad (3.3)$$

where $x_{signal}[u]$ and $x_{reset}[u]$ are the amount of counts in the counter detected during reference and active signal conversion. C is a constant corresponding with the initial counter value in case of up/down counters [24] or equal to the total amount of clock cycles during the reference conversion phase if the signal conversion phase uses the inverse comparator output [3].

If the reference and active signal conversions are considered as separate cycles (indexed by count variable w , Equation (3.3) can be rewritten as):

$$y[w] = x[w] - x[w - 1] + e[w] - e[w - 1] + C. \quad (3.4)$$

Relation (3.2) shows how the quantization errors in both cycles are related. In reality, thermal, flicker and RTS noise of the pixel source follower and the pre-amplifier will cause the pulse duration of the comparator output to vary slightly. This noise will appear as random jitter on the falling edge of the comparator output which adds to the quantization error. But the subtraction process will act as a 1st order noise shaping filter, similar as in time-to-digital converters [32].

The noise transfer function N_{TG} is a discrete-time differentiator operation, with transfer function:

$$N_{TG}(z) = 1 - z^{-1}. \quad (3.5)$$

To obtain the frequency response of the noise transfer function, let:

$$z = e^{j2\pi f/f_{cl}}. \quad (3.6)$$

For the magnitude of this response [13]:

$$|N_{TG}(f)| = 2 \cdot \sin(\pi \cdot f/f_{cl}) \quad (3.7)$$

where f_{cl} is the ADC counter clock frequency. This means that the quantization noise is high-pass filtered.

If the bandwidth of the comparator is substantially smaller than the clock frequency f_{cl} , then:

$$\sin(\pi f/f_{cl}) = \pi f/f_{cl}. \quad (3.8)$$

With this assumption, the maximum Signal-to-Noise Ratio ($\text{SNR}_{\max}$) becomes [13]:

$$\text{SNR}_{\max} = 6.02 \cdot n + 3.41 + 30 \cdot \log(\text{OSR}) \quad (3.9)$$

with n is the number of bits and the oversampling ratio OSR being equal to:

$$\text{OSR} = f_{cl}/2f_{comp} \quad (3.10)$$

in which f_{comp} represents the bandwidth of the comparator. Increasing the clock frequency, and hence the OSR improves the SNR, once the frequency of the counter (=sampling frequency) is substantially above the bandwidth of the comparator.

Intuitively, it may not feel beneficial to limit the comparator bandwidth. But this noise shaping can be optimally exploited, in combination with an adequate decimator filter. Practically, a large oversampling ratio may not be possible because the maximum frequency of the distributed clock is also limited.

3.10 Time-Stretched SS-ADC

A very specific SS-ADC architecture can be found back in the so-called time-stretched SS-ADC. The main goal of this architecture is to make the overall conversion time of the SS-ADC faster. Basically, the time-stretched SS-ADC is splitting the total conversion cycle into two parts: a first one for the most-significant bits according to the standard SS-ADC, next the ADC is applying the time stretching, and in a last step the least-significant bits are converted again in a standard SS-ADC. The principle of the time-stretched SS-ADC is applicable to a counting SS-ADC as well.

The principle of the time-stretched SS-ADC is explained in this subsection [25]. Figure 3.16 shows the origin of the quantization noise or quantization error: two analog signals V_1 and V_2 can result in the same digital code.

The ramp voltage V_{rc} is crossing the analog input voltages V_1 and V_2 respectively at time points t_1 and t_2 . But as can be seen in Figure 3.16, the two time points fall within the same clock period with a length of t_{cl} , and result in the same digital code. More digital information can be made available if also t_1 and t_2 could be measured. The latter can be done by means of the time-stretched ADC in which the “time-residues” $t_{cl} - t_1$ and $t_{cl} - t_2$ are measured and will add extra bits to the first conversion. These time-residues can be measured by increasing the clock 16 times (in the case extra 4 bits need to be generated). But a more

Figure 3.16: Origin of the quantization noise/error.

gentle solution can be found in stretching the time-residues by a factor of 16 and still use the same clock with frequency f_{cl} [25].

For example, in a 10 bit SS-ADC, the 6 MSB can be converted in the standard SS-ADC, while the 4 LSB can be retrieved from the time residues. The gain in conversion speed is obvious: the 6 MSB use $2^6 = 64$ clock cycles, the remaining 4 LSB are being made up by $2^4 = 16$ clock cycles extra. In total a 10 bit conversion with the time-stretching solution takes 80 clock cycles instead of $2^{10} = 1024$ clock cycles ($12.8 \times$ faster).

4

Circuit Elements

In Section 4 the various elements of a ramp ADC will be discussed in more detail. Unless otherwise specified, we assume a digital CDS counting ramp ADC with a continuous sawtooth ramp as described in Section 3 and a CDS pre-amplifier.

4.1 CDS Pre-Amplifier

Correlated double sampling of the reference level and active signal level of the pixel, as explained before, can also be realized by an analog pre-amplifier. The typical topology for this circuit is an inverting capacitive amplifier with coarse programmable gain, as shown in Figure 4.1. The amplifier is in feedback when the pixel reference level V_{reset} is applied at its input. The feedback switch Φ is opened after releasing the reset switch of the pixel. After charge transfer, the signal V_{signal} appears at the amplifier input and the output of the amplifier V_{PGA} is:

$$V_{PGA} = (C_i/C_f) \cdot (V_{signal} - V_{reset}) + V_{ref}. \quad (4.1)$$

Figure 4.1: Readout chain of a column showing the pixel, pre-amplifier, dual sample and hold stage and ADC comparator. Timing of the circuit presented in Figure 4.1(a).

The kTC noise and offset mismatch of the pixel is already eliminated by this amplifier. In fact, this CDS stage offers several more benefits:

- It reduces the span of the ADC reference ramp as the offset non-uniformity of the column amplifiers is considerably less than the pixel non-uniformity and the correlated noise.

- It allows pipelined operation of pixel signal sampling and AD conversion. This increases the frame rate. In combination with a S&H stage, several pipelining schemes can be considered.
- The adjustable gain reduces effects of ADC quantization noise at higher gain settings.

To reduce the read noise with this pre-amplifier, large capacitors are needed in the amplifier, up to several pF. This may not be feasible in a small pitch design. When a CDS pre-amplifier is used in combination with digital CDS in the ADC, smaller PGA capacitors can be used because the digital CDS can cancel introduced kTC noise in the PGA. Figure 4.1(a) shows a way to implement such a double CDS, together with the appropriate timing in Figure 4.1(b). Capacitor C_{rs} samples the reference of the pre-amplifier, right after releasing Φ , C_{ss} samples the output signal after charge transfer, as given by Equation (4.1). The ADC performs digital CDS on both samples as described earlier. The digital CDS step cancels the non-uniformity, as well as the kTC noise and the low-frequency noise of the CDS pre-amplifier without the need for large amplifier capacitors. In this way, the input-referred read noise of the readout chain can be drastically reduced. This is in particular relevant at high amplifier gain setting. An input-referred noise below 30 μV rms has been reported at $16\times$ gain [16].

4.2 Comparator

The task of the comparator is to decide if the ramp waveform has crossed the to-be-converted input sampled signal level. The inputs of the comparator are the distributed ramp reference signal and the pixel active signal. The latter is often stored on a sample capacitor. The range and offset level of the ADC depend on the architecture and the fabrication process, but a typical input range for the ramp is 1 V. Important other criteria are summarized in Table 4.1.

As explained earlier, the ramp ADC input can either be a stairway waveform or a continuous sloped sawtooth waveform. In case of a stairway, it is expected that the comparator takes its decision in a short time, after the distributed DAC reference has settled. The comparator

Table 4.1: Typical specifications of a comparator

Parameter	Typical	Unit	Comment
Power supply	3.3	V	Output stage can include level shifter to digital supply (1.8V or lower)
Input swing	1	V	
Offset variation	50	mV p-p	Cancelled by digital CDS
Output jitter	1	ns p-p	$\pm \frac{1}{2}$ clock cycle. Can be converted back to input noise
Comparator response delay	<200	ns	For 500 MHz clock with 2-edge counter Cancelled by CDS Depends on counter overhead
Current consumption	1 . . . 10	μ A	Depending on required response time and ramp slope

needs to decide within $\frac{1}{2}$ clock period, which is 5 ns for a 100 MHz ADC clock. This translates to very strong requirements for the comparator design, in terms of bandwidth and comparator response time (as well as on the ramp signal generation and distribution). But as explained, with a sawtooth and digital CDS, the timing is more relaxed. The comparator delay is cancelled by the CDS. If sufficient overhead is available in the digital CDS circuit, up to 100 clock cycles can be available before the comparator output toggles after the ramp-signal crossing. The next analysis will therefore be applicable to sawtooth ramp comparators with digital CDS.

The response time t_{res} of a comparator will be analyzed further. Figure 4.2 models the comparator circuit as operational transconductance amplifier (OTA) as its first stage and an inverter as a second comparator stage, similar to [29]. The transconductance amplifier is connected to the ramp reference signal V_{rc} at its positive input, and to the pixel signal V_p at its negative output. It drives a load capacitor C_L and an inverter. This inverter could be part of the next circuit block already, e.g., a latch or the first stage of a ripple counter. In most cases, this inverter is needed also as a level shifter between different supply voltage domains. At this location in the circuit, the design shifts from an analog high voltage supply (at 3.3 V, 2.8 V or 2.5 V, using thick gate oxide transistors) to the digital supply at a lower supply voltage

Figure 4.2: Comparator circuit, small-circuit model and signals.

(1.8 V or lower, using faster thin gate oxide transistors). The digital supply is connected to the counters and clock distribution tree. It is not only more power efficient and faster, but this split also makes the analog supply more quiet, and avoids interference of the digital activity on the analog signals.

The first stage of the comparator is a transconductance amplifier with transconductance G_m . Right after the ramp-signal crossing, when the comparator starts toggling, the OTA is operating in transient state. Before the crossing, the transconductance amplifier output was saturated in one output state, and right after the crossing it has to move to the other state. The inverter, which is the second stage of the comparator, will toggle during the transient state of the OTA. When the ramp is rising, as long as the ramp signal V_{rc} is below the pixel signal voltage V_p , the output of the OTA is saturated. Once V_{rc} crosses V_p the transconductance amplifier will output a current $i_c(t)$, given by:

$$i_c(t) = G_m \cdot (V_{rc}(t) - V_p) = G_m \cdot x(t) \quad (4.2)$$

which discharges (or charges) the load capacitor C_L . The differential input signal of the comparator will start to rise proportionally with time. Using the small-signal model of Figure 4.2, and defining as reference

time $t = 0$ s, the point where the ramp crosses the signal, the input signal to the comparator can be described as:

$$x(t) = m_{rc} \cdot t \cdot u(t) \quad (4.3)$$

where $u(t)$ is the step response ($u(t) = 0$ if $t < 0$, $u(t) = 1$ if $t \geq 0$), and the input slope ramp is given by m_{rc} :

$$m_{rc} = dV_{rc}/dt. \quad (4.4)$$

The transfer function of the OTA, $H_{TA}(s)$, including its load C_L and output impedance R_o is given by:

$$H_{TA}(s) = Y(s)/X(s) = G_m / [(C_L \cdot (s + 1/C_L R_o))] \quad (4.5)$$

where $Y(s)$ represents the OTA output in the Laplace domain, and $X(s)$ represents the OTA input in the Laplace domain.

The Laplace transform of the ramp signal $x(t)$ is m_{rc}/s^2 . This means that at the output of the OTA the signal will be:

$$Y(s) = H_{TA}(s) \cdot (m_{rc}/s^2) \quad (4.6)$$

or converted back to the time domain:

$$y(t) = m_{rc} G_m R_o \cdot [t - \tau_0 \cdot (1 - \exp(-t/\tau_0))] \cdot u(t) \quad (4.7)$$

where τ_0 is the time constant at the OTA output is given by:

$$\tau_0 = R_o \cdot C_L. \quad (4.8)$$

This output signal $y(t)$ is the ramp response of the amplifier, which shows that the output will follow the input ramp with a gain:

$$G_m \cdot R_o,$$

and a delay:

$$\tau_0 \cdot (1 - \exp(-t/\tau_0)).$$

After a time of about $3 \cdot \tau_0$ the circuit will reach its steady-state regime, where $y(t)$ follows the input with a fixed delay τ_0 and a constant slope $m_{rc} \cdot G_m \cdot R_o$.

Table 4.2: Calculation of a typical comparator response time

Parameter	Symbol	Value
OTA bias current		4 μA
OTA output impedance	R_o	1.1 $\text{M}\Omega$
OTA transconductance	G_m	33 mS
OTA gain: $A = G_m R_o$	A	37.5
OTA load capacitance	C_L	5 fF
Ramp slope	m_{rc}	0.25 $\text{V}/\mu\text{s}$
Threshold level of 2nd stage of comparator	ΔV_y	0.5 V
OTA time constant $\tau_0 = R_o C_L$	τ_0	5.6 ns
OTA ramp delay	$\Delta V_y / (m G_m R_o)$	53.3 ns
Comparator Response time	t_{resp}	59 ns

Once $y(t)$ crosses the threshold voltage V_t of the inverter, the output of the inverter flips. The response time t_r for the OTA to reach this point can be calculated by solving Equation (4.7) for

$$y(t) = \Delta V_y, \quad (4.9)$$

which is the required voltage change at node y to flip the inverter (practically either $\Delta V_y = V_{DD} - V_t$ or $\Delta V_y = V_t$ depending on the polarity of the comparator and ramp slope).

If $t_r \gg \tau_0$, the OTA will operate in steady state, and is tracking the input ramp with a fixed delay, so:

$$t_{resp} = \Delta V_y / (m_{rc} G_m R_o) + \tau_0. \quad (4.10)$$

The total response time of the comparator t_{comp} is given by:

$$t_{comp} = t_{resp} + t_{inv} \quad (4.11)$$

where t_{inv} represents the delay of the inverter (2nd stage of the comparator). But this delay t_{inv} often can be neglected. Because of the gain of the first stage, the slope of the signal rises or falls much quicker at the input of the second stage (node y) and the second stage will toggle considerably faster.

Table 4.2 lists the comparator response time for typical design parameters. A slope of 0.25 $\text{V}/\mu\text{s}$ is assumed, which means that a 500 MHz ADC with dual-edge counters will cover a 1 V ramp range for

12 bit codes in about $4 \mu\text{s}$. Counters take a decision on both edges of the 500 MHz clock, so every 1 ns. The response time of the comparator is much larger than this count period of 1 ns, namely 59 ns. The response time is also much larger than the OTA time constant τ_0 which means that the condition is fulfilled for which Equation (4.10) is valid and the comparator operates in steady-state.

The slow response time of the comparator is not a problem as long as the counters and ADC ramp foresee enough clock cycles to cover the entire range. Variation in delays between comparators in different columns will result in a spread of the comparator response time amongst columns. But this will be cancelled by the digital CDS in the ADC. The response time will also slow down with lower ADC ramp slope m_{rc} . A lower slope is sometimes used to increase the ADC gain. Sufficient count overhead range in the counters must be available to realize digital CDS for all ramp slope values.

A noise analysis for comparator-based circuits is described in [29], where it is shown that for a longer response time of the comparator, the noise bandwidth is lower if the comparator is in a transient regime. For response times longer than τ_0 the noise bandwidth approaches $1/4\tau_0$ which is the lowest value and is the classical noise bandwidth of an 1st order OTA in steady state. With steep ramp slopes, the comparator will typically be operated in this steady-state regime.

As shown in Equation (4.10), the response time is longer if the slope m_{rc} of the ramp signal is lower. The ADC has a higher gain (in $\text{DN}/\mu\text{V}$) with a lower slope. The comparator circuit can also be optimized to reach a lower read noise thanks to the relation between response time and noise bandwidth. With a lower ADC slope, the OTA bias current can be reduced. The OTA time constant τ_0 will rise with a lower bias current, due to the inverse relation between R_0 and the bias current. This will lower the noise bandwidth and hence the integrated comparator noise. The OTA bias current can be reduced to reach a lower noise level when operating with a slower ramp slope (and higher ADC gain), as long as the total comparator delay is below the maximum range that is in range for the digital CDS. So the ADC can provide an additional gain by reducing the ramp slope, and temporal noise can be reduced at low slopes by reducing the OTA bias current. In a practical

CIS design, the noise in the readout chain is dominated by $1/f$, RTS and thermal noise of the pixel source follower. Input-referred noise of the column stage is also further lowered by the pre-amplifier and dual CDS [16]. This relaxes noise requirements on the comparator.

Extending the comparator delay over multiple clock cycles is a way to fasten the AD conversion, but it is not compatible with a multi-slope ADC, where the ramp slope is changed for larger signal levels so that the quantization noise follows the shot noise of the pixel signal. A linear ramp signal is required because a change in slope would void the correction of the comparator delay during the digital CDS AD conversion process.

4.3 Ramp Generator

The usable output range of a typical pixel signal, at the pixel column bus, is about 1 V. The spread on the pixel values, including offset variation due to mismatch and temporal noise, can be up to 200 mV. The ramp needs to cover this voltage range (output range and spread) in the foreseen time. Some extra overhead ramp swing is needed to cover the comparator response time, which can also be several tens of clock cycles, as discussed above.

For an ADC with digital CDS, the reference ramp cycle can be shorter, as it only needs to cover the temporal and fixed pattern noise of the pixel, and the comparator response time. Often, the pixel active signal has been pre-processed by a pre-amplifier, which does provide a first analog CDS. The residual spread after this circuit, which needs to be converted in a dual CDS architecture, is the column amplifier offset variation and temporal noise. A range of 200–300 mV is typically sufficient.

For staircase-based ramp generators, several ramp generator circuits have already been discussed, such as voltage DAC, and single-ended and differential switched-capacitor integrators [36]. DACs can control the slope very easily, as used for example in a multi-slope architecture.

But as explained, the continuous sawtooth ramp reference signal allows to considerably speed up the AD conversion. Several circuits can be used to generate the ramp signal and distribute it. An implementation

Figure 4.3: Ramp generator and distribution of ramp voltage to the columns.

with a DAC and an integrator is proposed in [36]. Another simple implementation sinks a stable reference current onto an integration capacitor. The capacitor may be distributed inside the columns. Also the current sources can be distributed. Figure 4.3 shows a simple ramp generator realized by current mirrors and integration capacitors present in every column. The current mirror bias is adjusted by a switched capacitor circuit, which is a circuit in the periphery of the chip and shown at the left side of Figure 4.3. The frequency of the non-overlapping clocks ϕ and ϕ_{inv} controls the bias current. The opamp is connected to a stable bandgap reference voltage V_{bg} and ensures low temperature drift on the generated ramp signal. The ramp signal is generated by a distributed current integration on in-column capacitors. The capacitors may be present in every column or in a set of columns. An initialization switch connects the capacitors to a reference voltage V_{start} before the start of the current integration (and the ramp sloping). The distributed capacitors can be shorted together to make the response more uniform amongst the columns (as shown by the red dashed line).

The switched capacitor (SC) circuit controls the bias current, which scales proportionally with the frequency of the SC circuit. If the clock frequency of the SC circuit is proportional to the ADC clock, the ADC gain is invariant to its clock frequency. In that case, a faster clock proportionally increases both the ramp slope and the counter clock frequency, which keeps the AD gain (in DN/V) constant. To reduce

power consumption for operation at lower frame rate, the clock frequency can be reduced without much impact on the characteristics of the CIS.

In case when an inverted ramp signal is required, for example if there is no inverting pre-amplifier between the ADC and the pixel column bus, the capacitors are charged at the initialization phase of the ramp and discharged by a similar (but complementary) circuit as shown in Figure 4.3.

The ramp signal must be linear to ensure a linear response of the pixel signal. The non-linearity in the readout chain should be dominated by effects inside the pixel, like the body effect on the source follower and the voltage dependency of the junction capacitance of the floating diffusion. An integrated non-linearity below 2% over the entire ramp range is typically acceptable.

The ramp can also cause row-wise noise effects. To analyze the noise on the ramp signal, two separate effects need to be distinguished:

- integrated noise on the ramp signal capacitor from the current source, and
- temporal noise on the ramp initialization level.

4.3.1 Integrated Noise on the Ramp Signal

The ramp itself integrates a constant current during a specific time. The random walk noise process associated with this, has been extensively described in literature [19], [29]. The ramp generator works in non-stationary mode, and the random walk noise (or shot noise) on the current source will cause more spread on the ramp signal with the square root of the time. The following relation is obtained [19]:

$$\langle V_{rc,n}^2 \rangle = (2kTg_o t)/C_r \quad (4.12)$$

where g_o is the output impedance of the current source and C_r is the capacitance of the ramp signal node. For a 10 pF ramp signal capacitance, and 2.25 μ A integration current, 27 μ V RMS noise is integrated in 1 μ s and 87 μ V RMS in 10 μ s.

In regular cases, C_r is large, in particular when the node is shared amongst all columns. And this noise is an order of magnitude lower

than the shot noise on the pixel signal. So it will not be observed. But for specific architectures, e.g., with an individual ramp generator per column, this noise can bring a minimum limit to the value of the integration capacitor C_r . For pixels with large full well charge, and a good SNR, it must also be verified that this noise source is still negligible.

4.3.2 Temporal Noise on the Ramp Initialization Level

Temporal noise on the ramp initialization level is critical since it is not cancelled by the digital CDS operation in the ADC. Moreover, the uncorrelated reset levels of the ramp during reference and active signal conversion will double the noise power. Since this causes a row-wise temporal noise, it can be very visible. A level below 10% of the temporal pixel noise is required to ensure that this row noise is not visible (as was shown in Figure 2.3). Hence, the noise level on the ramp initialization level must maximum be 10% of the pixel noise or better. With a typical column-referred noise level of $80\ \mu\text{V RMS}$, the temporal noise on the row references and ramp initialization levels must be below $8\ \mu\text{V RMS}$. This can be achieved with reasonable power consumption thanks to the large capacitive load of the distributed reference lines and the relatively low bandwidth requirements. Alternatively, some reference signals can be converted by the column ADC in some extra “dummy” columns, but these must in their turn be very low noise references. A black reference pixel will just replace the row noise by the pixel noise. In that case, the average of at least 200 pixels are required to reduce the row noise to an invisible level. And single outlier defect pixels in this dark pixel set have to be filtered out.

4.3.3 Comparator-Ramp Signal Coupling

When the ramp is generated by integrating a fixed current on the capacitors, it is required that the capacitance remains constant and independent of the voltage across the capacitor, to generate a linear slope. While this is the case for the circuit capacitors, this is not necessarily so for the input capacitance of the comparator. A comparator is composed of a differential pair. In a comparator design with a classical nMOS

differential pair and with sufficiently different input voltages on the gates of the differential pair, the transistor with the highest gate voltage will conduct all current. The nMOS transistor that conducts the current has a higher gate-channel capacitance than the nMOS transistor that is not conducting and of which the channel is depleted. At the start of the ramp, in all columns, the same transistor of the differential pair will conduct the entire comparator bias current. If the ramp is lower than the signal level, all conducting transistors are connected to the pixel signal input node, and not to the node distributing the ramp signal. But when a comparator toggles, the current will switch to the other transistor of the differential pair. The capacitance of the ramp signal node will gradually rise as more and more comparators toggle. This can cause row banding effects and a non-linearity which depends on the number of bright/dark pixels on a row. In the case when many pixels have a high signal on the same column (e.g., due to the presence of a large white area in the image), it will take longer before the comparator toggles. The effective capacitance of the integration node of the ramp generator remains higher for a longer time, than when the row has a dark signal and all columns did toggle early during the ramp slope. This can shift the slope of the ramp and change the toggling point for the signal levels on the same row. It is mostly noticeable in dark areas. The offset of the pixels in a dark area will depend on the amount of white pixels on that row. This effect is often referred to as “row banding”. The described effect is one reason for row banding, there are also many other reasons which can cause row banding. Even small amounts of row banding are noticeable to the human eye.

A second problem that can cause a similar visual effect, is that the drain side of the comparator nMOS transistors can shift over a large voltage range at the moment when the comparator toggles. That drain is coupled by the nMOS gate-drain overlap capacitor C_{gd} to the ramp, as shown in Figure 4.4. This also causes changes to the ramp capacitor as well as potential glitches on the ramp signal. If many columns have similar signal levels (like a row of dark pixels), the glitch will be larger than when there is a large variety of signal levels on the row. The effect will also change depending on the data content on the row and this effect be another source of “row banding”.

Because of the high clock frequencies, the power dissipation in the counters is considerable and often dominates the total power consumption of the image sensor. In a ripple counter, most power is consumed by the first flipflop. Furthermore, the power consumption is largely signal-dependent. When the counters stop counting, the power dissipation drops. In an image sensor, there can be several thousand columns, each containing such a counter, and IR drops may occur in the routing of the power supply to the columns. If the power consumption drops, this can cause signal-dependent artefacts. Effects like signal-dependent clock jitter or signal-dependent ground coupling can cause visible artifacts in the image. It is therefore important to reduce power consumption and to keep power consumption constant insofar possible. A scheme using two counters per column, operating at opposite clock edges has been proposed to keep power consumption constant [22]. One counter clocks from the start of the ramp until the comparator toggles. Then the other counter takes over. Since the second counter can be clocked on the other clock edge, the ADC will also get an additional bit.

To reduce the power consumption, quite a few solutions have been proposed. One solution is to use two counters, of which the first counter is operated as described earlier, but counts only the most significant bits. For the least significant bits, a separate high-frequency counter is used that is only enabled after the ramp crossing [9]. A hybrid solution with latches for the 4 LSB working with a counter per group of columns, and regular counters for the 10 MSB was also proposed [35].

For further speed increase, also solutions have been proposed. A local clock generation in each column can solve the clock distribution bottleneck [4]. A DLL circuit can create extra timesteps within the clock period during which the comparator toggles can be detected [20]. A combination of a 2 bit LSB gray counters and a 9 bit ripple counter for the MSB (and overflow) was also recently proposed [17]. Each of the cells of the gray counter runs only at $\frac{1}{4}$ of the frequency of the LSB cell of a ripple counter.

Table 4.3: Power breakdown for counting signal slope ADC with typical performance

Circuit Block	Current Consumption [μA]	Supply Voltage [V]	Power Dissipation [μW]
Comparator stage 1	4	3.3	13.2
Comparator stage 2	1	3.3	3.3
Counter	7.5	1.5	11.2
Clock distribution	1.8	1.5	2.7
Total power/column			30.4

4.5 Column ADC Power Breakdown

Table 4.3 shows the power breakdown for a typical counting single-slope column ADC.

A counter clock frequency of 500 MHz is assumed, for which the comparator current consumption was already calculated in Table 4.2. The ADC counters clock on both the rising and falling edge of the clock, which means that counting all 2^{12} codes takes $4.096 \mu\text{s}$. About 200 extra digital codes must be added as overhead for the comparator delay and the offset variation range of the PGA. The conversion of the pixel reset signal takes another 1024 codes. The total counting time per row is $5.32 \mu\text{s}$. On top of this, about $2 \mu\text{s}$ must be added to reset the ramp signal. A 12 bit conversion with digital CDS takes $7.32 \mu\text{s}$. With such speed, 60 frames/s can be read out in an image sensor with 3840×2160 pixels, as typically used for 4 K video, for example.

Only the first flipflop of the column ripple counter clocks at the maximum clock frequency. In a ripple counter, the flipflop of the i th bit clocks at $1/2^i$ of the flipflop of the first bit. The power dissipation of all flipflops is together is:

$$f_{cl} \cdot C_{ff} \cdot V_{dd}^2, \quad (4.13)$$

where C_{ff} is the capacitive load inside one counter flipflop. For the power consumption in the clock distribution, a load C_{cl} of 5 fF per column for each clock is estimated, with a total power consumption of:

$$0.5 \cdot f_{cl} \cdot C_{cl} \cdot V_{dd}^2. \quad (4.14)$$

The power breakdown shows that for a typical architecture, the power consumption is about equal between the analog comparator stage and the digital counting logic. Various optimizations can be done to improve power consumption in the counter or the comparator, depending on the requirements of the image sensor.

5

Future Outlook

What can be the next steps in the development of the single-slope ADC for CIS? A further speed increase is definitely required, driven by market requirements for further resolution increase and faster frame rates. And solutions for lower read noise are demanded, to realize image sensors with deep sub-electron readout noise and devices with excellent low-light performance. And when the temporal noise improves, also the fixed pattern noises or structural artefacts need to be reduced to preserve an acceptable ratio between temporally varying noise and hidden fixed structural patterns in an image. Other applications demand more on-chip processing, and may ask for ADCs which can be operated with much flexibility, e.g., fast adjustment of ADC gain, bit resolution or readout speed, or random pixel access.

A first attempt to make the pixel-ADC structure more compact is to replace the in-pixel source-follower by one part of the input pair of the comparator (called part A). The second part of the input pair of the comparator can then be found in a direct neighbouring pixel (called part B) located on the next row of the imaging array [28]. When part A is readout, the sawtooth ramp for the ADC is fed into part B, when part B is readout, the sawtooth ramp for the ADC is fed into part A. The

main motivation for this change is noise reduction. Since the in-pixel comparator replaces the pixel source follower, one of the noise sources of the classical readout chain is eliminated.

The introduction of stacking technology for CMOS image sensors has opened new options and possibilities for the column-level ADCs as well. Having the ADCs on the “logic” layer has several advantages:

- physical space is no longer an issue, because on the second or logic layer there is plenty of silicon real estate available to include the column-level ADCs. The wealth on space can be used to provide every column with two SS-ADCs, fully in parallel. Averaging the outcome of the two conversions can gain a factor $2^{0.5}$ in temporal noise performance [33],
- the logic layer can be realized in a more aggressive CMOS technology. In this way the ADCs can more compact, be faster and/or consume less power,
- the combination of stacking with hybrid bonding does allow to move from column-level ADC to pixel-level ADC. Pixel-level ADCs have several extra advantages such as global-shutter operation, high-speed operation, having the pixel information immediately available in digital format. A major problem for high-speed imaging in combination with high resolution is the challenge to get all the digital data off chip, and in a first step, outside of the pixel array.

6

Summary and Conclusions

Today single slope analog-to-digital converters are widespread and several solutions have been implemented to increase the readout speed. The use of a sawtooth ramp signal decoupled the comparator response time from the ADC clock frequency. This can be elegantly combined with counter circuits to realize digital CDS, often as a second CDS stage for further noise and uniformity improvements. Other speed improvements came from architectural optimizations, such as the use of multiple slopes or multiple ramps. In the fastest architectures and for large resolution arrays, the column counters dissipate a considerable amount of power. Several solutions have been proposed to reduce power requirements and make current consumption constant throughout the conversion process.

List of Symbols

C : initial counter value

C_{cl} : capacitance of the clock node in the column ADC counter

C_{FD} : floating diffusion capacitance

C_f : feedback capacitor of a programmable gain amplifier

C_{ff} : internal capacitive load of one flipflop in the column ADC counter

C_{gd} : gate-drain overlap capacitance

C_i : input capacitor of a programmable gain amplifier

C_L : load capacitance of the 1st stage of the comparator

C_r : capacitance of the ramp signal node

C_{rs} : sample capacitor for the pixel reset signal

C_{ss} : sample capacitor for the photon-generated signal of the pixel

C_{sc} : capacitor in a switched capacitor circuit

DCNU: dark-current non-uniformity

DSNU: dark signal non-uniformity

e_{reset} : quantization error for the reset signal conversion

e_{signal} : quantization error for the photon-generated signal conversion

G_m : transconductance

g_o : output impedance of current source

i : random column number ($1 \leq i \leq k$)

i_c : output current comparator

f_{cl} : ADC clock

f_{comp} : bandwidth of the comparator

k : number of pixels in horizontal direction

l : number of pixels in vertical direction

m_{rc} : slope of the ramp reference signal of the SS-ADC

n : number of bits of the SS-ADC

N_e : number of generated and collected electrons within the exposure time

N_{ph} : number of incoming photons within the exposure time

OSR: oversampling ratio

P : number of bits in a coarse conversion

PPD: pinned-photodiode

PRNU: photon-response non-uniformity

q : number of bits of the address bus ($2^q = k$)

r : oversampling rate in the case of multiple sampling

R_o : output impedance of the 1st stage of the comparator

RS : row select pulse

RST : reset gate pulse

SF : source follower

$SNR_{\max}$: maximum signal-to-noise ratio

t_1, t_2 : time points at which V_1 and V_2 are converted

t : time

t_c : conversion time of a single pixel

t_{cl} : clock period

t_{comp} : delay time of the comparator

TG : transfer gate pulse

$t_{l,h}$: hold time of a latch

$t_{l,s}$: setup time of a latch

t_r : readout time for all bits of a single pixel

t_{ramp} : ramp settling time

t_{res} : response time of the comparator

V_1, V_2 : analog voltages

V_{bg} : bandgap reference voltage

V_{dd} : digital supply voltage

V_p : output signal of the pixel

V_{PGA} : output of the programmable gain amplifier

V_{rc} : ramp reference signal

V_{ref} : DC reference voltage

V_{reset} : reference signal of the pixel

V_{signal} : photon-generated signal of the pixel or active signal

V_{start} : reference voltage, initial start level of the ramp generator capacitors

V_t : threshold voltage of an inverter

x_{reset} : amount of counts during reset conversion

x_{signal} : amount of counts during reset conversion

$X(s)$: Laplace transform of the OTA input

$y[u]$: output of the ADC for the u -th conversion cycle

$Y(s)$: Laplace transform of the OTA output

ϕ : switch symbol

ϕ_{inv} : switch symbol

σ_{col} : noise on column level

σ_{pix} : noise on pixel level

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