SMU

1.28 and 5.12 Gbps multi-channel twinax cable receiver ASICs

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Outline

- The data transmission of ATLAS ITK Pixel detector
- GBCR1 design and test results
- GBCR2 design and simulation results
- Summary

ATLAS ITK Pixel detector

The ATLAS Phase-II Inner Tracker ITk

- The pixel sensor readout chip (RD53B), developed by CERN RD53 collaboration, sends data at 1.28 Gbps for each data lane.
- This readout scheme is dictated by the detector design, powering scheme and budget, and radiation level in the operation.

schematic layout of ATLAS ITk

Data transmission with “active cable”

- The “active cable” include an Aggregator chip as a transmitter, a Twinax cable and GBCR receiver chip to equalize high-frequency loss
- The Twinax cable length is up to 5 meters and its diameter is AWG34.

GBCR1 top level diagram

- 4 uplink channels work at 5.12 Gbps. 1 downlink channel works at 2.56 Gbps.
- Each uplink channel has a Clock and Data Recovery (CDR) to retime the equalized signal.
- The CDR is a re-use of the design from IpGBT, a Low Power Giga Bit Transceiver developed by CERN, and its frequency detector (FD) is removed so that it can be locked at 5.12 Gbps, 2.56 Gbps and 1.28 Gbps

AWG34 Twinax cable models

Length↵	Type↵	Source↵
1m↵	<u>Twinax</u> , AWG34↵	LBNL↵
3m↵	<u>Twinax</u> , AWG34↵	LBNL↵
4m↵	<u>Twinax</u> , AWG34↵	LBNL↵
5m↵	<u>Twinax</u> , AWG34↵	SLAC↵
5m↵	<u>Twinax</u> , AWG34↵	LBNL↵
6m↵	<u>Twinax</u> , AWG34↵	LBNL↵
6m↵	<u>Twinax</u> , AWG34↵	University of Bonn↵

- The AWG 34 Twinax models are based on the measured 4-port S-parameter files.
- The models are contributed from several institutes.

The signal loss of 5-m AWG34 Twinax cable

- DC gain is about -8.1 dB and Gain@2.56 GHz = -24.9 dB
- The maximum peaking strength required is about 16.8 dB

The uplink channel in GBCR1

- ❑ 2 Stages of CTLE and 3 Stages of LA
- ❑ All the transistors are ELT devices.
- ❑ The equalization can be turned off
- ❑ The power consumption of the equalizer is 6 mA.

GBCR1 Test Setup

Instruments Model:

Oscilloscope: Tektronix DSA70804B

Twinax cable length: 6 meters

Power Supply: Agilent E3641A

Signal Generator: CENTELLAX TG1C1-A & CENTELLAX PCB12500

Probe: 13 GHz differential probe, Tektronix P7313SMA

The input signal eye diagram @5.12Gbps

The eye diagram from signal generator

The eye after 5m Twinax cable

Typical output signal eye diagram @5.12Gbps

Total Jitter = 79.3 ps
RJ = 4.3 ps
DJ = 24.9 ps

Total Jitter = 35.5 ps
RJ = 1.5 ps
DJ = 16.4 ps

Direct data transmission

- New baseline from the collaboration: The ASIC Aggregator is removed and GBCR2 is straightly connected to the RD53B in the detector through a combo that combines a flex cable and a Twinax cable.
- The data rate of uplink channel decrease to 1.28 Gbps.
- The requirements of IpGBT ePort: < 200 ps (pk-pk) jitter and > 140 mV differential amplitude.
- We have tighter power budget requirement of the optical box (<100 mW, up to 6 channels).

GBCR2 top level diagram and layout

- Instead of using CDR, a phase shifter, adapted from IpGBT, is used to generate the retiming clock to save power
- The re-timing logic can be bypassed for test purpose or to save power especially when cable length is short.

Flex PCB models

Length↵	Type↵	Source↵
10cm↵	Flex↵	LAPP↵
45cm↵	Flex↵	LAPP↵
50cm↵	Flex↵	University of Bonn↵
80cm↵	Flex↵	University of Bonn↵
1m↵	Flex↵	University of Bonn↵

L3 AX-BSF flex cable

- Beside the Twinax cable model, the Flex PCB models are needed for direct transmission.
- The Flex length depends on the location of the connectors.

The signal loss of 6-m cable plus 1m Flex

- We divide the signal loss curve in 3 ranges:
- High Frequency range: 0.4-1.3 GHz, slope is 27.3 dB/decade, need a multiple order CTLE
- Middle Frequency range: 0.2 to 0.4 GHz, slope is 14.3 dB/decade , one order CTLE
- Low Frequency range: 0.8 to 0.2 GHz, slope is 8.5 dB/decade, one order CTLE

The equalizer in GBCR2

- 3 stages of high frequency CTLE . Zero=540M, Pole1=1.5G
- 1 stage of medium frequency CTLE. Zero=170M, Pole1=450M
- 1 stage of low frequency CTLE. Zero=120M, Pole1=170M.

Uplink simulation in GBCR2

Eye after the 1-m Flex and 6-m Twinax cable

Eye after the equalizer (config: 4'b1011)

DC-offset cancellation in GBCR2

- A RC filter is used to filter the high-frequency signal and the DC-offset is amplified and feedback to input stage of LA.
- We expect that the DC-offset cancellation suppresses the DC-offset to a few mV.
- The low cut-off frequency is down to 115 KHz, not impact the encoded data transmission

Summary of two GBCR chips

Chip type	Operation mode	Jitter from cable+GBCR (ps)	Power consumption(mW)	DC-offset correction
GBCR1 (5.12 Gbps)	CDR on	35.5	308	No
	CDR off	79.9	120	No
GBCR2 (1.28 Gbps)	Equalizer mode	81	80	Yes
	Retiming mode	11	105	Yes

- For power consumption estimation, we count 4 channels in GBCR and 6 channels in GBCR2.
- GBCR2 was submitted in November 2019 and we expect to test it in Q1 of 2020.

Backup slides

Test eye diagram @ 1.28 Gbps

Jitter(pk-pk) is 26 ps.

- GBCR1 also works at 1.28 Gbps but power consumption is too large due to CDR.