Performance Comparison of s-Si, $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, Monolayer BP- and WS_2 -Based n-MOSFETs for Future Technology Nodes—Part II: Circuit-Level Comparison

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Abstract—The first part of this paper presented the device-level comparison of emerging materials ($\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and 2-D materials) and device architecture (NW FETs) with s-Si FinFETs. In order to further understand the performance and energy efficiency of these device options for future technology nodes, it is required to go beyond the device-level comparison by accounting for not only intrinsic but also the extrinsic parasitic elements. In this paper, we present the comparison of s-Si, $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, and 2-D material-based n-type MOSFETs using the circuit-level figure of merits across three successive future technology nodes. The analysis incorporates both device characteristics obtained from an advanced quantum mechanical simulation tool and circuit-level comparison, which accounts for device parasitic elements and wiring load. The results show that 2-D material DG MOSFETs present a more energy-efficient device option than s-Si and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ FinFETs in sub-0.7-V supply voltage regime and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ nanowire (NW) FETs can outperform s-Si multi-gate (MuG) FETs and 2-D material FETs, but when considering non-idealities, s-Si NW FETs remain both faster and more energy-efficient device option.

Index Terms—2-D materials, benchmarking, FinFETs, InGaAs , monolayer black phosphorus, monolayer WS_2 , MOSFET, NWFETs, parasitic capacitances, s-Si.

I. INTRODUCTION

THE device-level comparison of s-Si, $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, and 2-D material MOSFETs presented in the companion paper highlights the advantages and disadvantages of a given material or device architecture using the device-level figure of merits (FoMs). Using advanced quantum simula-

tions and a physical compact model, both emerging materials and advanced device architectures were compared from both ON-state current and intrinsic delay perspective across technology nodes, including the intrinsic device capacitance. However, the device-level comparison in the companion paper does not account for the extrinsic parasitic elements, which have been reported to become significant compared with the intrinsic device capacitance with the technology scaling [1].

Moreover, the relative contribution of extrinsic parasitic capacitances, such as device parasitic capacitances and wire load, is expected to increase for future technology nodes due to both gate length and interconnect scaling. Therefore, the extrinsic parasitic elements play an important role in the scaling of total capacitance and, thus, the energy consumption and delay of emerging devices with technology node down-scaling. In other words, a circuit-level comparison becomes a necessity to compare the performance of different device architectures, by accounting for the extrinsic parasitic elements. For the circuit-level comparison, a ring-oscillator (RO) circuit is widely used to characterize the speed and energy efficiency of the device options in early stages.

This paper is organized as follows. Section II presents the validation of the physics-based analytical model, which was discussed in the companion paper. In order to proceed toward circuit-level simulations with the analytical model, Section III introduces the extrinsic parasitic components, which are then added to the analytical model. Furthermore, a circuit-level comparison of all the device options using RO simulations is discussed in Section IV. Section V concludes this paper highlighting the advantages and disadvantages of 2-D material DG FETs over s-Si and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ multi-gate (MuG) FETs for future technology nodes.

II. BRIDGING THE DEVICE SIMULATIONS AND EXPERIMENTS

Before delving into the circuit-level comparison, it is important to bridge the device simulations presented in the companion paper to the state-of-the-art experimental results using the mentioned physics-based analytical model [2]. The physics-based analytical model, which is valid in both quasi-ballistic and diffusive transport regimes, not only provides an insight into experimental and simulation results but

Manuscript received April 23, 2019; accepted June 10, 2019. The review of this paper was arranged by Editor L. Ge. (Corresponding author: Tarun Kumar Agarwal.)

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Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TED.2019.2923820

Fig. 1. Bridging the simulation and experimental data for different materials. (a) (left) Experimental Si FinFET [3] (circle) and modeled (solid line) transfer characteristics ($L_G = 20$ nm); (right) simulated ballistic (dashed line) and scattering (circle) with modeled (solid line) transfer characteristics ($L_G = 11.5$ nm). (b) (left) Experimental $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ FinFET [4] (circle) and modeled (solid line) transfer characteristics ($L_G = 30$ nm); (right) simulated ballistic (dashed line) and modeled (solid line) transfer characteristics ($L_G = 11.5$ nm). (c) (left) Experimental WS_2 FET [5] (circle) and modeled (solid line) transfer characteristics ($L_G = 2$ μm); (right) simulated diffusive [6] (circle) and modeled (solid line) transfer characteristics ($L_G = 10.5$ nm).

TABLE I

COMPARISON OF PHYSICAL MODEL PARAMETERS, SUCH AS GATE CAPACITANCE (C_{INV}), LONG-CHANNEL INTRINSIC MOBILITY (μ_{INT}), AND CONTACT RESISTANCES (R_S/R_D), CORRESPONDING TO THE EXPERIMENTAL AND SIMULATION DATA SHOWN IN **Fig. 1**

	s-Si FinFET		InGaAs FinFET		WS ₂ FET	
	Exp.	Sim.	Exp.	Sim.	Exp.	Sim.
C_{inv} ($\mu\text{F}/\text{cm}^2$)	2.1	3.6	1.2	2.1	0.0105	4.3
μ_{int} ($\text{cm}^2/\text{V.s}$)	180	680	1100	4500	163	900
R_S/R_D ($\Omega\cdot\mu\text{m}$)	130	—	180	—	1.25k	—

also helps in quantifying the gap between experiments and simulations with respect to important physical parameters, such as mobility, gate capacitance, and contact resistances. **Fig. 1** exhibits the agreement between the transfer characteristics from experiments/simulations and the analytical model for different materials. It should be noted that the experimental data are exclusively used to show the versatility of the analytical model and not for the circuit-level comparison. The performance comparison presented in Section IV uses the results from quantum simulations discussed in the first part of this paper. **Fig. 1(a)** shows Intel 14-nm Si FinFET experimental data and the modeled transfer characteristics (in log scale). Furthermore, the simulated N7 s-Si FinFET transfer characteristics, both ballistic (full-curve) and with electron-phonon scattering (few bias points), are shown in a linear scale with the modeled transfer characteristics. As shown in **Fig. 1(c)**, a disagreement can be observed in the modeled moderate inversion region of WS_2 -based back-gated experimental device. This is due to the dependence of the contact resistance on the applied back-gate bias, which needs to be obtained from the transmission-line-method (TLM) measurements. In the absence of these measurements, the fixed contact resistance is used in the analytical model, which leads to this discrepancy in the moderate inversion region of the experimental and modeled characteristics, as discussed in [2].

The extracted gate capacitances, mobility values, and contact resistance for all the experimental and simulated devices are shown in **Table I**. Although the extracted physical

parameters from experiments may be coupled, it can be clearly seen that the physical model parameters obtained from quantum simulations are more optimistic compared with the experimentally reported device options. The higher values of gate capacitance indicate that the effective-oxide-thicknesses (EOTs) considered in the simulation study are aggressively scaled to maintain electrostatics at smaller gate lengths compared with the experimental ones. The calculated mobility values are more promising than the experimentally reported values because of both higher stress values considered in the simulation study and the exclusion of the other scattering mechanisms besides electron-phonon scattering, such as impurity and surface roughness scattering. As mentioned in the companion paper, the improvement in the contact resistivity is based on the requirements of future technology nodes. Nevertheless, as recent experimental demonstrations have shown great promise, it can be expected that the gate capacitance in experimental devices can be further improved by scaling EOT below 1 nm, while the mobility is expected to increase by stress engineering in Si FinFETs and interface engineering in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ FinFETs [3], [4]. Lower contact resistivities have been demonstrated for Si and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ FinFET using higher Epi doping concentrations and *in situ* doping techniques, respectively [7], [8]. For 2-D material FETs, preserving the intrinsic material quality by capping the 2-D material and finding reliable methods for extension doping can result in higher mobility and lower contact resistances, respectively [5], [9]. The impact of these non-idealities (lower mobility values and higher contact resistivities) on circuit-level metrics is discussed at the end of Section IV.

III. EXTRINSIC PARASITIC MODELING

In this section, we focus on the modeling of the parasitic components due to front-end-of-line (FEOL) and back-end-of-line (BEOL) while the intrinsic gate-to-channel capacitance has been calculated using the quantum simulations, as discussed in the companion paper.

Fig. 2. Cross section of different device architectures showing the parasitic capacitances in (a) double-gate FET, (b) FinFET, and (c) vertically stacked NW FETs with $\epsilon_{sp} = 3.9$, $H_G = 2 \times L_G$, $H_{Epi} = 0.67 \times H_G$, $H_{M1} = 15$ nm, and other device parameters as given in Table II from the companion paper.

TABLE II

TECHNOLOGY AND DEVICE PARAMETERS ACROSS TECHNOLOGY NODES (N7, N5, AND N3). CGP, FP, N_{fin} , W_{foot} , T_{sp} , AND V_{DD} DENOTE THE CONTACTED GATE PITCH, FIN PITCH, NUMBER OF FINs, DEVICE FOOTPRINT, SPACER THICKNESS, AND SUPPLY VOLTAGE, RESPECTIVELY. HERE, ALL PHYSICAL DIMENSIONS ARE EXPRESSED IN nm

	CGP	L_G	T_{ch}	FP	N_{fin}	H_{fin}	W_{foot}	T_{ox}	T_{sp}	V_{DD} (V)
N7	42	11.5	4.6	24	3	25	52.6	3.2	10	0.61
N5	32	9.0	3.6	18	3	25	39.6	2.9	8	0.58
N3	25	7.0	2.8	14	3	25	30.8	2.6	6	0.56

A. Device Parasitic Capacitances

To account for the FEOL device parasitic capacitances, the cross sections of the planar DG, Fin, and nanowire (NW) FETs are shown in Fig. 2. To model these parasitic capacitances, the analytical equations developed for planar double-gate and MuG device architectures are used, which have been validated with numerical simulations [10], [11]. For the planar double-gate device, the outer fringing capacitances (C_{of}) and the gate contact to source/drain contact capacitance (C_{pcca}) are considered due to the top gate, and only C_{of} is considered due to the bottom gate, as shown in Fig. 2(a). It should be noted that there can be an additional parasitic capacitances due to the metal connection (orthogonal to the channel) of top and bottom gates in monolayer WS_2 and black-phosphorus double-gate FETs. However, the contribution of this capacitance component is estimated to be rather small compared with C_{pcca} because of the atomically thin body of 2-D materials. Fig. 2(b) and (c) exhibits the outer fringing capacitance for the Fin (C_{gfin}) and NW FETs (C_{gNW}), respectively. Similar to C_{pcca} in the planar device architectures, Fig. 2(b) also shows the gate contact to source/drain contact in two parts: 1) gate-to-epi capacitance (C_{gepi}) and 2) gate-to-contact (C_{gcont}). Here, the contact refers to an M1 contact over Epi. Furthermore, as shown in Fig. 2(c), the stacked NW device architecture consists of inter NW capacitances (C_{gNWb}) in addition to the FinFET device parasitics. C_{gNWb} depends on the vertical spacing between the stacked NWs denoted as SpaceNW. As shown in Fig. 3(a) and (b), C_{gfin} or C_{gNW} is composed of the fringing capacitance from different sides, i.e., top-gate to Fin/NW ($C_{gfin\text{top}}/C_{gNW\text{top}}$), both sides of the

gate to Fin/NW ($C_{gfin\text{side}}/C_{gNW\text{side}}$), both top corners of the gate to Fin/NW ($C_{gfin\text{corner}}/C_{gNW\text{corner}}$), and both bottom edges of the gate to Fin/NW ($C_{gfin\text{bottom}}/C_{gNW\text{bottom}}$).

Fig. 3(c) shows the breakup of total device parasitic capacitances (C_{par}) in planar DG, Fin, and NW FETs with technology node scaling. Here, C_{par} has three components as mentioned in the previous paragraph: 1) outer fringing capacitance ($C_{of}/C_{gfin}/C_{gNW}$); 2) gate-to-source/drain contact capacitance (C_{pcca}/C_{gcont}); and 3) gate-to-Epi contact in Fin and NW FETs (C_{gepi}). It can be observed from Fig. 3(c) that C_{pcca} starts dominating in C_{par} breakup for DG FETs at N5, which further increases at N3 due to the gate-pitch (CGP) scaling. This indicates the importance of optimizing the spacer thickness to minimize C_{pcca} at smaller CGP. Furthermore, C_{of} shows a good scaling of $\sim 0.7\times$ in DG FETs owing to the scaling in the device width contrary to FinFETs because of their fixed fin height. Moreover, C_{of} in NW FETs manifests a similar scaling as DG FETs because of the device width scaling caused by the channel thickness reduction with technology nodes. Thus, NW FETs show a very good scaling ($\sim 0.8\times$) of total device parasitic capacitances compared with FinFETs and DG FETs. It should be noted that Fig. 3(c) shows the scalar values of parasitic capacitances, while the effective value of C_{par} will be extracted from RO simulations, which inherently accounts for the capacitance increase due to the Miller effect.

B. BEOL Parasitic Components

With the increasing importance of interconnect parasitics over device parasitics, it becomes necessary to include them in the RO simulations. To represent the interconnect

Fig. 3. Device parasitic capacitances. (a) Outer fringing capacitance in FinFETs. (b) Outer fringing capacitance in stacked NW FETs. (c) Breakup of total device parasitic capacitance (C_{par}) for DG, Fin, and stacked NW FETs (with two vertically stacked NWs).

Fig. 4. Comparison of (a) effective capacitance (C_{eff}), (b) delay, and (c) energy-consumption for 2-D materials-based FETs and s-Si/ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ -based Fin/NW FETs, obtained from RO simulations.

between each RO stage in SPICE simulations, we use a transmission-line (T-) model of a lumped RC network [15]. Here, the resistance (R_w) and the capacitance (C_w) per unit length of an interconnect wire are calculated according to International Technology Roadmap for Semiconductors guidelines. For an average $50 \times \text{CGP}$ long wire length, we take $R_w = 317.4 \, \Omega/\mu\text{m}$ and $C_w = 0.27 \, \text{fF}/\mu\text{m}$ to benchmark all the investigated device options. The total interconnect resistance and capacitance show a scaling of $\sim 0.77\times$ owing to the gate pitch reduction with the technology node scaling.

IV. CIRCUIT-LEVEL COMPARISON

In this section, we benchmark the chosen device options using a 15-stage RO with a fan-out of three, including the effect of parasitic resistive and capacitive components [12]. We would like to emphasize that the nFETs and pFETs are assumed to be balanced in the RO. Therefore, the performance metrics obtained here indicate the performance of nMOSFET across different materials and device architectures. Fig. 4(a)

reports the breakup of different capacitive components (channel, device parasitic, and wire load) extracted from the RO simulations for the chosen device options across different technology nodes. The results indicate that the total capacitance scales well ($\sim 0.7\times$) with technology node scaling in both DG WS_2 FETs and stacked NW FETs. On the other hand, FinFET device architectures display a lower capacitance scaling because of a negligible reduction in the gate-to-channel capacitance with the technology node scaling due to the fixed fin height. Fig. 4(b) and (c) exhibits the RO delay and energy consumption of all the device options across technology nodes. It can be seen from Fig. 4(b) that s-Si FinFETs exhibit better RO delay than $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ FinFETs with the technology node scaling, while $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ NW FETs have the best performance for the same technology parameters. This is because of better electrostatic control in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ NW FETs compared with $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ FinFETs, as discussed in the companion paper. Fig. 4(b) also shows that although monolayer BP FETs can match the performance of s-Si FinFETs at N7, it is increasingly

Fig. 5. Circuit-level comparison with (a) EDP across technology nodes and (b) and (c) EDP and delay with V_{DD} (ranging from 0.5 to 0.7 V in steps of 0.05 V) at N7 and N3 technology nodes, for 2-D materials-based DG FETs, s-Si, and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MuG FETs.

difficult to maintain the performance of 2-D FETs with the technology node scaling due to the planar architecture. Thus, for high-performance computing, it is preferable to use a device option with higher effective device width in a given footprint, given the dominance of wire load on the total device capacitance. From an energy perspective, Fig. 4(c) exhibits that 2-D FETs demonstrate lower energy consumption than MuG FETs owing to its planar architecture. Thus, combining both delay and energy consumption, Fig. 5(a) highlights an important circuit-level metric, the energy-delay product (EDP), to assess the energy efficiency of all the investigated device options with the technology node scaling. It is clearly shown that monolayer 2-D FETs are more energy-efficient device option for the same speed compared with modern s-Si FinFETs. To further understand the energy efficiency of 2-D FETs for a given performance, we calculate EDP with delay for different supply voltages for N7 and N3 technology nodes, as shown in Fig. 5(b) and (c). It is demonstrated that both 2-D FETs and NW FETs offer better EDP compared with FinFETs for supply voltages below 0.7 V. However, for supply voltages beyond 0.7 V, it is increasingly difficult to match the speed of the FinFET device structure with both 2-D material DG FETs and s-Si NW FETs. Furthermore, 2-D FETs are shown to significantly loose performance at scaled nodes, such as N3, due to ultra-scaled device footprints. It is important to note here that the performance gap between 3-D device architectures (Fin/NW FETs) and monolayer BP- or WS_2 -based DG FETs is expected to further increase when accounting for the technology relevant higher fin heights than considered here. On the other hand, the energy efficiency of monolayer BP- or WS_2 -based DG FETs further improves compared with taller fins or a higher number of stacked NWs. Among all device options, $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ NW FETs stand out with both better delay and EDP at both N7 and N3, considering the same interface and contact conditions in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and 2-D materials as s-Si.

As discussed earlier in Section II, the mobilities and contact resistances used in the device simulations are rather

optimistic compared with the experimentally reported ones. Therefore, it is important to discuss the effect of mobility and contact resistivity degradation in s-Si and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ on the energy consumption and delay of stacked NW FETs, as shown in Fig. 6(a) and (b). The degradation in the mobility of s-Si and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ is expected due to the interplay of other dominant scattering mechanisms besides electron-phonon scattering and interface traps in III-V materials. The electron mobilities of 380 and 1100 $\text{cm}^2/\text{V} \cdot \text{s}$ are extracted using the physics-based analytical model from recent experimental demonstrations for s-Si and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ FinFETs, respectively [3], [4]. The extracted mobility values serve as a lower limit in order to evaluate the effect of mobility degradation on s-Si and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ NW FETs. Fig. 6(a) shows that a mobility degradation of 67% in s-Si NW FETs can lead to $\sim 17\%$ increase in the delay for the same energy consumption. On the other hand, performance degradation of $\sim 17\%$ in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ NW FETs is caused by a mobility reduction of 89%. Furthermore, taking the non-ideal mobilities of 380 (s-Si) and 1100 ($\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$) $\text{cm}^2/\text{V} \cdot \text{s}$, Fig. 6(b) underlines the effect of contact resistivities for s-Si and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ NW FETs. It is shown that $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ NW FETs performs better than s-Si NW FETs, assuming the same contact resistivities for s-Si and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. However, the optimistic contact resistivities reported for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and 2-D materials tend to be $\sim 5\times$ and $\sim 9\times$ higher than s-Si, respectively [13], [14]. Furthermore, the non-ideal oxide and oxide/semiconductor interface can also change the energy-delay metric by reducing the effective gate-to-channel capacitance. Nevertheless, this issue is expected to subside with the constant improvement in the quality of channel materials and their interfaces with gate oxides. Thus, considering the mobilities (s-Si: 380, $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$: 1100, BP: 269, and WS_2 : 900 $\text{cm}^2/\text{V} \cdot \text{s}$) and contact resistivities (s-Si: 1×10^{-9} , $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$: 5×10^{-9} , and 2-D materials: $9 \times 10^{-9} \Omega \cdot \text{cm}^2$), Fig. 6(c) indicates that s-Si NW FETs are the fastest and most energy-efficient device options among all the investigated device architectures and materials. As the reported mobility

Fig. 6. Energy delay after including non-idealities for the N7 technology node. (a) and (b) Effect of mobility degradation and contact resistivities for s-Si and In_{0.53}Ga_{0.47}As stacked NW FETs. (c) Benchmarking of all the investigated device options combining respective mobilities and contact resistivities for s-Si, In_{0.53}Ga_{0.47}As, and 2-D materials. Here, V_{DD} is varying from 0.5 to 0.7 V in steps of 0.05 V.

values and contact resistances in 2-D materials continue to be an issue in 2-D materials community, it is important to note here that the lower mobility values or higher contact resistances with monolayer BP and WS₂ would further increase the performance gap between 2-D material DG FETs and s-Si MuG FETs.

V. CONCLUSION

In this paper, we have benchmarked emerging materials (In_{0.53}Ga_{0.47}As and 2-D) and device architectures (DG-, Fin-, and NW FETs) with conventional strained silicon FinFETs for three successive future technology nodes. Using quantum mechanical simulations, it has been shown that 2-D materials, such as monolayer BP, offer better ON-state currents compared with s-Si and In_{0.53}Ga_{0.47}As for planar double-gate architectures. In order to thoroughly compare 2-D FETs with FinFETs and NW FETs at the circuit level, intrinsic device characteristics obtained from a quantum transport tool have been coupled with a physics-based analytical model accounting for device parasitic components and wiring load. It has been demonstrated that 2-D FETs are more energy efficient than s-Si FinFETs in the sub-0.7-V regime for the same performance. For the same technology parameters, In_{0.53}Ga_{0.47}As NW FETs have been shown to be a faster and more energy-efficient alternative to s-Si MuG FETs. However, if non-idealities, such as interface traps and high contact resistivities in III-V materials, are not kept in check, s-Si NW FETs will remain the preferred device option at low supply voltages. To further enhance the performance of 2-D FETs, a tri-gate device architecture based on 2-D materials needs to be evaluated. Alternatively, by taking advantage of the lower thermal budget associated with 2-D materials, integrating 2-D FETs in a monolithic 3-D fashion could further boost their performance compared with Si MuG FETs.

REFERENCES

- [1] Y. Cao, T. Sato, M. Orshansky, D. Sylvester, and C. Hu, "New paradigm of predictive MOSFET and interconnect modeling for early circuit simulation," in *Proc. IEEE Custom Integr. Circuits Conf.*, May 2000, pp. 201–204. doi: [10.1109/CICC.2000.852648](https://doi.org/10.1109/CICC.2000.852648).
- [2] T. Agarwal *et al.*, "Benchmarking of Monolithic 3D Integrated MX₂ FETs with Si FinFETs," in *IEDM Tech. Dig.*, Dec. 2017, pp. 5–7. doi: [10.1109/IEDM.2017.8268336](https://doi.org/10.1109/IEDM.2017.8268336).
- [3] S. Natarajan *et al.*, "A 14 nm logic technology featuring 2nd-generation FinFET, air-gapped interconnects, self-aligned double patterning and a 0.0588 μm^2 SRAM cell size," in *IEDM Tech. Dig.*, Dec. 2014, pp. 3.7.1–3.7.3. doi: [10.1109/IEDM.2014.7046976](https://doi.org/10.1109/IEDM.2014.7046976).
- [4] A. Vardi and J. A. del Alamo, "Sub-10-nm fin-width self-aligned InGaAs FinFETs," *IEEE Electron Device Lett.*, vol. 37, no. 9, pp. 1104–1107, Sep. 2016. doi: [10.1109/LED.2016.2596764](https://doi.org/10.1109/LED.2016.2596764).
- [5] M. W. Iqbal *et al.*, "High-mobility and air-stable single-layer WS₂ field-effect transistors sandwiched between chemical vapor deposition-grown hexagonal BN films," *Sci. Rep.*, vol. 5, Jun. 2015, Art. no. 10699. doi: [10.1038/srep10699](https://doi.org/10.1038/srep10699).
- [6] M. Luisier *et al.*, "First-principles simulations of 2-D semiconductor devices: Mobility, I-V characteristics, and contact resistance," in *IEDM Tech. Dig.*, Dec. 2016, pp. 4–5. doi: [10.1109/IEDM.2016.7838353](https://doi.org/10.1109/IEDM.2016.7838353).
- [7] J. L. Everaert *et al.*, "Sub-10⁻⁹ $\Omega \cdot \text{cm}^2$ contact resistivity on p-SiGe achieved by Ga doping and nanosecond laser activation," in *Proc. Symp. VLSI Technol.*, Jun. 2017, pp. T214–T215. doi: [10.23919/VLSIT.2017.7998176](https://doi.org/10.23919/VLSIT.2017.7998176).
- [8] U. Singiseti *et al.*, "Ultralow resistance *in situ* Ohmic contacts to InGaAs/InP," *Appl. Phys. Lett.*, vol. 93, no. 18, Nov. 2008, Art. no. 183502. doi: [10.1063/1.3013572](https://doi.org/10.1063/1.3013572).
- [9] R. Kappera *et al.*, "Phase-engineered low-resistance contacts for ultrathin MoS₂ transistors," *Nature Mater.*, vol. 13, no. 12, pp. 1128–1134, Aug. 2014. doi: [10.1038/nmat4080](https://doi.org/10.1038/nmat4080).
- [10] J. Lacord, G. Ghibaudo, and F. Boeuf, "Comprehensive and accurate parasitic capacitance models for two- and three-dimensional CMOS device structures," *IEEE Trans. Electron Devices*, vol. 59, no. 5, pp. 1332–1344, May 2012. doi: [10.1109/TED.2012.2187454](https://doi.org/10.1109/TED.2012.2187454).
- [11] J. Lacord, S. Martinie, O. Rozeau, M. A. Jaud, S. Barraud, and J. C. Barbé, "Parasitic capacitance analytical model for sub-7-nm multi-gate devices," *IEEE Trans. Electron Devices*, vol. 63, no. 2, pp. 781–786, Feb. 2016. doi: [10.1109/TED.2015.2506781](https://doi.org/10.1109/TED.2015.2506781).
- [12] T. Agarwal *et al.*, "Benchmarking of MoS₂ FETs with multi-gate Si-FET options for 5 nm and beyond," *IEEE Trans. Electron Devices*, vol. 62, no. 12, pp. 4051–4056, Dec. 2015. doi: [10.1109/TED.2015.2491021](https://doi.org/10.1109/TED.2015.2491021).
- [13] A. Agrawal, N. Shukla, K. Ahmed, and S. Datta, "A unified model for insulator selection to form ultra-low resistivity metal-insulator-semiconductor contacts to n-Si, n-Ge, and n-InGaAs," *Appl. Phys. Lett.*, vol. 101, no. 4, Jul. 2012, Art. no. 042108. doi: [10.1063/1.4739784](https://doi.org/10.1063/1.4739784).
- [14] M. H. Liao and C. Lien, "The comprehensive study and the reduction of contact resistivity on the n-InGaAs M-I-S contact system with different inserted insulators," *AIP Adv.*, vol. 5, no. 5, May 2015, Art. no. 057117. doi: [10.1063/1.4921023](https://doi.org/10.1063/1.4921023).
- [15] D. Yakimets *et al.*, "Vertical GAAFETs for the ultimate CMOS scaling," *IEEE Trans. Electron Devices*, vol. 62, no. 5, pp. 1433–1439, May 2015. doi: [10.1109/TED.2015.2414924](https://doi.org/10.1109/TED.2015.2414924).