A 4 GS/s 39.9 dB SNDR 11.7 mW Hybrid Voltage-Time Two-Step ADC With Feed-Forward Ring Oscillator Based TDCs

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Abstract—A power and area efficient two-step hybrid voltage-time ADC achieves a 4 GS/s conversion speed and 39.9 dB SNDR in 28 nm CMOS. Two pipelined time-based converters (TBC) with a thermometer capacitive DAC (CDAC) in the ADC lead to a high-speed and low-power operation. The pipelined architecture splits the full ADC resolution and thus relaxing the TBC complexity. The TBC consists of a voltage-domain comparator, a current-source based voltage-to-time converter (VTC), and a ring oscillator (RO) based time-to-digital converter (TDC) with feed-forward and $2\times$ interpolation that achieves high conversion speed and good linearity simultaneously. The prototype ADC is fabricated in a standard 28 nm CMOS process with an active area of only 0.017 mm^2 . The measured SNDR and SFDR are 39.9 dB and 47.8 dB with a Nyquist input at 4 GS/s. The FoM_w and FoM_s are 39.3 fJ/conv-step and 152.2 dB, respectively.

Index Terms—Analog to digital converter (ADC), time-based ADC, time-to-digital converter (TDC), ring oscillator (RO), voltage-to-time converter (VTC), low power, high speed, single channel.

I. INTRODUCTION

IN both wireless and wireline communication systems, energy-efficient and compact ADCs in the receiver are required to achieve higher data rates [1]–[4]. ADCs with an ENOB of 6–8 b and a sampling rate of up to several GS/s are of high interest [5]–[7]. These ADCs provide benefits for the reduction of the complexity in the communication system as a wideband ADC replaces a significant part of the signal chain [8]. The conventional ADCs reported in this field usually employ pipelined SAR or time-interleaved (TI) pipelined SAR ADCs [6]–[9].

SAR ADCs are well known for their simple topology and technology scalability. However, due to the SAR logic, SAR ADCs are intrinsically slow. Pipelined SAR ADCs are then used to increase the sample rate as shown in Fig. 1a. Despite the benefits, CMOS technology scaling results in a lower supply voltage, which eventually degrades the signal-to-noise ratio (SNR) and thus the resolution of the ADC. On the contrary, due to the higher switching speeds, scaled technologies enable increasingly finer resolutions in the time domain [10], [11]. Therefore, in order to solve the design difficulties imposed by the digital driven technologies, time-domain conversion has drawn increasingly attention from the ADC community. For example, with the basic voltage-to-time converter (VTC) + time-to-digital converter (TDC) ADCs, it

Fig. 1. Block diagram of pipelined (a) SAR ADC and (b) time-based ADC.

could be proven that time-domain ADCs are capable of achieving a comparable or even better efficiency compared with traditional voltage-domain ADCs [12]–[14]. Another category of the time-based approach is the voltage-controlled oscillator (VCO), which converts the input voltage to a phase difference and then extracts this phase difference as the digital output. Because of the delta sigma property, VCO based ADCs are able to achieve high resolution in the time domain [15]–[18].

However, due to the fact that most real world signals are in the voltage domain, a VTC is usually needed to convert the voltage-domain information to the time domain. The linearity of the VTC is typically limiting the performance of such a time-domain ADC for a high dynamic range. Moreover, for the TDC, the complexity and power consumption become excessive when the resolution increases because the TDC is actually a flash ADC in the time domain [10].

A recent approach to realize a high efficiency is the multi-domain converter, which utilizes the advantages from the different domains [19]–[22]. Similar to this approach, a single-channel hybrid voltage-time two-step ADC (Fig. 1b) is presented in this paper. The proposed ADC splits the full time-domain conversion into two pipelined stages. Therefore, it reduces the complexity of the TDC significantly. The VTCs linearity requirements are also relaxed at the same time, making it possible to obtain a high speed while maintaining a low power consumption. This approach resulted in a 4 GS/s sample rate ADC with high power and area efficiency.

This paper is organized as follows. In Section II, the basic structure of the proposed voltage-time hybrid architecture and the advantages compared to the traditional voltage-domain conversion are discussed. The implementations of the circuits with an emphasis on the VTC and TDC are treated in Sec-

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Fig. 2. Simplified top-level architecture (single-ended for simplicity) of the proposed single-channel hybrid voltage-time two-step ADC and its timing diagram.

tion III. Experimental results are summarized in Section IV. Finally, Section V draws the conclusion of this paper.

II. HYBRID VOLTAGE-TIME ADC

A. ADC Architecture

Fig. 2 shows the schematic of the hybrid voltage-time two-step ADC and its timing diagram. Compared with [19], the two stages are fully decoupled since the input voltage ($V_{inp} - V_{inn}$) is sampled simultaneously by two stages separately through the bootstrapping switches. This is because the VTC used in this ADC is based on the current source discharging, the information stored on C_0 will be lost after the voltage-to-time conversion. The mismatch between the two sampled voltages will be transferred to the residue voltage at the end of the thermometer CDAC cycle Φ_c . Since the full accuracy of the ADC is determined by the CDAC and the residue voltage, the mismatch between the two sampled voltages can be corrected in the digital domain afterwards if sufficient redundancy between the two stages is foreseen.

Two TBCs are used as quantizers in both the first and the second stage. The resolution of the two TBCs are both 4 b. With 1 b redundancy, the overall ADC has an 7 b overall resolution. In order to increase the TBC efficiency, the complexity of the TDC in the TBC is reduced by 1 b with the assist of a voltage-domain comparator. This comparator operates in parallel with the VTC and produces a sign bit to represent the voltage-domain polarity. Therefore, signed coding is used in the output of the TDC. With the same LSB in the time domain, the dynamic range and the conversion speed of the TDC are halved as the polarity is preserved by the sign bit. Thanks to the fact that the voltage comparator in this ADC consumes less power than the 3 b TDC in this ADC, the hybrid voltage-time operation improves the overall power efficiency.

The outputs from TBC₁ is applied to the CDAC, which generates a voltage residue at the end of Φ_c . The CDAC in this paper is thermometer coded due to the flash nature of

the TDC. The unit capacitor C_u is 6 fF in the CDAC because the non-linear parasitics from the bootstrapping switch and residue amplifier (RA) degrades the linearity performance. The unit capacitor has to be large enough to ensure a more than 7 b CDAC linearity. C_0 is chosen to be 12 fF also for the linearity reason. In contrast to a SAR ADC which needs a successive register to control the ADC to perform comparison and produce bits one by one, TBC₁ generates the first 4 b in one clock period and its output is directly connected to the CDAC switches through simple buffers. Thus, the critical path is shorter in this paper allowing the ADC to operate at a much higher frequency.

The residue voltage is amplified by the dynamic RA to provide a larger dynamic range for the second stage. The clocks Φ_{rst} , Φ_{amp} are implemented by delay lines with tunable voltage to calibrate over PVT variations. The RA also decouples TBC₁ and the thermometer CDAC from TBC₂ to implement a truly pipelined operation. A 1 b redundancy is implemented between the coarse and fine stages to tolerate the over-range caused by the dynamic RA gain error and the mismatch from the first stage. TBC₂ resolves the last 4 b. A digital encoder combines and converts the thermometer code to a binary output.

The TDC complexity is defined by the number of the delay cells in it, for example, the complexity of a Nb TDC is 2^N . Then the power consumption and the conversion speed also can be expressed by the complexity 2^N . Compared with a 7 b time-domain converter whose complexity is 2^7 , the two-step ADC in this paper splits the full resolution into two 4 b sub-TBCs in each step, thus the complexity is reduced to 2×2^4 . Therefore, the two 4 b TDCs are four times better than the one with 7 b in a single stage in term of power and speed. Since the input is sampled on the CDAC, and the full ADC resolution is preserved by the CDAC, the first TBC does not need to be 7 b accurate. A 7 b TDC therefore would pose more stringent requirements on matching, which would

Fig. 3. Concept of (a) polar TDC and (b) unipolar TDC, T_{FS} is the full swing in the digital domain.

further increase power and area. The two-step architecture also reduces the VTC linearity requirements from 7 b to 4 b because of the CDAC. The relaxed requirements of the TDC and VTC come at the cost of the RA however. Since the two stages are pipelined by the RA and the time consumed by the RA is much less than the time consumed by the VTC and TDC, the pipelined architecture almost doubles the sample rate. The RA operates in the voltage domain because voltage-domain amplification is more accurate and the second stage VTC alone is not enough to provide sufficient voltage-to-time gain. By utilizing the advantages from both the voltage and time domain, the hybrid architecture is able to achieve high efficiency at 4 GS/s.

B. Unipolar TDC

Unlike in the voltage domain, polarity is one difficult design consideration in the time domain [10], [11], [19]. To make the TDC differential, the polar TDC uses two sub-TDCs (TDC_p and TDC_n in Fig. 3a), each having half of the full resolution T_{FS} [11]. The time difference R_p and R_n signals are sent to both TDCs with opposite polarity. Then the overall TDC output is derived from the difference between the two output codes ($D_p - D_n$). However, due to the use of two TDCs and a digital logic to subtract the two output codes, the polar TDC is not power and area efficient. With two TDCs in parallel, the polar TDC also increases the VTC load, which further degrades the power efficiency and the linearity of the VTC. Also, the VTC is directly connected to the TDCs which is not preferred as the TDC is a noisy digital circuit.

To effectively increase the power efficiency and reduce the load at the output of the VTC [11], [19], a unipolar TDC is proposed as shown in Fig. 3b. It converts positive as well as negative time difference into an absolute digital code. A comparator performs a voltage-domain comparison to determine the polarity of the input signal and produces a sign bit during the voltage-to-time conversion. An XOR gate at the VTC output encodes the time-domain information to a pulse EN , the duration of which is proportional to the absolute value of $|V_p - V_n|$. The polarity in the time difference signal is thus eliminated, and the TDC only needs to resolve the absolute time difference EN , or in other words, the complexity of

Fig. 4. Metastability in a SAR ADC and the first stage of this ADC, orange zones represent the range that the metastability happens.

the TDC is reduced from 4 b to 3 b. As a result, one TDC is removed at the expense of adding one voltage-domain comparator.

From simulations, one 3 b TDC consumes more power and occupies more area than a comparator, so the unipolar TDC is more power and area efficient. Also, in the unipolar TDC, the output of the VTC only connects to an XOR gate. This means that the VTC is decoupled from the noisy TDCs. A small load also leads to a better power and linearity performance for the VTC. As the XOR gate is not fully symmetrical, it will degrade the linearity of the time difference information, but the output from the XOR gate is still sufficient for the following TDC. In the traditional TDC [19], the full delay chain has totally different loads for the START and STOP signals, which degrades the linearity even more compared with the proposed unipolar TDC. One drawback of the unipolar TDC is that the offset will cause the TDC to map the input to the opposite polarity when the input is smaller than the offset. Therefore, it will contribute to a linearity loss.

Compared with the SAR ADC whose comparator metastability can happen in any of the comparison cycles from MSB to LSB, the comparator metastability in this ADC only happens when the input amplitude is small since only one comparison is needed for each stage in every cycle (Fig. 4). The voltage-domain comparison is in parallel with the time-domain conversion (VTC, XOR and TDC), so the comparison and the time-domain conversion are independent events. Cross-coupled inverters are implemented at the output of the comparator. These cross-coupled inverters skew their thresholds because the cross-coupling forms a feed-forward structure. Most of the metastable comparator outputs are forced to "0" (the initial state of the comparator), but only half of them being correct [23]. Moreover, the voltage-domain comparator has more time to regenerate as only one comparison is performed inside each period. Therefore, the possibility of the wrong forced metastable comparator states are sufficiently low to have an insignificant influence on the overall ADC accuracy.

III. CIRCUIT IMPLEMENTATION

A. Voltage-to-Time Converter

The linearity of the VTC directly impacts the performance of the hybrid voltage-time ADC. Although the two-step architecture relaxes the VTC linearity requirement, the large input range greatly limits the linearity of the VTC [11], [14], [20]. Fig. 5a shows the schematic and operating waveform

Fig. 5. Circuit diagram and waveform of (a) conventional VTC and (b) current-source VTC.

Fig. 6. Simulated linearity comparison of the conventional VTC and current-source VTC.

of the traditional dynamic VTC [11], [14]. First, the output nodes X_{op} and X_{on} are reset to V_{DD} during the reset phase. When Φ_{VTC} goes high, the output capacitors C are discharged by a differential current through the differential pair M_1 and M_2 . The discharging rates at X_{op} and X_{on} are determined by the transconductance gm and the input voltage V_p and V_n , respectively. Once X_{op} and X_{on} cross the threshold voltage of the inverters, two rising edges R_p , R_n are generated, the time (Δt) between which is a measure of the voltage difference between V_p and V_n . The output of the VTC can be expressed as:

$$\Delta t_{conv} = \frac{(V_{DD} - V_{TH}) \cdot C}{I_p} - \frac{(V_{DD} - V_{TH}) \cdot C}{I_n}, \quad (1)$$

$$= \frac{(V_{DD} - V_{TH}) \cdot C}{I_c + gm \cdot V_p} - \frac{(V_{DD} - V_{TH}) \cdot C}{I_c + gm \cdot V_n}$$

where I_c is the biasing current and gm is the transconductance of the differential pairs M_1 and M_2 . Due to channel length modulation, the biasing current I_c is a function of the drain-source voltage V_{DS} . At the same time, the transconductance gm is affected by the input differential voltage V_p , V_n . The

Fig. 7. Simulated PVT variations of the VTC linearity and gain with fixed $V_{bias,VTC}$.

Fig. 8. Simulated gain control of the current-source VTC by tuning $V_{bias,VTC}$.

output time difference can be written as:

$$\Delta t_{conv} = \frac{(V_{DD} - V_{TH}) \cdot C}{I_c(V_{DS,p}) + gm(V_p) \cdot V_p} - \frac{(V_{DD} - V_{TH}) \cdot C}{I_c(V_{DS,n}) + gm(V_n) \cdot V_n} \quad (2)$$

$V_{DS,p}$ and $V_{DS,n}$ are the drain-source voltage for M_1 and M_2 , respectively. Due to the signal-dependent I_c and gm , the conventional dynamic VTC suffers from a serious linearity problem especially in the first stage where the full input swing is applied to the VTC in Fig. 2. Mismatch will further degrade the linearity because of the different gms in the denominators.

To resolve the linearity issue in the conventional dynamic VTC, a current-source based VTC is used in this ADC as shown in Fig. 5b. The reset phase is removed in this VTC. First, during the sampling phase, the differential input voltage is sampled on the capacitor C at nodes V_p and V_n , this

capacitor is actually the total capacitor in the CDAC. When Φ_{VTC} goes high, C is discharged with a current that is controlled by the biasing voltage $V_{bias,VTC}$. Then a time difference is produced just like in the conventional VTC. To ensure sufficient linearity, the inverter threshold voltage is designed so that M_1 and M_2 never enter the triode region. In this VTC, the discharging rate is defined by the current source only. The output of the VTC can be express as:

$$\Delta t_{current} = \frac{(V_p - V_{TH}) \cdot C}{I_c(V_{DS,p})} - \frac{(V_n - V_{TH}) \cdot C}{I_c(V_{DS,n})} \quad (3)$$

here the current I_c is also affected by the channel length modulation, but the gm influence is removed from the equation compared with (2). Since the channel length modulation can be reduced by increasing the impedance of the current source, transistors M_1 , M_2 with a long length are used in this design. M_3 , M_4 are working in linear region, and serve as degeneration to further improve the linearity. The removal of the gm part in the denominator makes the linearity of the current-source VTC more robust to mismatch. In this hybrid ADC, the input amplitude is selected to be 0.5 V and the CM to be 0.75 V due to the VTC linearity limit. A 1 V amplitude simply means one of the outputs will not travel across the V_{TH} of the inverters in Fig. 6b.

The simulated linearity comparison is shown in Fig. 6. The current-source based VTC is able to achieve a good linearity performance for almost a two times larger input range. It is preferred in this hybrid voltage-time ADC as the first stage VTC directly converts the sampled full range input signal by the bootstrapping switch.

Fig. 7 shows that the linearity of the VTC is between 31 dB and 42 dB, and the gain varies by approximately $\pm 5\%$ due to temperature and supply variations. The linearity of the current-source based VTC remains sufficiently high as each of the stages in this ADC only needs to resolve 4 b. However, the VTC is very sensitive to process variations. The gain can vary up to 50%. Therefore, the biasing voltage $V_{bias,VTC}$ is used as a gain control to compensate for this. As from Fig. 8, the current-source VTC has a tunable gain range of $-25\% \sim 51\%$ while maintaining sufficient linearity. The first stage $V_{bias,VTC}$ is also used to compensate part of the RA gain variations.

B. Thermometer Capacitive DAC

In this ADC, the simplified capacitive DAC structure with capacitor values is illustrated in Fig. 9. The DAC consists of unit size capacitors and half sized capacitors. The first seven MSBs are thermometer coded and the last two LSBs are half the size of the thermometer capacitors. All of the capacitors sample the ADC input during the sampling phase on the top plate of the capacitors while the bottom plates are connected to V_{cm} . During the acquisition phase, the bottom plates of the first seven capacitors are connected to the reference voltage V_{refp} or V_{refn} based on the output from the ring oscillator based TDC. One of the half-sized capacitors is always connected to the V_{cm} . The bottom plate of the final half-sized capacitor is connected to the output from the voltage-domain comparator to compensate for the residue range waste in Fig. 10.

Fig. 9. CDAC topology with 1/2 LSB compensation.

Fig. 10. Residue voltage and the 1/2 LSB shift.

Fig. 10 shows the simplified 1/2 LSB compensation concept. Due to the unipolar TDC, the digital output of the time domain is signed, meaning that the MSB represents the sign (positive or negative) of the signal and the rest of the thermometer bits represent the magnitude of the signal. In the TDC itself, the output is not shifted by 1/2 LSB for linearity considerations since introducing a delay in the ring would break the uniformity. As a result, the residue voltage range generated by the CDAC for positive signals is $0 \rightarrow +\text{LSB}$, while the residue range for negative signals is $-\text{LSB} \rightarrow 0$. This creates a CDAC output of $-\text{LSB} \rightarrow \text{LSB}$. However, this 2 LSB range wastes 1 LSB as it contains duplicated information. Thanks to the compensation capacitor in Fig. 9, the residue range is shifted by 1/2 LSB based on the polarity. Thus, the new residue range is now centered around V_{cm} and the missing bit is recovered.

The unit switch plus cap technique [23] is used in the CDAC to minimize the parasitic contribution to the CDAC settling. The unit capacitor is 6 fF. Ideally, to minimize power consumption and area, one would minimize this value towards the kT/C noise and the matching requirement. In this 7 b ADC, a 100 aF unit capacitor seems to be sufficient for the required noise and matching specifications. However, due to the non-linear parasitics from the bootstrapping switch and the RA, the size of the C_u has to be large enough to make the total non-linear parasitics negligible comparing to the total CDAC capacitance. Constant parasitics only contribute to a gain error that does not influence the linearity. Thanks to the double sampling scheme, the parasitics from the upper sampling part for TBC_1 (at the top plate of C_0) are isolated

Fig. 11. (a) Circuit diagram and (b) simulated output waveform of the feed-forward cross-coupled ring oscillator based TDC.

from the performance.

C. Ring Oscillator Based TDC

The ring oscillator based TDC consists of a cross-coupled feed-forward ring oscillator (RO), reset switches and interpolators. The speed of the TDC is the most critical metric in this ADC. However, the speed of a traditional delay line based TDC is usually limited by the intrinsic inverter delay of the technology [10]. In order to break this speed limitation, a cross-coupled feed-forward RO is used in this ADC.

The implementation of the RO is shown in Fig. 11a. Cross-coupled inverters are inserted in between two five-stage ROs to create pseudo-differential outputs for the CDAC. The feed-forward is implemented by connecting the inverters two stages ahead to the opposite side. For example, n_1 is connected to p_3 and p_1 is connected to n_3 . This feed-forward technique increases the oscillation frequency by approximately 50% resulting in an LSB of 7 ps [18]. The unit inverter cell in the RO is clocked by the enable signal EN , so the full TDC is power-gated by the signal EN from the VTC in Fig. 3b. The EN freezes the TDC to provide the outputs. The output nodes in the TDC are reset to a known initial phase before every conversion by the reset switches who reset the p-nodes to VDD and the n-nodes to ground. Compared to a free-running RO [11], [18], the RO in this ADC always starts from a reset phase, which eliminates the need for a cyclic output code decoder to subtract two phases [11]. Since the TDC is in a shut-down phase after each conversion, it is very power efficient. Moreover, unlike the traditional SAR ADC which consumes the same number of cycles for every input, the power consumption of this TDC is dynamic. Therefore, the smaller the input amplitude the lower the power consumption.

To further increase the speed, a $2\times$ time interpolating technique is employed in this ADC. The $2\times$ interpolator uses two inverters with their outputs shorted to produce an intermediate

Fig. 12. (a) Circuit diagram and (b) simulated input and output waveform of the $2\times$ interpolator in the TDC.

Fig. 13. An example of the metastable output $T_P[4]$ of the TDC, Φ_{amp} is used to stop the propagation of the metastability, in this case all metastability fall into the metastability zone.

phase ($2i+1$ in Fig. 12) [24]. The conversion time of the TDC is still the same, but the resolution is doubled. In other words, the conversion speed is doubled for the same resolution. T_p and T_n are the differential TDC outputs. The simulated LSB for the RO based TDC is only 3.5 ps ($T[2i+1] - T[2i]$) in 28 nm CMOS technology. Because the RO consists of five stages with $2\times$ interpolators, it is able to achieve a maximum linearity of 3.32 b.

Metastability can also happen in the TDC when the input is close to the transition point. Fig. 13 shows an example of the TDC₁ output $T_P[4]$ in a metastable state. Since the output from TDC₁ is connected to the CDAC and the CDAC produces the residue voltage for the RA, the output from TDC₁ should be frozen before the amplification starts. Therefore, the buffer in the CDAC is combined with Φ_{amp} to stop the propagation of the metastable outputs. By doing this, only metastability within the metastability zone in Fig. 13 will influence the overall ADC performance, resulting in a half-way stuck CDAC output. The error produced by the metastable output is therefore always smaller than 1 LSB of the full ADC thanks to the thermometer code in the TDC. This error is then transferred to the second stage due to the redundancy. Therefore, only the metastability from TDC₂ will influence the overall ADC performance. TDC₂ has more time to regenerate compared with TDC₁. The cross-coupled inverters in the RO and buffers

Fig. 14. Simulated PVT variations of the TDC linearity and gain.

also reduce the metastability as the feed-forward helps to skew around the threshold. As all the metastability is moved to the narrow metastability zone, the overall ADC metastability possibility is only $6 \cdot 10^{-6}$ in simulation. Again, even if a wrong decision is made during the regeneration period, the error will only be smaller than 1 LSB. Therefore, it does not impose a significant resolution drop for the overall ADC.

The linearity of the TDC is limited by the matching between the unit inverter cells in the RO. The cross-coupled differential architecture improves the delay uniformity and thus the linearity. The $2\times$ interpolator is the major contributor to the mismatch for power consumption reasons. The matching can be easily improved by sizing up the transistors but the power would increase drastically. Higher order (e.g $4\times$) interpolation is not applied in the design to increase the speed as it poses even more stringent requirements on matching.

The linearity and unit step size of the TDC versus PVT variations is shown in Fig. 14. The linearity of the TDC is higher than 17 dB which is sufficient for both stages. However, the TDC unit step size changes by $\pm 15\%$ due to PVT variations, which means the overall TDC dynamic range (DR) also changes by $\pm 15\%$. As mentioned above and will be discussed in the next section, the VTC and RA have tunable gains to adjust their output to match the TDC DR.

Fig. 15. Schematic of the dynamic residue amplifier and the second stage comparator.

Fig. 16. Transient simulation of the performance of the dynamic residue amplifier and comparator.

D. Dynamic RA and the Second Stage Comparator

As shown in Fig. 2, the RA amplifies the residue voltage generated by the thermometer CDAC for the second stage. The total voltage-to-time gain is defined by the amplifier and the second VTC together. A dynamic integrator RA (Fig. 15) is designed with around $2\times$ gain to minimize the overall power consumption [25]. The amplification is terminated by a common-mode detector (CMD). It is realized by two capacitors and a NOR gate. The two capacitors connect the differential output nodes and produce a common-mode voltage at the midpoint. This common-mode voltage is combined with the clock Φ_{amp} to freeze the amplification as shown in Fig. 16. The output common mode voltage is a bit lower than 0.5 V, because the second stage VTC uses a PMOS current source. The lower common-mode output gives the PMOS a large V_{DS} , resulting in a better linearity as discussed in III-A.

Fig. 17 shows the simulated linearity and gain of the RA versus PVT variations. It shows that the linearity of the RA is higher than 42 dB across all variations, which means the linearity is sufficient for the second stage conversion. The gain of the RA is very sensitive to the variations, it changes by approximately $\pm 15\%$ due to PVT variations. Therefore, $V_{bias,Amp}$ is introduced to tune the gain. As shown in Fig. 18, when $\Delta V_{bias,Amp}$ changes by ± 100 mV, the gain can be changed by $\pm 20\%$ to cover the gain error caused by the

Fig. 17. Simulated PVT variations of the RA linearity and gain with fixed $V_{\text{bias,Amp}}$.

Fig. 18. Simulated gain control of the RA by tuning $V_{\text{bias,Amp}}$.

PVT variations. In this RA, the output CM will change with the $V_{\text{bias,Amp}}$. Since the output from the RA is the input for the second stage VTC and the voltage-to-time conversion in Section III-A does not rely on the input CM, the changed output CM from the RA will not influence the operation of the full ADC.

The dynamic RA is reused as the differential pair for the comparator which provides the sign bit for TBC_2 . In Fig. 16, the RA outputs V_{op} , V_{on} are similar to the differential pair in a typical Strong Arm comparator [26] but with a pre-terminated output. Therefore, only one additional latch is connected to the differential pair outputs to implement this comparator. Because the RA terminates the discharging for amplification and the input at VTC_2 contributes large capacitance load, the

Fig. 19. Simplified block diagram of the input test setup.

Fig. 20. Simulated common-mode variation due to the input network mismatch at 2 GHz with 8° (20 ps) phase shift and 3% magnitude imbalance.

Fig. 21. Simulated amplifier transfer function with and without phase compensation.

regeneration time of this RA comparator is worse than the Strong Arm comparator. This is not a limitation in this ADC as the comparison is not inside the critical path.

The dynamic amplification has one major drawback, namely the lack of common-mode rejection. The input network in the measurement setup is shown in Fig. 19. First, a single-ended input signal is generated by a signal generator. After the band-pass filter (BPF), the single-ended signal is converted to a differential signal through the Balun. DC-biasing is then added to the signals before they are fed to the chip.

Unfortunately, mismatches between the two differential signals are generated from the Balun, followed by the Bias-Ts and the input cables. Fig. 20 shows a 2 GHz differential signal with 8° (20 ps) phase shift and 3% magnitude imbalance and its corresponding common-mode voltage. As can be seen, the common-mode voltage is actually signal dependent. Due to its open-loop nature, the gain of the dynamic amplifier will change together with the common-mode voltage. Therefore, a phase shifter is inserted in Fig. 19 to compensate the common-mode variation. The transfer curves of the dynamic amplifier

Fig. 22. Die micrograph of the ADC with a zoomed-in view of the core area occupying an active area of 0.017 mm².

Fig. 23. Power consumption breakdown, CLK GEN and output buffers are not included.

Fig. 24. Measured DNL/INL at 4 GS/s.

with and without the phase shifter are plotted in Fig. 21. Finally, the dynamic amplifier is able to achieve a linearity that is higher than 5 b with the phase compensation in simulation.

IV. MEASUREMENT RESULTS

The prototype chip is fabricated in a standard 1P10M 28 nm CMOS with an active area of 0.017 mm² (125 μm × 135 μm) as shown in Fig. 22. The measured total power consumption is 11.7 mW at 4 GS/s. There are four voltage domains in the ADC: CLK, analog, digital and I/O. The power consumption breakdown is shown in Fig. 23, CLK and I/O power are not included.

Fig. 25. Measured calibrated output spectra with 0 dBFS signal applied at 156.25 MHz and 1.843 GHz, respectively. Sampling frequency is 4 GS/s.

Fig. 24 shows the DNL and INL characteristics at 4 GS/s with a 156.25 KHz sinusoidal input. The mismatch introduced by the layout connections near the ends of the RO (p_4 , n_2 in Fig. 11a) is visible in the INL around codes 10 and 118. The DNL and INL are within 0.51 LSB and -0.63 LSB, respectively. As the second stage TBC is capable of resolving 4.32 b, the overall ADC is able to achieve a maximum resolution of 7.32 b. The output spectra of 4 GS/s at 156.25 MHz and 1.843 GHz input frequencies are depicted in Fig. 25. The SNDR and SFDR at Nyquist are 39.91 dB and 47.83 dB, where the distortion is dominated by HD_3 and HD_5 .

Since the performance of the open loop RA, VTC and the time-based circuit are sensitive to process variations, digital calibration is applied in post processing. As the CDAC preserves the overall ADC linearity and the matching of MOM capacitors in CMOS processes is very good, only the inter-stage gain and TDC₂ mismatch were treated. In the reconstruction of the ADC output, the second stage output can be written as:

$$D3 \cdot 2^0 + D2 \cdot 2^{-1} + D1 \cdot 2^{-2} + D0 \cdot 2^{-3} \quad (4)$$

However, the weights for digital output bits are not ideal in reality. Scaling factors W are added in (4) to improve the linearity:

$$[D3 \cdot 2^0, D2 \cdot 2^{-1}, D1 \cdot 2^{-2}, D0 \cdot 2^{-3}] \times [W_3, W_2, W_1, W_0]^T \quad (5)$$

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART ADCs

	VLSI' 12 [28]	VLSI' 13 [29]	ISSCC' 15 [6]	VLSI' 17 [13]	ISSCC' 14 [30]	ISSCC' 19 [18]	VLSI' 18 [19]	This Work
Architecture	Flash	Flash	TI SAR	Time	Time	TI VCO	Hybrid	Hybrid
Technology	40nm	32nm	65nm	40nm	65nm	28nm	65nm	28nm
Supply [V]	1.1	1.1	1.0	1.2	1.1	1/0.85	1	1
Resolution [b]	6	6	6	8	7	8	8	7
fs [GS/s]	3	5	5	2	2.2	5	1.0	4
SNDR [dB]	33.1	30.9	30.25	40.7	37.4	45.2	44.4	39.9
Power [mW]	11.0	8.5	5.5	21	27.4	22.7	2.3	11.7
$FoM_W = P / (2 \cdot BW \cdot 2^{ENOB})$ [fJ/conv-step]	99.3	59.4	39	119	210	30.5	18.7	39.3
$FoM_S = SNDR + 10 \log(F_s / 2 / P)$ [dB]	144.4	145.6	146.8	150.6	143.3	155.6	157.3	152.2
DNL/ INL [LSB]	NA/ 0.28	0.52/ 0.37	0.95/ 1.4	0.14/ 0.61	0.60/ 1.00	NA	0.60/ 0.80	0.51/ 0.63
Area [mm ²]	0.021	0.03	0.008	0.08	0.052	0.023	0.007	0.017

Fig. 26. Measured dynamic performance versus input frequency at 4 GS/s.

Fig. 27. Measured SNDR/SNR versus input power.

In order to get the scaling factor W , a slow ramp signal is first applied to the ADC with an amplitude equals to $\frac{FS}{8}$. By doing this, only the second stage output bits are triggered and the first stage is isolated from this operation. $V_{bias,VTC}$ and $V_{bias,Amp}$ are set to match the input range for the TBC at this moment. Then the output is sampled and the transfer function is extracted. From the transfer function, the calibration coefficients W can be easily calculated. The temperature is assumed to be constant during the measurement. With sinusoidal inputs, the corresponding output is multiplied with the extracted coefficients in post processing.

Fig. 26 summarizes the dynamic performance versus the input frequency at 4 GS/s. The SNDR and SFDR remain better than 42.1 dB and 53.5 dB respectively for input frequencies

Fig. 28. FoM_W comparison with state-of-the-art single-channel ADCs (f_{snyq} : 1 GHz–10 GHz) presented at ISSCC and VLSI 2010–2019. Two TI ADCs with similar performance are also included.

below 1 GHz, leading to an FoM_W of 28.1 fJ/conv-step. The SNR and SFDR start to degrade above 1 GHz. The SNDR and SFDR reduces to 39.9 dB and 47.83 dB at Nyquist, leading to an FoM_W of 39.3 fJ/conv-step. The SFDR is mainly limited by the quality of the differential input signal and the dynamic amplifier. Due to the amplitude and phase imbalance of the differential signal, a severe input common-mode variation was present at high frequencies, which eventually limited the RA linearity. Fig. 27 shows the SNDR/SNR versus different input amplitude.

In Table I, the ADC performance is summarized and compared with state-of-the-art ADCs reported at the ISSCC and VLSI symposium with similar performance [32]. The presented ADC achieves the highest conversion rate among all the other time-domain ADCs. The ADC reported in [19] achieves the best FoM, however, its sampling frequency is $4\times$ lower than in this paper. Owing to the hybrid architecture, the presented ADC achieves excellent FoM_W among all the single-channel ADCs with a similar sampling rate (1 GS/s–10 GS/s) as can be seen in Fig. 28. Even compared with the time-interleaved ADCs [18], [33], this ADC shows competitive performance while having a lower complexity and a smaller area.

V. CONCLUSION

This paper introduces a simple and efficient single-channel hybrid voltage-time two-step ADC to achieve high speed in low-voltage nanoscale CMOS. The new hybrid ADC solves the dilemma in the voltage domain as the supply voltage continuously decreases with technology scaling. It combines the high accuracy of the voltage-domain CDAC and the high speed and high efficiency of the time-domain converter to satisfy the need for high speed and low power ADCs. A speed-optimized VTC and RO based TDC were introduced resulting in a power efficient operation.

Fabricated in a standard 28 nm CMOS process, the prototype ADC consumes 11.7 mW at 4 GS/s for a 1 V supply and achieves a SNDR of 39.9 dB with a Nyquist input, resulting in FoM_w and FoM_s of 39.3 fJ/conv-step and 152.2 dB, respectively. The ADC's efficiency is among the best for reported single-channel ADCs, enabling a potential of TI ultra wideband ADC in the future.

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