Design of Single-Topology Continuously-Scalable-Conversion-Ratio Switched-Capacitor DC-DC Converters

Nicolas Butzen, *Student Member, IEEE*, and Michiel Steyaert, *Fellow, IEEE*

Abstract—This paper introduces a fundamentally different type of switched-capacitor DC-DC converter with large voltage swing flying capacitors, that is made efficient using advanced multiphasing soft-charging. A single-capacitor topology is derived that behaves like a gyrator and achieves a continuously-scalable-conversion-ratio with high efficiency. A circuit fabricated in a 28nm CMOS process demonstrates the working principle of the presented topology and advances the state-of-the-art by achieving a peak-efficiency of 93%, and a single-topology 0.9-to-2.03V output voltage range with more than 90% efficiency.

I. INTRODUCTION

Since their first usage in monolithic systems, switched-capacitor (SC) DC-DC converters basic principles have remained largely unchanged [1]. Because capacitors inherently incur charge-sharing losses when switched between different voltages by means of a battery or other capacitors, the only viable strategy to make efficient switched-capacitor converters has been to limit the voltage swing across the capacitor terminals as much as possible. This can be explained as follows. The charge-sharing loss of a charge transfer, E_{cs} , is proportionate to the capacitor's voltage swing squared, ΔV^2 . At the same time, the transferred charge, q , is proportionate to ΔV . Combining both, the efficiency of a charge transfer can be established:

$$\frac{q}{E_{cs}} \propto \frac{1}{\Delta V}. \quad (1)$$

In other words, if a charge-transfer is to be efficient, the voltage swing needs to be minimized. Consequently, SC topologies with approximately fixed capacitor voltages are used, which are only able to supply a specific rational voltage conversion ratio (VCR) efficiently, as shown in Fig. 1. When a smaller VCR than the topologies ideal VCR (iVCR) is required, or when a larger output power is needed, the converter must increase the capacitors voltage swing and thereby lower its efficiency. As such, there is a very strong connection between a

Fig. 1. High level concept of a conventional two-phase switched-capacitor converter.

Fig. 2. Output charge per cycle and efficiency of a gearbox switched-capacitor converter.

conventional SC converter's VCR, efficiency, and output power. Naturally, this is a problem for applications that require a large output voltage range, like voltage-scaling processors [2].

In the literature, the usual solution is to combine multiple topologies together in a gearbox converter [3]–[8], which results in the typical saw-tooth curve portrayed in Fig. 2. Such converters do, however, have multiple disadvantages. For one, to maintain a high efficiency over a wide voltage range, many topologies are usually required, each adding extra transistors which often end up as extra series resistances in other topologies. Moreover, the required control overhead to switch between different topologies at the right moment increases

The authors are with the Department of Electrical Engineering, KU Leuven, B-3001 Heverlee, Belgium, e-mail: nicolas.butzen@esat.kuleuven.be .

Fig. 3. High level concept of the proposed switched-capacitor converter.

rapidly with the number of topologies, and thus induces significant losses. An example hereof is the design in [7] where the efficiency reportedly drops from 94% to 87% by activating the control loop. In addition, as switched-capacitor converters implement more ratios, they suffer significantly in terms of power-density [9].

In [10]–[13] it was demonstrated that charge transfers between capacitors can be soft-charged using the advanced multiphasing concept, by spreading the transfer of charge out over multiple phases. Consider a capacitor that was soft-charged using S phases, its charge-transfer efficiency can easily be deduced:

$$\frac{q}{E_{cs}} \propto \frac{S}{\Delta V}. \quad (2)$$

Thus, minimizing the capacitors' voltage swing is no longer required to obtain an efficient converter. Instead, the efficiency of the converter can be guaranteed using the soft-charging parameter. Advanced multiphasing consequently offers the exciting opportunity to make switched-capacitor converters with large capacitor voltage swings.

This paper has the following outline: Section II proposes a new type of switched-capacitor topology that maintains high efficiency despite large capacitor voltage swings. A closer look will be taken to how it can be modeled and optimized in Section III. Section IV discusses an example implementation of such a topology, while Section V verifies its working principle with measurement results. Finally, Section VI highlights the important conclusions of this work.

II. WORKING PRINCIPLE

Figure 3 illustrates the high level concept of the proposed topology. As can be seen, the basic idea is to maximize the voltage variation of the flying capacitor(s) by making it swing between approximately V_{in} and 0V

and back, regardless of the output voltage. Opening up the capacitors' voltages to have no fixed bias voltage, dramatically increases the number of topologies one can make, especially when also using a lot of phases. Therefore, to minimize the design complexity, only single-capacitor topologies are considered in this work. In order to simplify a practical implementation, it is assumed that the capacitor polarity stays the same over a full cycle. Furthermore, the main goal here is to make a step-down converter.

A. Useful soft-charging

To boost the efficiency, soft-charging must be applied carefully such that each charge transfer is useful to the full conversion effort. For example, in [13] each soft-charging step transfers charge from the ground terminal to the output, resulting in an increase of the output charge per cycle. As such, a necessary condition for a charge transfer to be considered useful, at least when there is only a single capacitor topologically speaking, is that it results in charge being added/subtracted to the converter terminals. Also, these charge exchanges with the terminals should be in line with the desired voltage conversion ratio: for step-down converters charge should be subtracted from the V_{ss} terminal. Translating said condition to the phases of the converter, this implies that the capacitor should always have one terminal connected to one of the converter terminals. Moreover, during a set of soft-charge transfers, the capacitor should stay connected to the same terminal, thereby gradually (dis)charging the converter terminal.

B. Topology structure

While soft-charging is an essential element of the topology, its structure is actually defined by the phases that would be there even without soft-charging. In some sense, the topology is build on these phases, and as such they are referred to as *cornerstone phases*. During a cornerstone phase, each capacitor terminal must be connected to a converter terminal. In addition, to satisfy the condition that the capacitor has to stay connected to the same terminal during a set of soft-charge transfers, two consecutive cornerstone phases should always share a capacitor terminal connection.

From the basic concept description above, it was established that the voltage swing of the converter should be as large as possible. For a step-down converter, the largest achievable voltage swing where the polarity of the capacitor does not change equals V_{in} . As such, two cornerstone phases are deduced: One where the capacitor is connected to V_{in} and V_{ss} , and one where the capacitor voltage is zero. In the latter cornerstone phase, the capacitor could technically be connected to

Fig. 4. Effect of having cornerstone phase with zero capacitor voltage at the input terminal.

Fig. 5. Cornerstone phases of presented topology.

any of the three converter terminals. However, if it were to connect to the input- or ground terminal in this phase, this will inevitably lead to charge being pumped to said terminals, which is of course to be avoided for step-down conversion. This is illustrated for V_{in} in Fig. 4.

Because the two cornerstone phases so far do not share a capacitor terminal connection, at least two more cornerstone phases need to be added in between. Only two valid phases remain that match the earlier made assumption of capacitor polarity and there is only way of combining these with the previous cornerstones such that charge is transferred to and from the right terminals. The resulting set is shown in Fig. 5.

It can be appreciated that the top plate of the capacitor alternates between the input- and output terminals, while the bottom plate alternates between V_{out} and V_{ss} . Because each capacitor terminal goes through a separate charge- and discharge cycle, soft-charging is thus simply enabled by adding intermediate nodes for the top- and bottom plate separately. These intermediate nodes spread evenly between the boundary conditions of V_{in}/V_{out} and V_{out}/V_{ss} for the respective capacitor plate [10].

Figure 6a shows the topology with M soft-charging phases at the top-side (nodes T_1 to T_M) and N soft-charging phases at the bottom-side, with corresponding nodes B_1 to B_N . All charge-transfers here are useful for step-down conversion, except for those of the two initial cornerstone phases. These phases can thus better be omitted, leading to the improved topology of Fig. 6b.

Fig. 6. Voltage versus phase diagram of (a) the basic topology and (b) the improved topology for step-down conversion.

Fig. 7. Phase diagram of improved topology with two top- and bottom-side soft-charging phases. (a) is without- (b) is with outphasing. D1 and D2 are the cornerstone phases, and B/B1/B2 and T/T1/T2 are the bot- and top-side intermediate nodes respectively. A selection of connections between core 1 and cores 3/4 is highlighted.

Fig. 8. Input-, (a), and output-, (b), charge per cycle of presented topology for different number of top- and bottom-side soft-charging phases, compared with a regular 2:1 and 3:1 SC converter.

C. Outphasing

The improved topology has the additional benefit of being compatible with Outphasing [13]. This is illustrated in Fig. 7. As can be seen, all of the connections that take place through the intermediate nodes B1/B2/T1/T2 between the different converter cores, can be replicated with half as many intermediate nodes if the soft-charging phase durations are doubled in length relative to the cornerstone phase durations. Moreover, the number of switches that connect the capacitor to those nodes, is also halved.

III. MODELING

A. Intrinsic behavior

For the following analysis it is assumed that the converter is in steady-state and that all charge transfers are completed fully. In addition, V_{ss} is presumed to be zero, while the output has infinite decoupling. With these assumptions in mind, a set of equations is derived by applying a charge-analysis to Fig. 6b:

$$\frac{q_{out}}{C_{tot}} = \frac{M+2}{M+1}V_{in} - \frac{M+N+4}{(M+1)(N+1)}V_{out}, \quad (3)$$

$$\frac{q_{in}}{C_{tot}} = \frac{1}{M+1}V_{in} + \frac{MN+M-2}{(M+1)(N+1)}V_{out}, \quad (4)$$

with q_{out} and q_{in} the output- and input charge per cycle respectively, and C_{tot} the total capacitance. Figure 8 plots these formula's for increasing values of M and N , and also compares them to those of a regular 2:1 and 3:1 SC converter. The presented topology has a very

Fig. 9. Gyrator model of presented topology.

different behavior compared with the regular converters [14]. Indeed, q_{in} and q_{out} are not proportionate to each other, and there is no sign of an ideal VCR. Instead, as M and N increase, the output charge converges to being constant regardless of the VCR and including step-up conversion. The input charge, on the other hand, is proportionate to the VCR, which leads to a high efficiency.

For M and N infinitely high, the behavior described above matches that of a gyrator. A gyrator is a lossless two-port element where the current through a port only depends on the voltage of the other port, and is characterized by its (trans)conductance, Y .

$$\begin{bmatrix} I_{in} \\ I_{out} \end{bmatrix} = \begin{bmatrix} 0 & Y \\ Y & 0 \end{bmatrix} \begin{bmatrix} V_{in} \\ V_{out} \end{bmatrix} \quad (5)$$

Figure 9 shows the equivalent gyrator model of the presented topology, with additional resistance parameters, R_A , R_B and R_C . Using (3) and (4), these parameters can be deduced:

$$Y = f_{sw}C_{tot} \frac{MN+N+M}{(M+1)(N+1)} \quad (6)$$

$$R_A = \frac{-1}{f_{sw}C_{tot}}(M+1)(N+1) \quad (7)$$

$$R_B = \frac{1}{f_{sw}C_{tot}} \frac{(M+1)(N+1)}{M+2} \quad (8)$$

$$R_C = \frac{1}{f_{sw}C_{tot}} \frac{(M+1)(N+1)}{N+2}, \quad (9)$$

with f_{sw} the switch frequency. From (6) it can be appreciated that, despite the fact that the converter behaves like a current source for constant V_{in} , the output current is also proportionate to the switching frequency. Frequency control schemas like the lower-bound hysteretic control commonly used in SC DC-DC conversion, are thus compatible with this topology.

Figure 10 plots the efficiency of the presented topology for different values of M and N . As can be seen, the topology obtains a wide efficient voltage conversion ratio range, which is substantially larger than that of a single regular SC converter. In addition, the larger the number of top- and bottom-side soft-charging phases, the higher the obtained efficiency. Naturally, M and N do not have to be the same value. For VCRs smaller than 2:1, the losses at the top-side are more significant relatively speaking, which makes M more important. Similarly, N

Fig. 10. Efficiency of presented topology for different number of top- and bottom-side soft-charging phases, compared with a regular 2:1 and 3:1 SC converter.

Fig. 11. Efficiency of presented topology with $M,N=16$, and scaling total switch conductance, G_{tot} .

gains in importance for VCRs larger than 2:1, including step-up conversion.

B. Finite switch resistance

In a practical implementation, the finite switch resistance prohibits the full completion of charge transfers. With regular SC converters, the effect of the finite switch resistance can be approximated by looking at the converter in the worst-case asymptotic limit where the capacitors behave like perfect DC voltage sources [15]. In the presented converter, however, this limit has little meaning because it is precisely the highly variable capacitor voltage which is key to its operation. Due to a lack of a closed-form approximation, this forces one to work with numerical methods or simulations. Figure 11 shows the result of such numerical calculations for an example converter and with varying total switch conductance. In the reference case, the normalized losses are approximately 5.6% for a VCR of 2:1, with the charge transfers almost fully completing (99.93%). Reducing the switch conductance by a factor of 4 and 16, corresponding to respective charge transfer completions of 81% and 30%, these losses increase to 8.1% and 35.5% respectively. In other words, the efficiency takes a significant hit if the switches are not sized for near-full charge transfer completion.

C. Extrinsic losses

The continuous charging of the parasitic coupling was shown to be a limiting factor to the achievable efficiency of regular fully integrated SC converters [16]. From Fig. 7b, though, it can be appreciated that in the introduced topology, both top- and bottom-plate nodes are inherently soft-charged, which means that any parasitic coupling on these nodes is soft-charged as well. Consequently, these losses are not as important for this converter type. The transistor driving and leakage losses, on the other hand, are important loss contributors that provide a trade-off for the total transistor area. Like with regular SC converters, these losses are considered extrinsic to the topology itself and are thus presumed not to interfere with its operation [16].

D. Optimization

The performance of the presented topology is decided by four major design parameters: the switch frequency, the total switch conductance per unit (converter) area, G'_{tot} , and the number of intermediate phases at the top- and bottom-side. Because the output charge per cycle of the topology is nearly constant for larger M/N , the desired power-density, P_D , basically sets the required switch frequency in stone:

$$f_{sw} \propto P_D, \quad (10)$$

which leaves G'_{tot} and M/N to optimize the converter.

To explore the optimal scaling of these parameters and the converter performance versus P_D , a closer look is taken at how the different loss contributors scale themselves. From the gyrator model, the intrinsic energy loss per cycle can be written as

$$E_{int} = \frac{C_{tot}}{M+1} \left(V_{in}^2 - 2V_{out} \frac{M+2}{M+1} (V_{in} - V_{out}) \right), \quad (11)$$

assuming that $M=N$. Thus, E_{int} is approximately inversely proportionate to M for large enough M . This formula does not include the effect of incomplete settling due to the switch resistance. That being said, due to the significant efficiency degradation that was witnessed in Section III-B once the charge transfer completion percentage drops, it is presumed that the optimal switch sizing is large enough such that its effect on the intrinsic energy loss can be ignored. Furthermore, it is also assumed that the optimal charge transfer completion percentage stays approximately constant, which means that $RCf_{sw}p$, with p the number of phases and RC the charge transfer time constant, is constant as well. This leads to the following (approximated) relation:

$$\frac{M^2}{G'_{tot}} \propto \frac{1}{f_{sw}}. \quad (12)$$

Combining (10), (11) and (12) then yields

$$E_{int} \propto \sqrt{\frac{P_D}{G'_{tot}}} \quad (13)$$

Because of (10), E_{int} has the same scaling as the intrinsic losses of the converter normalized by the output power, P_{int} . For the other loss contributors, the scaling is more easily identified. The transistor driving losses, P_{trans} , are proportionate to G'_{tot} , while the leakage energy loss, P_{leak} , is proportionate to G'_{tot}/f_{sw} and in turn to G'_{tot}/P_D . At low power densities, the leakage losses consequently dominate the driving losses, and vice versa at high power densities. Two distinct regimes of operation consequently emerge. For low P_D , optimization of the normalized total losses, P_N , yields

$$\begin{cases} G'_{tot} & \propto P_D \\ P_N, M & \propto 1 \end{cases} \quad (14)$$

In other words, an efficiency ceiling is reached where the intrinsic- and leakage losses balance each other out, and the number of soft-charging phases stays constant. At high power-densities, on the other hand, this behavior changes.

$$\begin{cases} P_N, G'_{tot} & \propto P_D^{1/3} \\ M & \propto P_D^{-1/3} \end{cases} \quad (15)$$

Note that this loss scaling is identical to that of regular switched-capacitor converters at high power densities [12], [16]. Figure 12a shows the scaling of the optimized design parameters and energy loss, but using a full numerical optimization of the converter. As can be seen, both the high- and low power-density regimes are clearly demonstrated, and the simplified model used above remains valid for most of the power-density range. Ultimately, though, a point is reached where M gets close to 1 which causes some of the approximations that were used to break down. Here, a third regime can be witnessed where the optimal value for M is four.

The relative loss contribution of the same optimization is illustrated in Fig. 12b. The optimal relative contribution of P_{int} is approximately 65% regardless of the power-density, until the very high power-density regime is reached. The other 35% are attributed to a combination of leakage- and transistor driving losses, with the latter dominating at higher power densities, as predicted.

IV. IMPLEMENTATION

The presented topology is implemented with $N, M=32$, as illustrated in Fig. 13. To enable direct charge transfers between capacitors through the soft-charging nodes, the converter is split into $1+N+M=65$ phase-shifted cores. Thanks to outphasing, only 16 top- and bottom nodes have to be implemented. All switches are implemented

Fig. 12. Scaling of (a) the frequency, switch conductance per unit area, normalized power loss and number of soft-charging phases, and (b) the relative loss contribution of an optimized continuously-scalable-conversion-ratio SC converter for a VCR of 2:1.

Fig. 13. System overview of implementation of proposed topology.

using two stacked thin-oxide transistors to enable a wide V_{out} range with a V_{in} of 2V. Furthermore, to maximize their conductance over the entire range, four 3pF bootstrap capacitors are used per core, each of which generates a voltage rail relative to the top-/bottom-plate, TP_p/TP_m and BP_p/BP_m , that is charged each time this plate connects to V_{out} using the external V_{outp} and V_{outm} rails. These external voltage rails are at a fixed voltage of 1V and -0.85V relative to V_{out} . All transistors that connect to a soft-charging node need to block both

Fig. 14. Micrograph of the monolithic SC converter using a continuously-scalable-conversion-ratio topology.

positive and negative voltages across their drain-source and are therefore driven by tristate buffers [17].

An external frequency reference, F_{CLK} , is divided using a non-overlapping clock generator into 130 phases, which are then distributed to each cores local decoder. The V_{ss} -connecting transistors together with the logic are powered by $V_{control}=1.1V$. $V_{control}$, V_{outp} and V_{outm} are provided externally for flexibility and measurement purposes, but their peak current consumptions of $70\mu A$, $8\mu A$ and $-6\mu A$, respectively, allow them to be generated with classical charge-pumps and limited overhead.

V. MEASUREMENTS

To verify the working principle of the proposed topology, the design is realized in a 28nm CMOS process using 9.5nF of MOM- and thick-oxide MOS-capacitance for the flying capacitors, in addition to 780pF for the bootstrap circuits. The MOS capacitors are biased with a high-impedant bias, V_{bias} , of 3V [13]. Figure 14 shows a micrograph of this realization, measuring $1.05mm^2$ in total. All cores are distributed over two rows to minimize the length of the top- and bottom-side intermediate nodes, as well as the control signals, both of which are positioned centrally.

A. Gyrator behavior

The gyrator behavior of the converter is verified by measuring the converter's input and load current versus the output voltage. This was achieved by setting the output voltage externally using a source meter that simultaneously measured the output current, while a second source meter measured the input current. These results are shown in Fig. 15. Compared with Fig. 8, it can be appreciated that the measured results match the expected behavior reasonably well. In addition, both currents scale linearly with the clock frequency, which demonstrates the converter's compatibility with frequency-control.

Fig. 15. Measured input- and output current versus output voltage for scaling F_{CLK} .

Fig. 16. Measured efficiency versus output voltage of the presented converter at $F_{CLK}=20MHz$.

B. Efficiency

Figure 16 plots the measured efficiency, including power consumed from all external rails, versus output voltage. The converter maintains a high efficiency over a wide VCR, staying above 80% efficiency from 0.43V to 2.13V, and above 90% from 0.9V to 2.03V. For output voltages larger than the input voltage of 2V, the efficiency drops rapidly. However, this is due to the fact that the converter was not designed to handle these output voltages, leading to body diode conduction.

The measured efficiency versus load current is shown in Fig. 17. Here, the load current is scaled by tuning the external clock frequency. A peak efficiency of 93% is witnessed at a V_{out} of 1.65V. Furthermore, the efficiency remains high down to 15-20% of the peak current, where the transistor leakage loss contribution becomes more significant.

C. Comparison

Table I compares the measurement results with the state-of-the-art of monolithic SC converters. The presented work achieves the largest output voltage range of all compared designs, and does so using a single topology. In order to allow for fair comparison between

TABLE I
DETAILED COMPARISON TO STATE-OF-THE-ART.

	This work [18]	[10]	[3]	[8]	[4]
Technology	28nm	40nm	130nm	65nm	180nm
Capacitors	MOM+MOS	MOM	Ferro Electric	MOS+MIM	MIM
V_{in} [V]	2	1.855-2.07	1.5	0.22-2.4	2
V_{out} [V]	0-2.22	0.9	0.4-1.1	0.85-1.2	0.2-1.87
Number of topologies	1	1	4	24	79
VCR range $\eta > 90\%$	0.56	0.04	0.05*	0	0.38
VCR range $\eta > 80\%$	0.85	0.05	0.17*	0.33*	0.7
Area [mm^2]	1.05	2.4	0.366	2.42	3.36
η_{peak}	93%	94.6%	93%	84.1%	95%
Topology control?	Not needed	/	Yes	No	No
P_D at η_{peak} [mW/mm^2]	4.6	1.3	1.32	13.2	0.13*

* estimate based on graphs

Fig. 17. Measured efficiency versus load current for several output voltages.

different designs using different input- or output voltages, the concept of an efficient VCR range can be used. Here, the largest continuous VCR range for which the converter stays above a certain efficiency is considered. Also, as an additional normalization step, the input and output voltages are swapped for step-up converters. From Fig. 18 it can be appreciated that the design has the highest VCR range above 80% efficiency, even when including gearbox converters that do not implement any kind of topology control.

VI. CONCLUSIONS

In this paper it was shown that, at a fundamental level, soft-charging provides an opportunity to make efficient SC topologies with large voltage swing capacitors. A single-capacitor topology using soft-charging was de-

Fig. 18. Comparison with state of the art of fully integrated SC converters.

rived that behaves like a gyrator. By increasing the number of intermediate soft-charging phases, the efficiency of the converter tends to 100% regardless of the voltage conversion ratio. Similar to regular converters, the proposed topology reaches a maximum efficiency at low power-densities, while at high power-densities the normalized losses scale with the cubic root of the power-density. A circuit was fabricated in a 28nm CMOS process that verified the working principle of the presented topology and advances the state-of-the-art by achieving a peak-efficiency of 93%, and a single-topology 0.9-to-2.03V output voltage range with more than 90% efficiency.

REFERENCES

- [1] J. F. Dickson, "On-chip high-voltage generation in mmos integrated circuits using an improved voltage multiplier technique,"

- IEEE Journal of Solid-State Circuits*, vol. 11, no. 3, pp. 374–378, 6 1976.
- [2] W. Kim, M. S. Gupta, G. Y. Wei, and D. Brooks, “System level analysis of fast, per-core DVFS using on-chip switching regulators,” in *High Performance Computer Architecture, 2008. HPCA 2008. IEEE 14th International Symposium on*, Feb. 2008, pp. 123–134.
 - [3] D. El-Damak, S. Bandyopadhyay, and A. P. Chandrakasan, “A 93% efficiency reconfigurable switched-capacitor DC-DC converter using on-chip ferroelectric capacitors,” in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, Feb. 2013, pp. 374–375.
 - [4] W. Jung, D. Sylvester, and D. Blaauw, “A rational-conversion-ratio switched-capacitor DC-DC converter using negative-output feedback,” in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, 1 2016, pp. 218–219.
 - [5] L. G. Salem and P. P. Mercier, “An 85%-efficiency fully integrated 15-ratio recursive switched-capacitor DC-DC converter with 0.1-to-2.2V output voltage range,” in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International*, Feb. 2014, pp. 88–89.
 - [6] S. Bang, A. Wang, B. Giridhar, D. Blaauw, and D. Sylvester, “A fully integrated successive-approximation switched-capacitor DC-DC converter with 31mV output voltage resolution,” in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, Feb. 2013, pp. 370–371.
 - [7] Y. T. Lin, W. H. Yang, Y. S. Ma, Y. J. Lai, H. W. Chen, K. H. Chen, C. L. Wey, Y. H. Lin, J. R. Lin, and T. Y. Tsai, “Unsymmetrical parallel switched-capacitor (up-sc) regulator with fast searching optimum ratio technique,” in *ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference*, 9 2017, pp. 287–290.
 - [8] Y. Jiang, M. K. Law, P. I. Mak, and R. P. Martins, “A 0.22-to-2.4V-input fine-grained fully integrated rational buck-boost SC DC-DC converter using algorithmic voltage-feed-in (AVFI) topology achieving 84.1% peak efficiency at 13.2mW/mm²,” in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, Feb. 2018, pp. 422–424.
 - [9] C. Schaef, J. S. Rentmeister, and J. Stauth, “Multimode Operation of Resonant and Hybrid Switched-Capacitor Topologies,” *IEEE Transactions on Power Electronics*, pp. 1–1, 2018.
 - [10] N. Butzen and M. Steyaert, “A 94.6%-Efficiency Fully Integrated Switched-Capacitor DC-DC Converter in Baseline 40nm CMOS using Scalable Parasitic Charge Redistribution,” in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, 1 2016, pp. 220–221.
 - [11] —, “A 1.1W/mm²-Power-Density 82%-Efficiency Fully Integrated 3:1 Switched-Capacitor DC-DC Converter in Baseline 28nm CMOS using Stage Outphasing and Multiphase Soft-Charging,” in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2017, pp. 178–179.
 - [12] N. Butzen and M. S. J. Steyaert, “Scalable Parasitic Charge Redistribution: Design of High-Efficiency Fully Integrated Switched-Capacitor DC-DC Converters,” *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 2843–2853, 12 2016.
 - [13] —, “Design of Soft-Charging Switched-Capacitor DC-DC Converters Using Stage Outphasing and Multiphase Soft-Charging,” *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3132–3141, 12 2017.
 - [14] M. S. Makowski and D. Maksimovic, “Performance limits of switched-capacitor dc-dc converters,” in *Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE*, vol. 2, 6 1995, pp. 1215–1221 vol.2.
 - [15] M. D. Seeman, “A Design Methodology for Switched-Capacitor DC-DC Converters,” Ph.D. dissertation, EECS Department, University of California, Berkeley, 5 2009. [Online]. Available: <http://www.eecs.berkeley.edu/Pubs/TechRpts/2009/EECS-2009-78.html>
 - [16] H. P. Le, S. R. Sanders, and E. Alon, “Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters,” *IEEE Journal of Solid-State Circuits*, vol. 46, no. 9, pp. 2120–2131, 9 2011.
 - [17] H. Meyvaert, G. V. Pique, R. Karadi, H. J. Bergveld, and M. S. J. Steyaert, “A Light-Load-Efficient 11/1 Switched-Capacitor DC-DC Converter With 94.7% Efficiency While Delivering 100 mW at 3.3 V,” *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 2849–2860, 12 2015.
 - [18] N. Buzen and M. Steyaert, “A Single-Topology Continuously-Scalable-Conversion-Ratio Fully Integrated Switched-Capacitor DC-DC Converter with 0-2.22V Output and 93% Peak-Efficiency,” in *VLSI Circuits, 2018 Symposium on*, 6 2018, pp. 103–104.