Backup Protection Algorithm for Failures in Modular DC Circuit Breakers

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***Abstract*—HVDC grid protection with adequate speed and reliability is required to minimise the impact of DC faults. In particular, fast breaker failure backup protection algorithms are needed to meet the expected reliability requirements of HVDC grids. In this paper, existing breaker failure backup protection algorithms are shown inadequate to detect partial failures like a single module failure of breakers with a modular structure. This paper proposes a backup protection algorithm which rapidly detects a DC breaker failure based on estimating the counter-voltage created by the energy absorption branch during an interruption. The performance of the proposed algorithm is evaluated using a four-terminal test network with both hybrid and mechanical DC breaker technologies. The simulation results show that the proposed algorithm is able to quickly detect both complete and partial failures of the two breaker technologies even considering measurement errors, noise and ageing of the energy absorption components.**

***Index Terms*—HVDC grid protection, DC circuit breaker, breaker failure, backup protection algorithm**

I. Introduction

Voltage source converter (VSC) based high voltage direct current (HVDC) grids are expected to play a key role through bulk transmission capacity to support decarbonisation of electricity generation [1]. For large-scale HVDC grids, selectively protecting the grid against DC faults is essential to ensure the required reliability and flexibility to deal with the variable nature of renewable energy generation [1]. In an HVDC grid, the rapid increase of the prospective fault current requires fast fault current interruption both to prevent damage to semiconductor-based components and to allow for successful interruption within the limited breaking capability of DC circuit breakers (DCCBs) [2]. Consequently, fast fault detection algorithms and DCCBs are required.

In a selective protection scheme, backup protection should be provided to isolate the faulty element in the case of failure or unavailability of primary protection components, such as the intelligent electronic device (IED) or circuit breaker, to meet the expected reliability requirements for large-scale HVDC grids [1], [3]. Considering the complexity and novelty of DCCB technologies, breaker failure backup protection is of particular significance in HVDC grids to prevent the prospective fault current reaching dangerous levels [1].

Numerous DCCB technologies have been proposed in the literature to address the technical challenges in interrupting a DC current and dissipating the inductive energy stored in the circuit [4]. The most promising options are the hybrid and mechanical types, which have been prototyped and tested in laboratory environment [5]–[7], and installed in several HVDC systems in China [8]–[11]. A modular design is typically adopted to achieve the required voltage level for HVDC applications [5], [6], [11], [12]. For example, breaker modules rated at 80 kV/100 kV are proposed to be connected in series to attain the required voltage withstand ability for voltages up to 320 kV/500 kV [5], [6].

Due to a limited operational experience, a large number of components and complex circuit structures compared with AC circuit breakers (ACCBs), the failure modes and mechanisms of DCCBs have not yet been thoroughly investigated in the literature. Furthermore, the failure modes and mechanisms vary significantly between different DCCB technologies. In [13], [14], the authors have provided the first insights on failure modes of a hybrid and mechanical DCCB using hardware small-scale test set-ups and electromagnetic transient (EMT) simulations. The results from [13], [14] have shown that most realistic failures are those on components in a single module (such as power electronic switches, surge arresters), resulting in one module failing into a short-circuit.

The breaker failure backup protection algorithms proposed in the literature are inadequate to provide a high detection speed or to address a single-module failure. The overcurrent criterion proposed in [15] is able to activate backup protection only after the longest primary fault clearing time, which is in the order of tens of ms. The current derivative (di/dt) algorithm [16], local measurements-based algorithm [17] and quickest change detection (QCD) algorithm [18] are capable of providing a fast detection speed. However these algorithms have been developed considering failures of the whole breaker, and thus may fail to detect failures of a single module. The breaker failure detection algorithm proposed in [19] uses currents of various branches measured internally for the specific DCCB, which may not be available to the local IED. In addition, the algorithm is not likely to be applicable to different breaker technologies or topologies. The limitations of existing breaker failure detection algorithms will be analysed in detail in section III-C.

In order to overcome the limitations of existing breaker failure detection algorithms, this paper proposes a novel fast breaker failure backup protection algorithm particularly to detect both failures of the whole breaker and of a single module for various DCCB technologies. Generalised characteristics of successful fault clearings and component failures are inves-

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tigated in order to propose such an algorithm, considering two DCCB technologies. The main feature of the proposed algorithm is fast detection of a breaker failure by estimating the counter-voltage across the energy absorption branch during fault current interruption. The proposed algorithm is generally applicable, as a parallel energy absorption branch is universally used in existing DCCB technologies to create the necessary counter-voltage. The robustness of the proposed algorithm is validated considering worst conditions for measurement errors and ageing of the energy absorption branch, as defined in relevant standards by the International Electrotechnical Commission (IEC).

This paper is structured as follows. Section II gives an introduction to a selective HVDC grid protection system. Section III first provides a brief review on failure modes studied in the literature and characterises breaker failure transients using two DCCB technologies in a four-terminal test grid. Section IV presents the proposed breaker failure backup protection algorithm. Simulation and sensitivity analysis are provided in section V using the four-terminal test system. Finally, section VI summarises conclusions of this paper.

II. HVDC GRID PROTECTION

A. Selective protection scheme in HVDC grids

Large-scale HVDC grids are required to be selectively protected in order to minimise the impact of DC faults by confining the fault clearing to the faulted component [2]. In a selective protection scheme, each line is protected by DCCBs at both ends with their associated IEDs. A simplified schematic diagram of a selectively protected HVDC grid is shown in Fig. 1, with details depicted for IED_1 at a functional level.

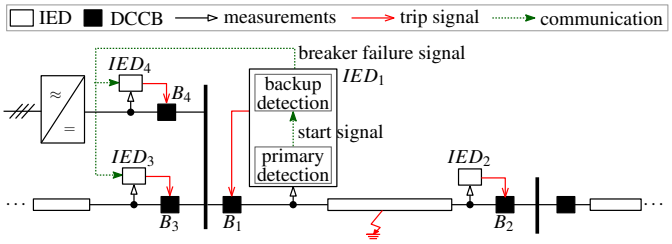

Fig. 1. Simplified schematic diagram of a selectively protected HVDC grid (details indicated for IED_1 with functional blocks).

As shown in Fig. 2 (a), after the fault-initiated travelling wave arrives at the measurement position, the primary IED detects a fault and sends a trip signal to the associated DCCB. If the primary protection breaker fails, the local IED (IED_1 in Fig. 1) detects a breaker failure, and sends the signal to the adjacent IEDs (IED_3 to IED_4 in Fig. 1) to trip the adjacent DCCBs. Depending on the backup protection algorithm, a breaker failure can be detected prior to [17] or after [15] primary fault clearing. The operating time of a breaker failure backup protection IED (t_{BF}) can be defined as the time interval from the fault inception instant (t_f) to the instant when a breaker failure tripping signal is generated (t_t^b). In addition, a breaker failure detection time (t_d^b) can be defined from the prospective breaker opening instant (t_o^p) instead of fault arrival

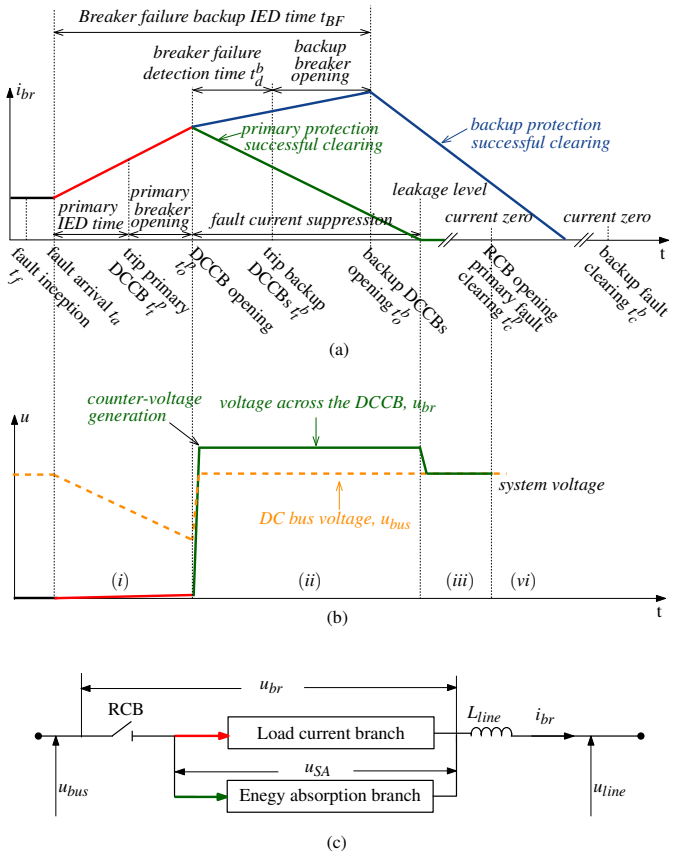

Fig. 2. Primary and breaker failure backup protection timelines and simplified schematic illustration of (e.g. breaker B_1 in Fig. 1), (a) breaker current, (b) DC bus and breaker voltages, and (c) a generic DCCB ($u_{br}, u_{SA}, u_{bus}, u_{line}$: voltage across the breaker, voltage across the energy absorption branch, DC bus-side voltage, DC line-side voltage).

which can better represent the speed of a breaker failure detection algorithm since the breaker opening time varies from a few ms to tens of ms [4].

B. Breaker technologies and operating principles

DCCBs are broadly grouped into passive oscillation, mechanical, hybrid and pure power electronic types [4]. Despite the differences in the interruption technologies and operating speeds, each DCCB topology includes at least a load current branch and an energy absorption branch (Fig. 2 (c)). In addition, a residual circuit breaker (RCB) and a line inductor are typically used to isolate the faulty line to protect the energy absorption branch from thermal overload and to limit the rate-of-rise of the current [4].

After receiving a trip signal from the IED, a successful interruption can be divided into four stages, as shown in Fig. 2 (a) and (b). (i) the DCCB creates local current zero-crossing(s), for instance, by using power electronic or mechanical switches. During this stage, the breaker current (i_{br}) is increasing while the DC bus voltage (u_{bus}) is decreasing. (ii) a counter-voltage u_{SA} higher than the system voltage is build up by the energy absorption branch to drive the fault current to zero. This process is commonly referred to as fault current suppression [4]. (iii) the RCB can safely open after the current has reached

a leakage level. In the meantime, the DC bus voltage (u_{bus}) recovers to the system voltage. (vi) the fault is cleared and the HVDC system can recover. The DCCB also needs to absorb the inductive energy stored in the system and withstand the voltage across its terminals during the interruption process as well as after fault clearing (the system voltage u_{bus} as shown in Fig. 2 (b)).

In this paper, hybrid and mechanical DCCBs are used as examples to investigate breaker failure mechanisms and demonstrate the proposed breaker failure backup protection algorithm. The hybrid DCCB consists of two parallel branches, a load current branch, and a main breaker (MB, T_2) branch (Fig. 3 (a)). The load current branch is composed of an ultra fast disconnector (UFD) and a load commutation switch (LCS, T_1). The main breaker typically has a modular design with several modules, each consisting of a string (or an array) of power electronic switches for the current interruption and parallel surge arresters (SAs) for energy absorption. Both the LCS and the MB valves can be realized by insulated gate bipolar transistors (IGBTs) or bimode insulated gate transistors (BIGTs) [6], [20].

The mechanical DCCB uses high-speed making switches (HSMS, S_3) to inject an oscillating AC current to the load current branch, by switching in an LC current injection (CI) branch with a pre-charged capacitor. The current is then interrupted by vacuum interrupters (VI, S_1). As shown in Fig. 3 (b), a modular design of the mechanical DCCB is typical, where each module is composed of a separate current injection circuit, a surge arrester and a parallel vacuum interrupter [5]. RCBs are used in both mechanical and hybrid DCCBs to provide isolation.

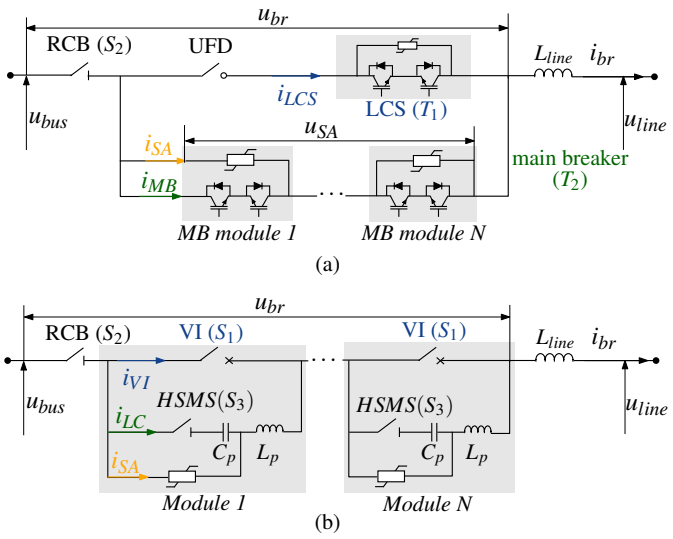

Fig. 3. Example DCCB technologies (a) a hybrid type [6] and (b) a mechanical type [5].

III. Breaker Failure Modes and Characterisation

A. Breaker failure modes

Breaker functional failure modes can be categorized into fail-to-open, fail-to-close and spurious operation (including opening while it should be closed or vice versa) [14]. Fail-to-open (on command) during a DC fault is the most relevant mode for breaker failure backup protection, and is therefore summarised in this section based on the results in [13], [14].

1) Hybrid DCCB: Complete failures of the LCS and the entire MB valves are considered extremely unlikely as they are built with high redundancy [6], [20]. However, malfunctions of the gate unit drivers, the DCCB internal controller and power supply are possible, which can lead to failures of individual power electronic switches, the LCS valve, one MB module or the whole MB valve.

The surge arresters in a DCCB are subjected to different stresses compared to those used for overvoltage protection, as carrying a high current of several kA for a few milliseconds is required in DCCB applications. They are therefore exposed to the largest thermal loading among the DCCB components. Their failure rates also depend on the installation environment as hybrid DCCBs are likely to be placed indoors, which may reduce the risk of surge arrester failure due to moisture or pollution. The surge arresters may fail in the middle of the current suppression process due to degradation or excessive energy absorption. This may pose a challenge for breaker failure detection as it will be explained in Section III-C. When surge arresters of a single MB module fail, the decreasing fault current resembles a successful interruption due to the counter-voltage created by the remaining healthy MB modules.

The failure rate of the UFD can be expected to be higher than existing disconnectors as the extremely fast opening speed imposes stringent requirements on the contacts and actuator [21]. In addition, ultra fast disconnection is a novel technology with very limited manufacturing and operational experience. The RCB is less likely to fail as the existing ACCB technology can be used for this application.

2) Mechanical DCCB: Failures of a mechanical DCCB include failures of the key components: (1) the vacuum interrupter(s), (2) current injection circuit, and (3) the RCB. Failure of the VI can be caused by reasons such as scatter of the opening times of individual interrupters, degraded contacts, malfunction of the actuator, or auxiliary system failure, which can result in arcing or remaining in a closed position [14]. The most likely cause for a current injection failure is inaccurate injection timing due to malfunction of the HSMS, auxiliary power supply or control system [14]. The stresses on the surge arresters and RCB of a mechanical DCCB are similar to those in a hybrid DCCB.

3) Summary: Considering the resulting transients from the detection system point-of-view and the probability of failure, the following failures are investigated in detail in the remainder of the paper: i) the LCS surge arrester, the UFD, the surge arresters of one MB module, and the whole hybrid DCCB and ii) the vacuum interrupter and current injection of one module, and the whole mechanical DCCB. Failures which result in similar transients as cases listed above are not considered to avoid repetition. For instance, a failure of the main breaker valve of one module will lead to similar transients as a failure of the surge arresters of one module. Thus, the behaviour of the breaker failure detection algorithm is similar in these two cases.

B. Test system

A four-terminal cable-based symmetrical monopolar test system based on the model in [22], [23] is used to study the breaker failure transients and detection algorithm.

1) Converter model: Half-bridge modular multilevel converters (MMCs) are modelled with a Type 4 detailed equivalent circuit model as specified in [24]. During normal operation, MMC2 and MMC4 are operating in active power control mode, exporting 600 MW and 1000 MW, respectively. MMC1 and MMC3 are operating in voltage power droop control mode, importing 1200 MW and 400 MW, respectively. The main parameters of the converter station are listed in Table I.

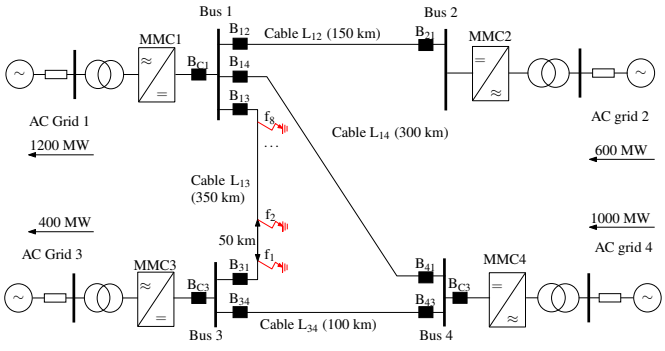

Fig. 4. A four-terminal symmetrical monopolar test system (DCCBs are indicated with ■).

TABLE I
CONVERTER AND GRID PARAMETERS

Parameters	Value	Unit
Rated apparent/active power S/P_{DC}	1265/1200	[MVA/MW]
Rated DC voltage U_{DCp},U_{DCn}	± 320	[kV]
Rated transformer voltages	400/333	[kV]
Transformer leakage impedance	0.18	pu
submodule capacitance C_{SM}	1760	[μF]
Arm inductance L_{arm}	42	[mH]
Converter DC smoothing reactor L_{DC}	10	[mH]
Line inductor L_{line}	100	[mH]

2) DCCB models: Detailed hybrid and mechanical DCCB models for system-level studies are used in this paper based on models developed in [25], [26]. Both hybrid and mechanical DCCBs have a rated voltage of 320 kV with four 80 kV modules and a rated breaking current of 16 kA [25], [26].

Failure mechanisms of various components and the associated voltage and current transients have been analysed in detail in [13], [14], [27]–[29]. These studies show that the resulting voltage across the failed component (power electronic switches, mechanical switches and surge arresters) is considered negligible compared to the system voltage, and the failed component can be viewed as by-passed. Therefore, the failure modes are modelled by short-circuiting the associated component(s) [13], [14], [27]–[29]. These references also provide further details on failures of power electronic switches, mechanical switches and surge arresters.

Main parameters of the DCCBs are given in Table II.

TABLE II
MAIN PARAMETERS FOR DCCBS

DCCB	Parameters	Value	Unit
Hybrid	UFD opening time	2	ms
	UFD residual current	1	A
	RCB opening time	20	ms
	RCB residual current	10	A
Mechanical	Opening times for VI and RCB	8	ms
	HSMS closing time	8	ms
	Residual current for VI and RCB	10	A

C. Breaker failure characterisation

Breaker B_{31} is used as an example to study breaker failure detection by applying pole-to-pole faults on cable L_{13} at various locations. A complete failure is simulated by short-circuiting the whole DCCB. Failures of a single module are simulated by short-circuiting the surge arrester of one MB module at 0 ms to 5 ms after the prospective breaker opening instant with a 1 ms step.

From the detection system point-of-view, the characteristics of the line current (i_{br}), the DC bus voltage (u_{bus}), and the voltage across the breaker (u_{br}), as depicted in Fig. 2, are of importance. Their waveforms are analysed considering the hybrid and mechanical DCCBs as shown in Fig. 5 and Fig. 6, respectively. In particular, based on the counter-voltage generated during interruption, the characteristics of the voltage across the breaker (u_{br}) can be categorized as either complete or partial failure, as shown in Fig. 5 (d) and Fig. 6 (d). Complete or partial failure of a DCCB leads to respectively zero or partial counter-voltage being built up, compared with a full counter-voltage during a successful fault clearing. Complete failures include failure of the whole breaker or common components of a modular structured DCCB, such as the LCS and UFD of the hybrid DCCB or the controller of the mechanical DCCB. Partial failure is caused by a failure of one module, such as the surge arrester of one MB module of the hybrid DCCB, or the VI in one module of the mechanical DCCB.

D. Limitations of existing algorithms

Complete failures can be readily distinguished from successful clearings using the di/dt calculated from a few sampling points, e.g. five samples as studied in [22], since the di/dt remains positive after the presumed breaker opening instant, while it becomes negative for successful clearings (Fig. 5 (b)). However, it is more cumbersome to find a di/dt threshold to detect single-module failures, as the di/dt becomes negative after the breaker opening instant, similar to a successful clearing. In addition, the di/dt of a successful clearing can be larger than zero during the clearing process due to the reflected travelling waves.

The local measurement-based algorithm proposed in [17] can detect complete failures by using distinct features for cleared and uncleared faults, namely, low current and high voltage for cleared and the opposite for uncleared faults. However, such features cannot easily be found for single-module failures as shown in Fig. 5 (a), (c) and Fig. 6 (a), (c). The resulting currents and voltages have very similar features

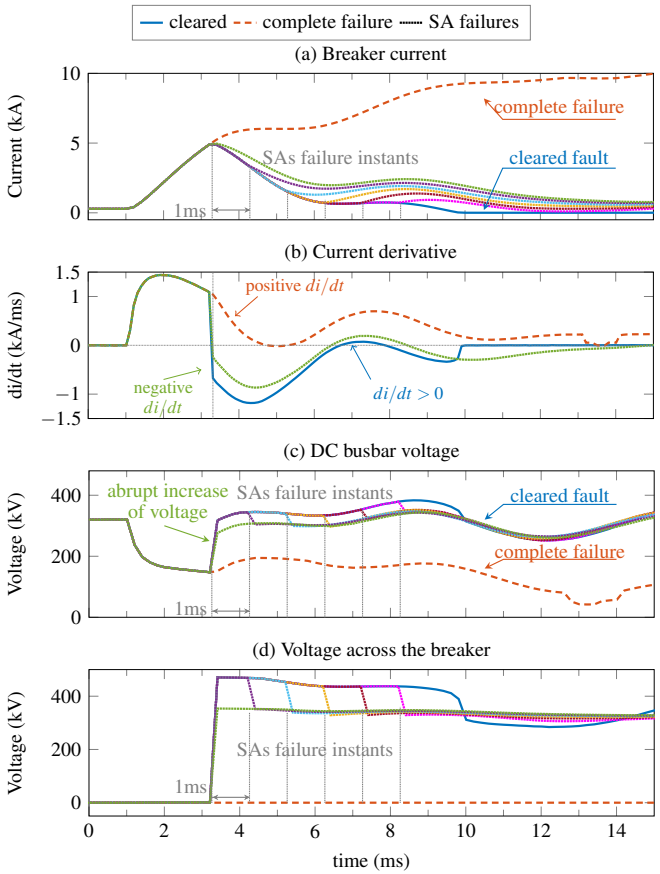

Fig. 5. Hybrid DCCB: voltages and currents during successful clearing and breaker failures, solid line: successful clearing, dashed line: failure of the whole breaker, dotted lines: partial failure (surge arrester of one module failure), fault location: 200 km from DC bus 3.

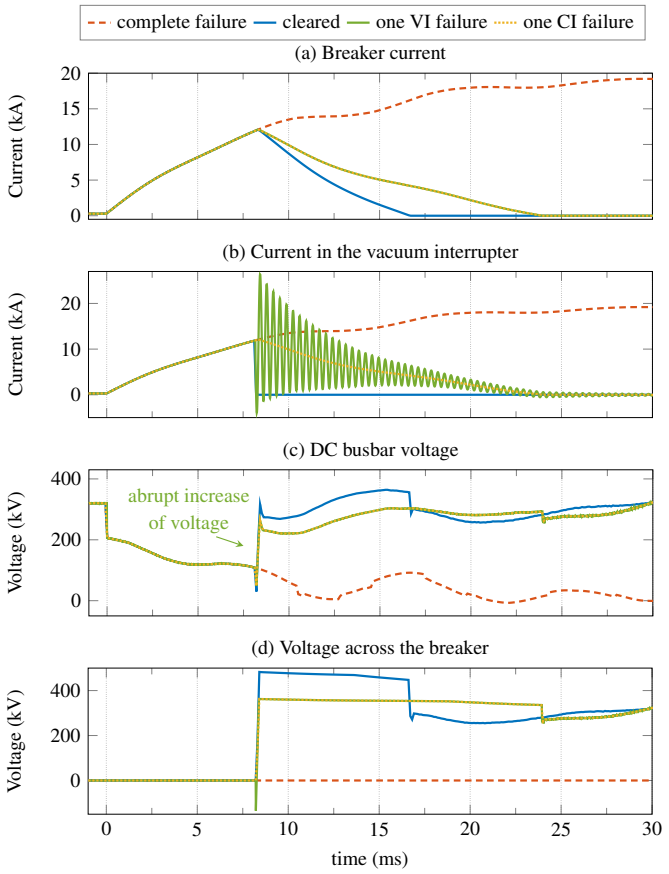

Fig. 6. Mechanical DCCB: voltages and currents during successful clearing, whole breaker failure and failures of one breaker module, (fault location: cable terminal near DC bus 3).

as the successful fault-clearing cases, particularly at the failure instants towards the end of the current suppression period.

The quickest change detection (QCD) based algorithm proposed in [18] essentially identifies a breaker failure by using the abrupt change in the DC bus voltage, occurring since the DCCB builds up a counter-voltage at the moment of breaker opening (Fig. 5 (c) and Fig. 6 (c)). However, this algorithm may fail to detect a single-module failure, as the DC bus voltage still rises quickly as a partial counter-voltage is generated by the remaining healthy modules.

IV. Proposed Breaker Failure Backup Protection Algorithm

As analysed in section III-C, the voltage signal gives the best observability between successful clearing, partial and complete failure (Fig. 5 (c)). This paper proposes a backup protection algorithm which compares the expected and estimated counter-voltages across the surge arresters during an interruption.

As shown in Fig. 2 (c), during the current suppression process, the expected total counter-voltage generated by the surge arresters ($u_{SA.exp}$) can be calculated by equation (1a), which is the sum of the expected counter-voltage generated by surge arresters in each module. The non-linear resistance of the surge arrester of each module (R_{SAk}) can be expressed as piece-wise linear resistances using the voltage-current (U-I) characteristics typically given in the datasheet. During the current suppression period, the actual counter-voltage generated by the surge arresters ($u_{SA.est}$) is approximately the voltage across the breaker u_{br}. The actual counter-voltage can thus be estimated by equation (1b).

$$\begin{cases} u_{SA.exp} = \sum_{k=1}^{Nm} R_{SAk} i_{br} & \text{(1a)} \\ u_{SA.est} = u_{bus} - u_{line} - L_{line} \dfrac{di_{br}}{dt} & \text{(1b)} \end{cases}$$

where $u_{SA.exp}$ and $u_{SA.est}$ are the expected and estimated counter-voltages; N_m is the number of the breaker modules; R_{SAk} is the non-linear resistance of the surge arrester of module k; u_{bus}, u_{line} are the measured voltages at the DC bus and line side, respectively; i_{br} is the measured line current.

For a successful fault clearing, the difference between $u_{SA.exp}$ and $u_{SA.est}$ should in principle be zero. On the contrary, for a failure of the whole DCCB or one module, the voltage difference should be 1.5 pu or $1.5/N_m$ pu considering that the surge arresters are typically chosen to have a clamping voltage of approximately 1.5 pu of the system voltage [5], [6]. A breaker failure can thus be detected using a counter-voltage

criterion and a current criterion, as described by equation (2).

$$\begin{cases} \Delta u_{SA} = u_{SA.exp} - u_{SA.est} > U_{thr},\ AND \\ i_{br} > I_{thr} \end{cases} \quad t_1 < t < t_2 \qquad (2)$$

where U_{thr} and I_{thr} are the voltage and current detection threshold; t_1 and t_2 are the start and end of the current suppression period. The detection window can be ideally set from the prospective breaker opening instant to the RCB opening instant.

The voltage threshold U_{thr} can be determined by considering the maximum Δu_{SA} of successful clearing cases and the minimum Δu_{SA} of failed cases. The current criterion is used to prevent false detection during successful clearing. The main reason is that the surge arrester has high non-linearity in the very low current region as shown in Fig. 7. Consequently, even a small difference of the leakage current level between the measured breaker current i_{br} and the surge arrester current i_{SA} can lead to a large difference in the estimated counter-voltage $u_{SA.exp}$ in this highly non-linear region. The current threshold I_{thr} can be set as the residual current level of the RCB.

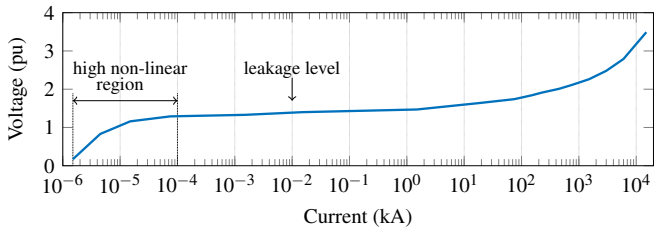

Fig. 7. Voltage-current characteristic of the surge arrester [26].

A failure of the RCB has insignificant influence on the system-level response of the DCCB [6], [14]. However, it may lead to overloading of the surge arresters on a long time period due to the leakage current [6]. For a mechanical DCCB, there will be small oscillating components in the line current and the DC bus voltage due to the LC injection branch is not isolated [14]. In addition, a failure of the RCB may impact the HVDC system recovery speed. Additionally, an overcurrent criterion can be used in parallel with the counter-voltage criterion (eq. (2)) to detect a RCB failure.

$$i_{br} > K_1 I_{RCB,res},\ t > K_2 t_3 \qquad (3)$$

where $I_{RCB,res}$ is the residual current level of the RCB, t_3 is the longest primary fault clearing time, and K_1, K_2 are the detection margin coefficients.

The proposed algorithm is considered widely applicable, since all known DCCB technologies employ surge arresters for the energy absorption branch and a modular structure [4]–[6]. It is tested for two generic implementations of the main breaker technologies: hybrid and mechanical.

V. Simulation Studies

A. IED implementation in PSCAD

A two-out-of-three voting scheme is used for primary fault detection based on a non-unit protection algorithm [30], travelling wave derivative algorithm [31] and travelling wave direction algorithm [32].

Fig. 8 presents a simplified block diagram of the proposed breaker failure backup protection. The trip or fault identification (FI) signal from the primary fault detection is used as the start signal for the breaker failure backup protection. The start of the detection window (T_1 in Fig. 8) for the counter-voltage criterion (U_{det}) is $t_t^p + t_{br,o} + t_{mgn}$, which is the expected breaker opening instant plus a small margin (t_{mgn} = 0.5 ms). The margin is considered in order to remove the impact of variations in the breaker opening time and initial transients. The length of the detection window T_1 is set as the longest primary clearing time. The detection window (T_2 in Fig. 8) for the overcurrent criterion (I_{det}) for RCB failure detection can be set starting from the longest primary clearing time until the IED reset time. If a breaker failure is detected by any of these two criteria, a breaker failure (BF) signal is sent to the adjacent IEDs to trip the backup DCCBs. The voltage threshold U_{thr} is set as 60 kV and the current threshold I_{thr} is set as the residual current of the RCB ($I_{RCB,res}$ = 10 A).

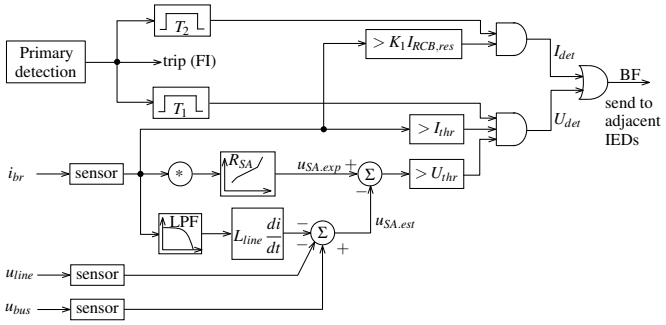

Fig. 8. Simplified block diagram of the proposed breaker failure backup protection.

A simplified sensor model as detailed in Section V-D is used for measured quantities. The nonlinear resistance of the surge arrester is implemented using a lookup table. A moving average smoothing filter is used when calculating the current derivative for noise removal as studied in [22].

B. Example cases

A pole-to-pole fault is applied at the cable terminal near DC bus 3, and the DCCB B_{31} is used as an example to study the performance of the proposed breaker failure detection algorithm. All the DCCBs are represented as either hybrid or mechanical types in corresponding cases.

1) Complete failure of a whole breaker: The failure of a whole breaker is simulated by short-circuiting the DCCB. The performance of the proposed algorithm at detecting a whole breaker failure is shown in Fig. 9 using the mechanical DCCB as an example. The difference between the expected ($u_{SA.exp}$) and estimated ($u_{SA.est}$) counter-voltages is approximately 480 kV (Fig. 9 (c)), this allows the proposed algorithm to immediately detect this voltage difference and imitate the breaker failure backup protection sequence.

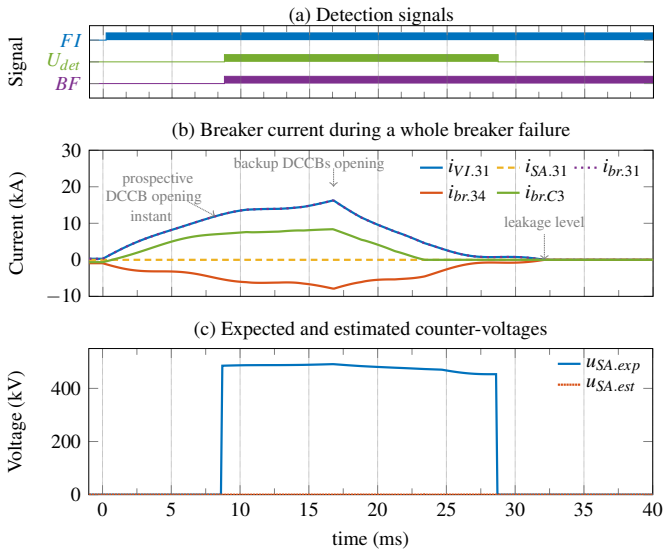

Fig. 9. Mechanical DCCB: breaker failure detection and backup fault clearing during a whole breaker failure.

2) One MB module surge arrester failure of the hybrid DCCB: The surge arrester of one MB module is set to fail at 5 ms after the prospective breaker opening instant, which leads to a difference in the expected and estimated counter-voltages of approximately 114 kV (Fig. 10 (c)). The proposed algorithm can almost immediately detect this voltage difference (e.g. 0.16 ms after the surge arrester failure) and send a breaker failure signal (BF) to the adjacent IEDs to trip the backup breakers. The backup fault clearing time, in this case, is less than 10 ms.

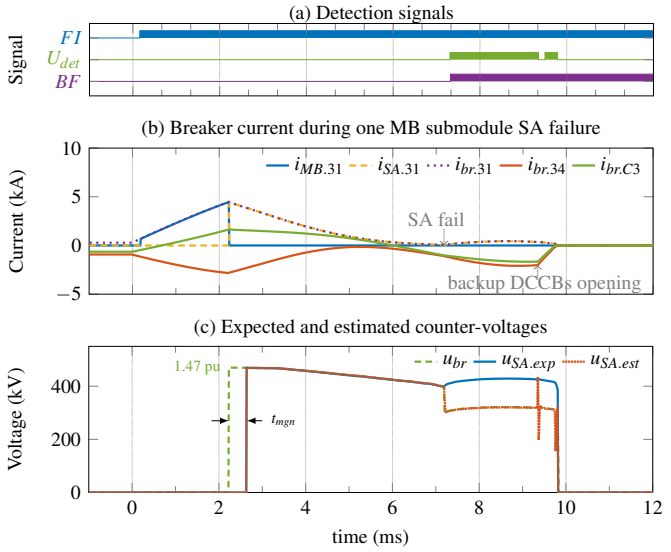

Fig. 10. Hybrid DCCB: backup fault clearing during one MB module surge arrester failure (failed instant 5 ms after t_o^p).

3) One module VI failure of the mechanical DCCB: The difference between the expected and estimated counter-voltages is approximately 122 kV during a VI failure of one module of the mechanical DCCB as shown in Fig. 11 (c). The failure is detected 0.6 ms after the prospective breaker opening instant, which results in a backup fault clearing time of 18.4 ms. Compared with the hybrid DCCB case (Fig. 10), the longer fault clearing time is mainly due to the opening speed of the mechanical DCCBs.

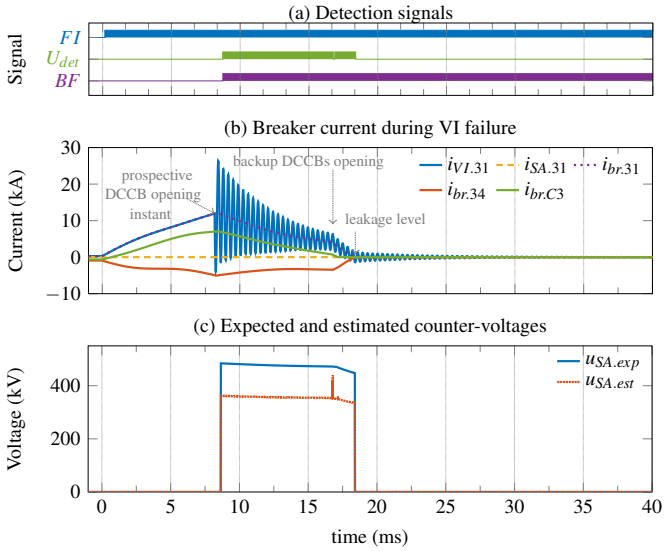

Fig. 11. Mechanical DCCB: breaker failure detection and backup fault clearing during one breaker module VI failure.

C. Detection time evaluation

The breaker failure detection time (t_d^b) is evaluated for the proposed breaker failure detection algorithm, considering failures of the LCS surge arresters, UFD, the surge arrester of one MB module, the whole hybrid DCCB, the VI and current injection of one module and the whole mechanical DCCB. As shown in Fig. 12, for component failures assumed before the prospective breaker opening instant, the breaker failure detection time is approximately 0.6 ms, which is the sum of the margin (t_{mgn}) and the algorithm decision time. For surge arrester failures assumed after the prospective breaker opening instant, the breaker failure detection time is the sum of the failed time (t_{SA}=0 ms to 5 ms after the prospective breaker opening instant) and the algorithm decision time. The proposed algorithm has a maximum decision time of 0.16 ms for all the simulated cases. This demonstrates that the proposed algorithm is able to detect both complete and partial failures in a short time.

D. Impact of inaccuracy of measurements and surge arrester characteristics

The robustness of the proposed breaker failure backup protection algorithm is evaluated considering measurement accuracy, noise, and inaccuracy of the surge arrester U-I characteristics.

For the DC voltage and current measurements, a reduced sensor model (Fig. 13), including a delay, a low-pass filter, and inaccuracy is considered [23]. The worst conditions as specified in IEC 61869 standards are considered for the

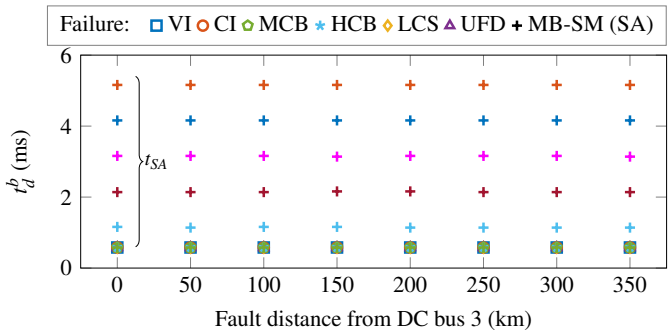

Fig. 12. Breaker failure detection time t_d^b (Legend VI/CI: one module VI or current injection circuit failure, HCB/MCB: whole breaker failure of the hybrid/mechanical DCCB, MB-SM (SA) one MB module surge arrester failure, failed time t_{SA}: 0 ms to 5 ms after t_o^p).

primary sensor delay, noise level and accuracy class, as listed in Table III. The low-pass filter for voltage and current measurements has a sampling frequency of 100 kHz with a bandwidth of $0.2f_s$ as studied in [33].

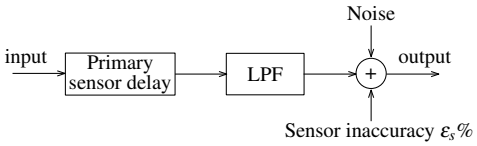

Fig. 13. Simplified sensor model [23].

TABLE III
SPECIFICATIONS ON MEASUREMENTS IN IEC 61869-14/-15 [34], [35]

Parameter	Value	Considered value
Primary sensor delay	τ_s = 5μs/25μs/100μs	100μs
Accuracy class	ε_s%=0.1/0.2/0.5/1	1%
Noise to signal ratio	-70dB to -50dB	-50dB

The U-I characteristics of the surge arresters are typically well matched by the manufacturers as a small mismatch could cause disproportionate scatter in energy sharing among the surge arresters [4], [14]. However, inaccuracy of the surge arrester characteristics used in the detection algorithm can be introduced due to measurement inaccuracy or ageing. Ageing can occur both due to environmental factors and repeated use, and can result in a considerable increase of the U-I characteristics in the protection-level current region [36], [37]. Similar to the accuracy class of the measurement devices, a 0.1% to 1% measurement error is considered for the accuracy of the surge arrester characteristics (ε_{SA}%). A maximum 5% increase in the protection-level current region is considered based on IEC standard [38] and experimental results in [36].

The inaccuracies of the measurements and surge arrester characteristics reduces the counter-voltage threshold margin between the failure and successful clearing cases. As shown in Fig. 14, in comparison with the base case without considering any inaccuracy, the minimum Δu_{SA} for the failed cases decreases from 112.2 kV to 104.3 kV; whereas, the maximum Δu_{SA} for the successful clearing cases increases from 20.5 kV to 31.5 kV, when considering 1% sensor error

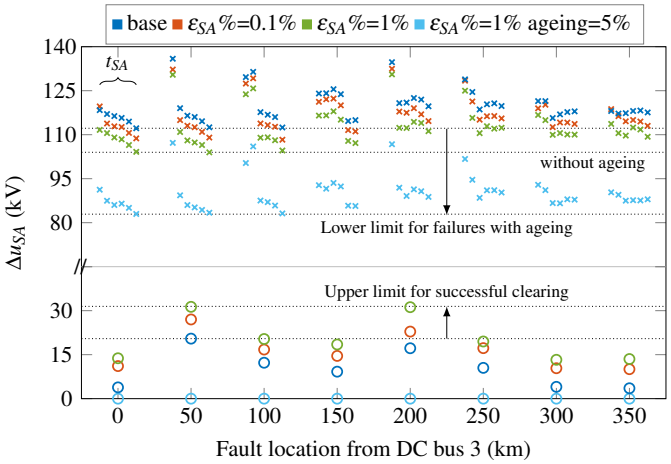

Fig. 14. Differences between expected and estimated counter-voltages (base case: without considering any inaccuracy of measurements and surge arrester characteristics).

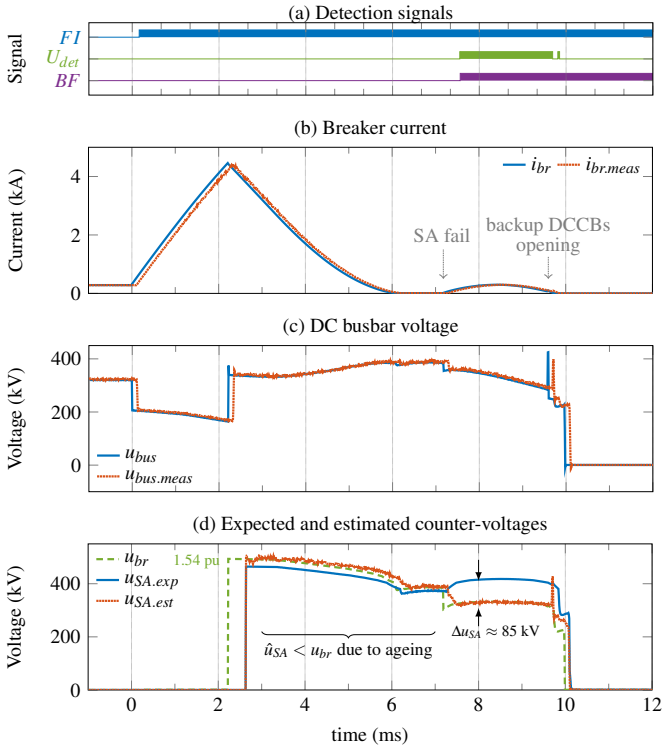

Fig. 15. Hybrid DCCB: impact of even ageing on the proposed algorithm (subscript meas: measurements with 1% sensor error and -50dB noise; ageing=5% on all four modules).

and 1% inaccuracy of the surge arrester U-I characteristics due to measurement error. When an additional 5% ageing of the surge arrester characteristics is considered, the Δu_{SA} for the failed cases further decreases to 83 kV. However, a voltage threshold of 60 kV is considered to allow for a sufficient margin to ensure both dependability (sufficiently below the failure gives the lowest Δu_{SA}) and security (sufficiently above the successful clearing case gives the highest Δu_{SA}), even considering the inaccuracy of measurements and surge arrester characteristics.

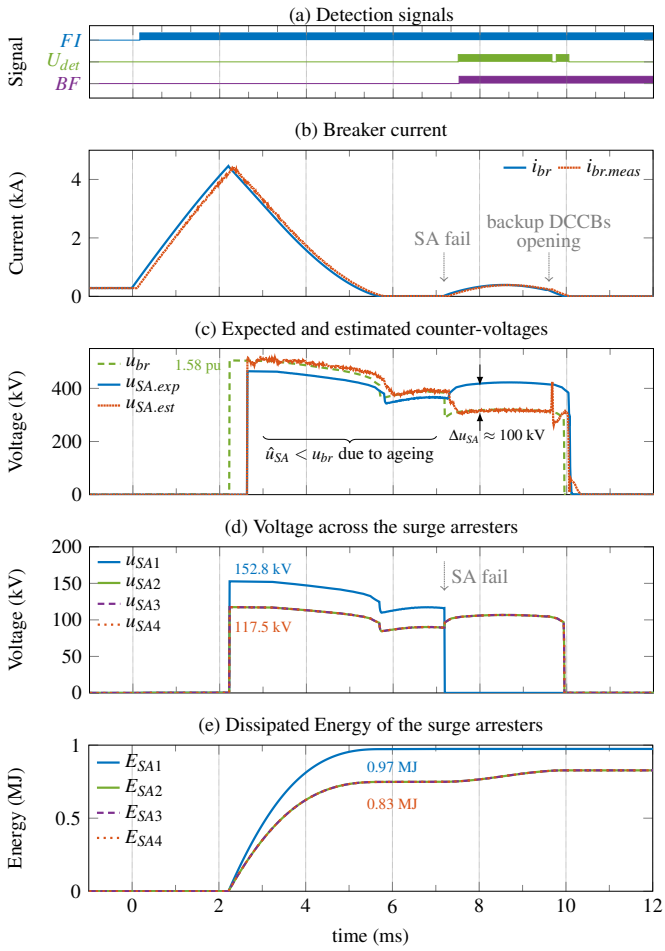

Fig. 16. Hybrid DCCB: impact of uneven ageing on the proposed algorithm (subscript meas: measurements; ageing=30% on MB module 1).

The robustness of the proposed algorithm is demonstrated considering both even and uneven ageing between the surge arresters of different modules. Both cases are studied with the surge arrester of one MB module failing at 5 ms after the prospective breaker opening time for a pole-to-pole fault at cable terminal near DC bus 3.

1) Even ageing of the surge arresters: Even ageing of 5% of the surge arresters distributed in all MB modules is considered in this case. First, the inaccuracy of the sensors leads to delayed measurements superimposed with noises as compared to the real current and voltage in the circuit, as shown in Fig. 15 (b) and (c). The 1% inaccuracy of surge arrester characteristics considering measurement errors and additional 5% ageing increases the counter-voltage across the DCCB (u_{br}) as compared to the expected counter-voltage $u_{SA.exp}$ before breaker failure (Fig. 15 (d)). The breaker failure is detected 0.4 ms after the surge arrester failure instant, which is only slightly longer than the case without considering the inaccuracies (Fig. 10).

2) Uneven ageing of the surge arresters: Uneven ageing among the surge arresters of different MB modules is considered in this case, with a 30% ageing of the surge arrester in MB module 1 and no ageing of the rest MB modules. This is considered as an extreme case of a very large difference of the surge arrester degradation between the breaker modules. In practice, the modules of the same DCCB would be exposed to the similar environmental conditions and current stress, and therefore should experience similar levels of degradation.

Degradation of the surge arresters leads to a maximum transient interruption voltage (TIV) of 1.58 pu, which is higher than 1.47 pu in the case without considering the inaccuracies (Fig. 10 (c)). Uneven ageing of the surge arresters also leads to a 30% higher counter-voltage and 17% higher energy absorption of MB module 1 compared to other modules (Fig. 16 (d), (e)). The proposed algorithm is still able to detect a single-module failure with a sufficient margin when considering uneven ageing of the energy absorption surge arresters.

VI. Conclusion

This paper proposes backup protection based on a fast breaker failure detection algorithm, suitable for both complete and partial failures of DCCBs with a modular structure. The proposed algorithm is based on estimating the counter-voltage across the energy absorption branch during fault interruption. Since a parallel energy absorption branch is universally used in existing DCCB technologies to create the necessary counter-voltage to drive the fault current to zero, the proposed algorithm is generally applicable. The simulation results show that the proposed algorithm is able to quickly detect both complete and partial failures caused by various component failures of two common DCCB technologies, with a sufficient margin even considering measurement errors, noise and ageing of surge arresters.

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