Effective reduction of interfacial traps in Al₂O₃/GaAs (001) gate stacks using surface engineering and thermal annealing

Y. C. Chang,^{1,2} C. Merckling,^{3,a)} J. Penaud,⁴ C. Y. Lu,² W.-E. Wang,³ J. Dekoster,³ M. Meuris,³ M. Caymax,³ M. Heyns,^{2,3} J. Kwo,^{5,6,a)} and M. Hong^{1,a)}

¹Department of Materials Science and Engineering, National Tsing Hua University, 30013 Hsinchu, Taiwan

²Katholieke Universiteit Leuven, B-3001 Leuven, Belgium

³Interuniversity Microelectronics Center (IMEC vzw), 3001 Leuven, Belgium

⁴Riber, F-95873 Bezons, France

⁵Center for Condensed Matter Sciences, National Taiwan University, 10617 Taipei, Taiwan

⁶Department of Physics, National Tsing Hua University, 30013 Hsinchu, Taiwan

(Received 2 July 2010; accepted 22 August 2010; published online 13 September 2010)

To effectively passivate the technologically important GaAs (001) surfaces, *in situ* deposition of Al₂O₃ was carried out with molecular beam epitaxy. The impacts of initial GaAs surface reconstruction and post-deposition annealing have been systematically investigated. The corresponding interfacial state density (D_{it}) were derived by applying the conductance method at 25 and 150 °C on both *p*-type and *n*-type GaAs metal-oxide-semiconductor capacitors to establish the D_{it} spectra in proximity of the critical midgap region. We show that significant reduction of D_{it} near the midgap is achieved by applying an optimized thermal annealing on samples grown on a Ga-rich (4×6) reconstructed surface. © 2010 American Institute of Physics. [doi:10.1063/1.3488813]

The quest for technologies beyond the 15 nm node complementary metal-oxide-semiconductor (CMOS) devices has now called for research of high κ dielectrics on alternative channel materials such as Ge and III-V compound semiconductors with inherently higher carrier mobility than those of Si. Among the III-V's and the related MOS devices, GaAs nMOS has received intensive efforts in the past decades,^{1,2} owing to GaAs's superior bulk electron mobility (8500 cm²/V s) and its lattice parameter (5.65 Å) nearly identical to that of Ge. Direct oxidation of GaAs surfaces using thermal, anodic, and plasma methods have failed to produce an insulator-GaAs heterointerface with a meaningful measure of interfacial state density (D_{it}).¹

Reducing the high D_{it} 's on oxide/GaAs, particularly those near the GaAs midgap region, is an important issue for realizing GaAs MOS field-effect-transistors (MOSFETs) with surface inversion.^{3,4} The oxide/GaAs interface with low D_{it} was not achieved until the discovery of direct deposition of high κ oxides such as Ga₂O₃(Gd₂O₃) [GGO] and Gd₂O₃ on GaAs in the 1990s.^{5,6} However, unlike GGO, most other high- κ dielectrics on GaAs exhibit high D_{it} values at the GaAs midgap region,⁷ resulting in serious Fermi-level pinning, and thus preventing a proper inversion response required for the inversion-channel GaAs MOS devices. Sulfur passivation^{8–10} and/or insertion of interfacial passivation layer of Si or Ge (Refs. 11–13) on GaAs may have decreased D_{it} values in regions away from the midgap, but fail to effectively reduce the high midgap D_{it} peak.

Moreover, the initial GaAs surface reconstructions for GaAs MOS devices have also been investigated, and shown to have limited success.^{14–17} Among them, the dielectric/GaAs interfaces started with a variety of GaAs surface reconstructions have been studied by x-ray photoelectron spec-

troscopy (XPS) and photoluminescence (PL).^{15–17} However, there are few reports to correlate electrical properties and their corresponding D_{it} spectra of GaAs MOS devices with surface reconstruction of the starting GaAs substrate, prior to high κ oxide deposition. Furthermore, most of the electrical characteristics were studied using conventional capacitance-voltage (C-V) and conductance-voltage (G-V) characteristics measured at room temperatures. Due to a larger energy band gap of GaAs compared to that of Si, interfacial traps of the dielectric/GaAs interfaces near the midgap are too slow to respond to the usual C-V and G-V characterization frequencies (100 Hz–1 MHz) at room temperatures; consequently, only a small portion of D_{it} spectrum away from the midgap region has been measured.¹⁸

In this work, this inadequacy is remedied by performing additional C-V and G-V measurements at a high temperature of 150 °C to probe D_{it} spectrums around the midgap region. The D_{it} distribution as a function of the energy above valence-band maximum (E_v) has been derived by C-V and G-V measurements at 25 and 150 °C on both *n*-type and *p*-type GaAs MOS capacitors (MOSCAPs) with the gate dielectric Al₂O₃ deposited using molecular beam epitaxy (MBE). Furthermore, the influence on the D_{it} of the Al₂O₃/GaAs interfaces with the GaAs initial surface reconstructions and the systematic postannealing conditions is reported. We found that post annealing at 550 °C for 60 min and 650 °C for 30 s on samples grown on a Ga-rich (4×6) reconstructed surface have led to significant reduction of D_{it} near the midgap.

The growth of GaAs epilayers was carried out in a 200 mm Riber III-V MBE chamber. Reflection high-energy electron diffraction (RHEED) was used to monitor the growth, and to examine the GaAs surface reconstructions prior to the oxide growth. Three different surface reconstructions of GaAs (001) were studied: the As-rich (2×4) surface, the As-covered (100%) c(4×4) surface, and the Ga-rich (4×6) surface. Here we report only the latter two

^{a)} Authors to whom correspondence should be addressed. Electronic addresses: raynien@ntu.edu.tw, mercklin@imec.be, and mhong@mx.nthu.edu.tw.

FIG. 1. (Color online) C-V measurements on Ni/Al₂O₃(9 nm)/*p*-type GaAs MOSCAPs with Ga-rich GaAs reconstructed surface: (I) C-V curves measured at 25 °C, and (II) C-V curves measured at 150 °C.

reconstructed surfaces, which correspond to the highest arsenic and gallium surface coverage, respectively. The 0.3 μm thick GaAs buffer layers were grown at 580 °C under As-rich conditions with $P(\text{As})=1.8 \times 10^{-5}$ Torr. The substrate temperature was cooled down below 350 °C under As overpressure, leading to a $c(4 \times 4)$ reconstructed, As-covered surface. The samples were subsequently *in situ* transferred to an oxide molecular beam deposition chamber and heated up in UHV to 580 °C for 5 min to form the Ga-rich (4×6) surface reconstruction. Al₂O₃ films 9 nm thick were deposited by evaporating aluminum from an effusion cell under an atomic oxygen flux of $P(\text{O}) \sim 3 \times 10^{-6}$ Torr using a plasma source. During the oxide deposition, the substrate temperature was kept ~ 250 °C. The samples were postannealed to optimize the oxide and interface quality under nitrogen ambience at various temperatures and dwelling durations. After the annealing, Ni metal gate was deposited through a shadow mask. Ohmic contacts to the back side of the substrates of the *p*-type and *n*-type GaAs were made through the deposition of AuZn/Au and AuGe/Ni/Au multi-layers, respectively. C-V and G-V characteristics of these MOSCAPs were measured by using Agilent 4284 A. The corresponding D_{it} 's of these MOSCAPs were calculated by the conductance method.¹⁹

C-V characteristics of Al₂O₃/*p*-type GaAs MOSCAPs (with a Ga-rich surface reconstruction) annealed under various conditions have been summarized in Fig. 1: (a) annealing at 550 °C for 20 min, (b) at 550 °C for 60 min, (c) 550 °C for 60 min followed by 650 °C for 30 s, (d) 550 °C for 60 min followed by 650 °C for 20 min, and (e) 550 °C for 60 min followed by 750 °C for 30 s. All the C-V curves denoted as (I) were measured at 25 °C, and are well behaved with almost identical characteristics for various annealing conditions. This is because only a small range of interfacial traps with energies of 0.3–0.5 eV lying above the valence band edge (E_v) (Ref. 18) in these samples was probed at 25 °C and the measured D_{it} 's are nearly the same of $\sim \text{low } 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$ in this narrow region. In contrast, C-V measurements denoted as (II) were performed at 150 °C, probing the interfacial traps covering the midgap region. Pronounced trap-induced capacitance responses, manifested as the “hump” located in the depletion region, were observed at the low frequencies, consistent with those reported previously.^{8,12,17}

As shown in Fig. 1(II), annealing condition (b) and (c) show much smaller humps than those of (a), (d), and (e), indicating an improved interfacial quality. These results reveal that the long-time annealing at a medium temperature of 550 °C helps to reduce the hump [Figs. 1(a) and 1(b)], and

the annealing at 550 °C for 60 min followed by 650 °C for 30 s [Fig. 1(c)] is the optimized annealing condition responsible for the lowest values of D_{it} [Fig. 3(a)] and the smallest frequency dispersion in depletion. The heat treatments of a prolonged duration at 650 °C and/or at higher annealing temperature, such as 650 °C for 20 min [Fig. 1(d)] or

FIG. 2. (Color online) C-V curves of GaAs MOSCAPs started with Ga-rich surface on (a) *p*-type and (b) *n*-type substrates, and started with As-covered surface on (c) *p*-type and (d) *n*-type substrates.

FIG. 3. (Color online) (a) Comparison of D_{it} on various annealing temperatures and dwelling durations, and (b) D_{it} distribution as a function of the energy above E_v for GaAs MOSCAPs prepared on the Ga-rich and As-covered surfaces.

750 °C [Fig. 1(e)], tend to deteriorate the interfacial quality. Recent XPS study on the $\text{Al}_2\text{O}_3/\text{GaAs}$ interface revealed the interdiffusion of Ga into Al_2O_3 at elevated temperatures over 750 °C. Nevertheless, all the $\text{Al}_2\text{O}_3/\text{GaAs}$ MOSCAPs demonstrated low gate leakage current densities at V_{fb} -1 V under various annealing conditions (not shown here), which are lower than 10^{-7} A/cm^2 and 10^{-6} A/cm^2 , measured at 25 °C and 150 °C, respectively, suggesting that the good insulating property of Al_2O_3 is still maintained.

Figure 2 shows the C-V characteristics of MOSCAPs of Ga-rich and As-covered samples of both *p*-type and *n*-type, treated with the optimized annealing condition described above. As expected, all the corresponding C-V results at 25 °C show negligible differences. The C-V and G-V taken at 25 °C fail to detect notable D_{it} changes for the reasons given above. However, the C-V at 150 °C of the samples with a $c(4 \times 4)$ reconstructed, As-covered surface show larger humps measured for both *p*-type [Fig. 2(c)] and *n*-type substrates [Fig. 2(d)], giving substantially higher D_{it} near the midgap by nearly one order of magnitude than the samples on the Ga-rich surface.

Systematic post anneals of MOSCAPs grown on the As-covered GaAs surface of $c(4 \times 4)$ reconstruction led to only slightly reduction of D_{it} shown in Fig. 3(a). The post annealing process optimized for the Ga-rich surface appears to be rather ineffective to improve the interfacial quality of the samples with As-covered. The D_{it} near the midgap still exceeds $10^{13} \text{ eV}^{-1} \text{cm}^{-2}$ for the As-covered sample. In contrast, a significant reduction of D_{it} to $\sim 2 \times 10^{12} \text{ eV}^{-1} \text{cm}^{-2}$ near the midgap region ($E - E_v = 0.7 \text{ eV}$) is clearly demonstrated on Ga-rich samples after the optimized anneal. Extracted from corresponding G-Vs at various temperatures, the D_{it} spectra of $\text{Al}_2\text{O}_3/\text{GaAs}$ gate stacks grown on the Ga-rich and the As-covered surfaces are plotted in Fig. 3(b), showing

a peak value of low 10^{12} , and $10^{13} \text{ eV}^{-1} \text{cm}^{-2}$, respectively, in sharp contrast to a “U” shaped D_{it} for SiO_2/Si with a mean value in low $10^{10} \text{ eV}^{-1} \text{cm}^{-2}$.

In summary, a significant reduction of the midgap peak in D_{it} has been demonstrated for the first time in $\text{Al}_2\text{O}_3/\text{GaAs}$ MOSCAPs by employing *in situ* MBE oxide growth on a Ga-rich (4×6) reconstructed GaAs (001) surface as opposed to the As-covered $c(4 \times 4)$ reconstructed surface, followed by an optimized thermal annealing at 550 °C for 60 min and 650 °C for 30 s. Furthermore, C-V and G-V measurements conducted at elevated temperatures at 150 °C provided the essential assessment of the interfacial quality near the critical midgap region. The low D_{it} at midgap region indicates the optimized GaAs MOS structures will show proper inversion response, which may lead to high-performance inversion-channel GaAs MOSFETs.

The authors wish to thank the National Science Council, Taiwan, under Grant Nos. NSC98-2120-M-007-002 and NSC97-2120-M-007-008 for supporting this work. We would also like to acknowledge the support from Intel.

¹Physics and Chemistry of III-V Compound Semiconductor Interfaces, edited by C. W. Wilmsen (Plenum, New York, 1985).

²M. W. Hong, J. R. Kwo, P. C. Tsai, Y. C. Chang, M. L. Huang, C. P. Chen, and T. D. Lin, *Jpn. J. Appl. Phys., Part 1* **46**, 3167 (2007).

³F. Ren, M. Hong, W. S. Hobson, J. M. Kuo, J. R. Lothian, J. P. Mannaerts, J. Kwo, S. N. G. Chu, Y. K. Chen, and A. Y. Cho, *Solid-State Electron.* **41**, 1751 (1997).

⁴Y. C. Wang, M. Hong, J. M. Kuo, J. P. Mannaerts, J. Kwo, H. S. Tsai, J. J. Krajewski, J. S. Weiner, Y. K. Chen, and A. Y. Cho, *Compound Semiconductor Surface Passivation and Novel Device Processing*, MRS Symposia Proceedings No. 573 (Materials Research Society, Pittsburgh, 1999), p. 219.

⁵M. Hong, J. P. Mannaerts, J. E. Bower, J. Kwo, M. Passlack, W.-Y. Hwang, and L. W. Tu, *J. Cryst. Growth* **175–176**, 422 (1997).

⁶M. Hong, J. Kwo, A. R. Kortan, J. P. Mannaerts, and A. M. Sergent, *Science* **283**, 1897 (1999).

⁷W. E. Spicer, P. W. Chye, P. R. Skeathm, C. Y. Su, and I. Lindau, *J. Vac. Sci. Technol.* **16**, 1422 (1979).

⁸G. Brammertz, H.-C. Lin, K. Martens, D. Mercier, S. Sioncke, A. Delabie, W. E. Wang, M. Caymax, M. Meuris, and M. Heyns, *Appl. Phys. Lett.* **93**, 183504 (2008).

⁹R. Suri, B. Lee, D. J. Lichtenwalner, N. Biswas, and V. Misra, *Appl. Phys. Lett.* **93**, 193504 (2008).

¹⁰N. Goel, P. Majhi, C. O. Chui, W. Tsai, D. Choi, and J. S. Harris, *Appl. Phys. Lett.* **89**, 163517 (2006).

¹¹S. J. Koester, E. W. Kiewra, Y. Sun, D. A. Neumayer, J. A. Ott, M. Copel, and D. K. Sadana, *Appl. Phys. Lett.* **89**, 042104 (2006).

¹²C. Marchiori, D. J. Webb, C. Rossel, M. Richter, M. Sousa, C. Gerl, R. Germann, C. Andersson, and J. Fompeyrine, *J. Appl. Phys.* **106**, 114112 (2009).

¹³C. Merckling, J. Penaud, F. Bellenger, D. Kohen, G. Brammertz, A. Alian, G. Pourtois, M. Scarrozza, M. Houssa, M. El-Kazzi, J. Dekoster, M. Caymax, M. Meuris, and M. Heyns, *CMOS Gate-Stack Scaling – Materials, Interfaces, and Reliability Implications*, MRS Symposia Proceedings No. 1155 (Materials Research Society, Pittsburgh, 2009), p. C06–07.

¹⁴D. J. Webb, J. Fompeyrine, S. Nakagawa, A. Dimoulas, C. Rossel, M. Sousa, R. Germann, S. F. Alvarado, J. P. Locquet, C. Marchiori, H. Siegwart, A. Callegari, E. Kiewra, Y. Sun, J. De Souza, and N. Hoffmann, *Microelectron. Eng.* **84**, 2142 (2007).

¹⁵T. Yasuda, N. Miyata, and A. Ohtake, *Appl. Surf. Sci.* **254**, 7565 (2008).

¹⁶N. Negoro, S. Ananthathanasarn, and H. Hasegawa, *J. Vac. Sci. Technol. B* **21**, 1945 (2003).

¹⁷C. L. Hinkle, M. Milojevic, B. Brennan, A. M. Sonnet, F. S. Aguirre-Tostado, G. J. Hughes, E. M. Vogel, and R. M. Wallace, *Appl. Phys. Lett.* **94**, 162101 (2009).

¹⁸G. Brammertz, K. Martens, S. Sioncke, A. Delabie, M. Caymax, M. Meuris, and M. Heyns, *Appl. Phys. Lett.* **91**, 133510 (2007).

¹⁹E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology* (Wiley, New York, 1981).