Ultralow equivalent oxide thickness obtained for thin amorphous LaAlO_3 layers grown on Si(001)

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Electron beam evaporation in a molecular beam epitaxy reactor was used to deposit, at 400 °C, amorphous LaAlO_3 high- κ oxide films on *p*-type Si(001). X-ray photoelectron spectroscopy and transmission electron microscopy showed that the interface with Si is free of SiO_2 or silicates. Electrical measurements performed on as-deposited samples reveal an equivalent oxide thickness as low as 5 Å for a film having a physical thickness of 41 Å, a leakage current of 5.6×10^{-2} A/cm² at $|V_g - V_{FB}| = 1$ V, and no flatband voltage shift. © 2007 American Institute of Physics. [DOI: 10.1063/1.2811956]

Continuous scaling of complementary metal-oxide-semiconductor (CMOS) devices requires scaling of the SiO_2 equivalent oxide thickness (EOT) of the gate dielectric. To limit direct tunneling through ultrathin oxides, high- κ gate dielectrics are replacing SiO_2 and SiON as gate dielectrics for technology nodes beyond 45 nm. Up to now, hafnium based high- κ dielectrics such as HfO_2 , HfON , and HfSiON appear to be among the leading candidates for the integration in 45 and 32 nm CMOS technology, despite some remaining problems such as mobility degradation, charge trapping, and thermal stability. Some of these problems are solved by keeping an interfacial SiO_2 or silicate thin layer between the silicon substrate and the high- κ dielectric. However, this could prevent achieving the very low EOTs, below 0.7 nm, needed for sub-22-nm technology nodes. Thus, there is a need to explore alternative high- κ dielectrics, stable at high temperature on silicon, which could be prepared with abrupt interfaces. LaAlO_3 (LAO) is identified as one of the most promising candidates for future technology nodes.¹ This oxide is stable in air and thermally stable on silicon up to 1000 °C.^{2,3} It has a high band gap of 5.6 eV and a large conduction band offset of 1.8 eV with respect to Si.⁴ In the bulk crystalline phase, its dielectric constant is 25.³

Theoretically, epitaxial oxides with coherent interfaces would be ideal since they are free of interfacial layers and should lead to bulk dielectric properties. In fact, LAO was

unable to be epitaxied on silicon due to its high epitaxial growth temperature.^{4–6} Up to now, only a few oxides such as Al_2O_3 , Pr_2O_3 , and Gd_2O_3 have been epitaxially grown coherently on Si by molecular beam epitaxy (MBE) but these oxides suffer from some intrinsic limitations and do not meet all the roadmap criteria. An alternative approach would be to keep the oxide amorphous (LAO is known to remain amorphous up to 860 °C) without producing an interfacial layer during deposition or postdeposition annealing (PDA). Amorphous LAO films have been explored using various physical or chemical deposition techniques. The properties of the films reported in the literature were found to be highly dependent on the deposition techniques and on the growth conditions.^{7,8} The results are often contradictory with EOTs higher than 1 nm. Only Suzuki *et al.* reported a 0.31 nm EOT for films prepared using a laser sputtering method.⁹

In this letter, we report on the dielectric properties of amorphous LAO films grown on *p*-type Si(001) in a MBE reactor using reactive electron beam evaporation from a LAO single crystal target. This technique allows producing high quality stoichiometric epitaxial films on oxide substrates^{6,10} and gives better electrical properties than the usual evaporation of Al and La elements in oxygen ambient.⁸ The physical properties of the films were measured using x-ray photoelectron spectroscopy (XPS) and transmission electron microscopy (TEM). The electrical characteristics were determined by capacitance-voltage and current density–voltage measurements.

The sample considered in the following has been grown on *p*-type Si(001) substrate (doping concentration of $\sim 1 \times 10^{16}$ cm⁻³) in an ultrahigh vacuum reactor Riber 2300

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FIG. 1. [(a) and (b)] RHEED patterns along the $[110]_{\text{Si}}$ and $[100]_{\text{Si}}$ azimuths of the reconstructed 2×1 Si(001) surface before LAO growth, respectively. (c) TEM image of the sample showing that there is no amorphous interfacial layer between the amorphous 41 Å thick LAO high- κ oxide and the Si substrate.

with a base pressure of 8×10^{-10} Torr. It is representative of our technology process. Bulk LAO was evaporated using an electron beam gun. Before loading, the Si substrate was first cleaned in a $\text{HF}:\text{H}_2\text{O}$ (1:10) solution, then chemically oxidized in a $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$ (2:1) solution, and finally etched in NH_4F (40%). This procedure leads to the formation of an atomically flat H-terminated-Si(1 $\times$ 1) surface. The growth was followed *in situ* by reflection high-energy electron diffraction (RHEED) monitoring using a 30 kV RHEED system. Heating the sample to temperatures above 500 °C results in a sharp 2×1 RHEED pattern for Si(001) with Kikuchi lines [Figs. 1(a) and 1(b)]. Then amorphous LAO deposition was achieved. The LAO growth temperature was chosen sufficiently high at 400 °C in order to favor strong chemical bonding at the interface and within the oxide layer. Higher temperatures could favor silicate formation.⁶ The key point in the process was to manage the oxygen pressure during the deposition process to prevent the formation of SiO_2 or silicate at the interface while minimizing oxygen vacancies in the oxide, in order to ensure good dielectric properties. This was done by raising progressively, during growth, the molecular oxygen pressure up to 2×10^{-6} Torr. In order to evaluate the real potential of the deposition technique the samples were investigated as deposited. No usual PDA was carried out to improve the electrical quality of the heterostructures. To investigate the electrical properties of the sample, MOS capacitors were fabricated by a lift-off technique with evaporation of Ni (3 nm)/Au (300 nm) metal electrodes on the LAO layer to produce $95 \times 95 \mu\text{m}^2$ squares. The back side Ohmic contact was made using silver bonding. A probe station with an HP4284 A and an HP4156 B was used to obtain C - V and I - V curves, respectively, at room temperature.

The thickness of the LAO film was estimated to be equal to 41 ± 3 Å by TEM analyses, as shown in Fig. 1(c). Figure 2(a) presents the Si 2s core level of an amorphous LAO structure recorded at normal angle detection. The sharp peak at 151.1 eV is attributed to the Si 2s component of the silicon substrate. No SiO_2 or silicate is visible at the interface. Only a weak component is attributed to the interfacial Si atoms bonded with the oxygen network of LAO. More-

FIG. 2. XPS spectra of a 41 Å thick amorphous LAO layer deposited directly on Si(001) substrate: (a) Si 2s, (b) Al 2p, (c) La 3d, (d) La 4d, and Si 2p core levels. The La 3d and La 4d core level spectra of a crystalline LAO reference are also represented. The interface is free of SiO_2 or silicates.

over, Figs. 2(c) and 2(d) show the XPS spectra of the La $3d_{5/2}$ and La $4d$ core levels of the LAO/Si(001) heterostructure compared to those of a reference sample of crystalline LAO. The La $4d_{5/2}/\text{La } 4d_{3/2}$ and La $3d_{5/2}/\text{multiplet splitting satellite}$ ratios, respectively equal to 1.07 and 1.29, are similar for both samples. This is another indication of the absence of SiO_2 or silicates in the Si 2p components¹¹ and confirms that the chemical properties of the as-deposited thin LAO films are comparable to those of the LAO reference. Finally, there is no aluminum suboxide component detected in the Al 2p core level spectrum centered at 75.1 eV, proving that the oxygen pressure was high enough to fully oxidize the Al and La species [Fig. 2(b)].

Figure 3(a) shows the typical experimental C - V curves obtained at 1 MHz on the same sample. The measured oxide capacitance is 300 pF, leading to a capacitive equivalent thickness (CET) of 10 Å. For such a low CET value, quantum effects due to the depletion layer in the silicon substrate are no more negligible and CET overestimates EOT by several angstroms. The EOT was therefore extracted by fitting the experimental C - V data with realistic quantum simulations.^{12,13} To fit the C - V curves shown in Fig. 3(a), a work function of 4.5 eV for the Ni metal gate, a 7 Å EOT ($\kappa_{\text{LAO}}=22.8$) without any charge, and D_{it} were taken. In such a material system, the theoretical flatband voltage is equal to -0.5 V, which corresponds to the experimental value. The high quality of the fit means that the density of interface states and the density of localized charges in the oxide layer are relatively low. At $|V_g - V_{\text{FB}}|=1$ V [Fig. 3(b)], the leakage current through the structure presents a value of 9.3×10^{-2} A/cm² which meets the requirements of the ITRS roadmap¹ for such low EOT value. This result is compared with a I - V simulation^{12,13} showing that a 7 Å thick SiO_2 layer on silicon gives a leakage current of 1.8×10^2 A/cm², much larger than the one obtained from our sample. Note that the C - V and I - V curves depicted in Figs. 3(a) and 3(b) were measured on the same capacitor. Most of the measured capacitors (around 30) displayed the same 7 Å EOT values. However, we found on the same wafer some capacitors with lower EOT values. Our best C - V and I - V results are shown in Fig. 3(c). A 7.8 Å CET was extracted $C_{\text{ox}}=396$ pF. Assuming a quantum mechanical correction of 3 Å, an EOT smaller than 5 Å is obtained [confirmed by simulation with a SiO_2 layer in Fig. 3(c)]. However, we were not able to fit perfectly the C - V curve, without introducing interface states, as was

FIG. 3. (Color online) (a) Typical C - V curves obtained at 1 MHz for a 41 Å thick LAO/Si MOS sample ($\kappa_{\text{LAO}}=22.8$). A simulation of a 7 Å thick SiO_2 /Si MOS sample without any charge in the dielectric matches up to the experimental curve. (b) J - V measurement done on this 41 Å thick amorphous LAO layer (EOT=7 Å) and comparison with a simulation (for $V_g < 0$ V only) of a 7 Å thick SiO_2 layer. For the same EOT value, the leakage current of our LAO layer is lower than the one observed with a simulated SiO_2 layer. (c) Best C - V at 1 MHz ($\kappa_{\text{LAO}}=32$) and I - V measurements found on the amorphous LAO film deposited directly on p -type Si(001) substrate at 400 °C. The C - V simulation fit was realized with a SiO_2 layer with a thickness of 5 Å and without charge or D_{it} .

done above for the 7 Å EOT curves. This 5 Å value is relatively close to the 3 Å record value reported by Suzuki *et al.*⁹ We extracted a dielectric constant of 32, higher to the bulk LAO dielectric constant. The minimum leakage current acquired at $|V_g - V_{\text{FB}}|=1$ V is 5.6×10^{-2} A/cm². The origin of these variations is not clear to us. It seems that locally we may find on the wafer some areas with better dielectric properties than on the average.

The good dielectric quality of our as-grown layers can be attributed to the reactive evaporation deposition technique. First, LAO was prepared by congruent evaporation of LAO single crystals which assures a good La/Al stoichiometry

and favors the production of oxidized AlO_x and LaO_x species, thus minimizing oxygen vacancies. Second, the deposition is done at a relatively high temperature which favors strong chemical bonding at the interface and structural arrangement within the oxide layer. The dielectric constant of our LAO layer ranges from 22 to 32 which is in the order of the 25 bulk value. We speculate that the high- κ value of 32 could be associated with La rich areas and thickness fluctuations (thinner layer on some parts of the sample).

In summary, we have fabricated amorphous LaAlO_3 films on silicon with sharp interfaces using a MBE related growth technique. The as-grown layers are characterized by small EOTs and good leakage currents which meet the gate leakage criteria for high- κ gate stacks. Optimization of the deposition process should even give higher performances and lower EOTs. These results show that LaAlO_3 should still be considered among a few other materials as a promising candidate for the next CMOS technology generations. However, this does not preclude that other important criteria such as mobility will be met. This has to be quantified in further studies. Optimization of the electrical properties of the layers with PDA is currently in progress.

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