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Stacking Isolated SC Cores for High Voltage Wide Input Range Monolithic DC-DC Conversion

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Abstract—A fully integrated DC-DC converter that uses isolated switched capacitor cores in a stacked way, is presented. The converter can transform a wide input voltage range from 7.5 V up to 42 V by the multiple available VCRs, which are realized through reconfiguration of the stackable cores. Additionally, stacking simplifies the design to the low voltage isolated SC core. Level shifters are included to fulfill the high voltage interfaces while bulk biasing circuits ensure correct driving of the switches in the cores. As such, the power converter is implemented in a 0.35 μm CMOS technology and produces a stable 3V output with less than 5% voltage ripple for a peak output power of 2.1mW.

Index Terms—Fully integrated, DC-DC converter, switched capacitor, stacking, isolated converter, multi-ratio, high voltage.

I. INTRODUCTION

STACKED power conversion with isolated switched capacitor DC-DC converter cores, as presented by this work, is a technique that can serve as a solution for the required high voltage interfaces. In particular, a trend towards electronics operating at higher voltages appears in numerous industries, where a shift from 12 V towards 42 V and even 48 V takes place [1]. Moreover, many of our devices are powered by the AC-mains. In contrast, the internal circuits in many electronic devices operate at lower voltages (LV).

The voltage gap between the high input voltage and the lower internal voltages is typically bridged by power converters containing discrete components. These converters, however, are inefficient when powering mW-range applications or devices in standby mode [2]. A plugged-in mobile phone in standby, for instance, consumes about 5 mA [3]. Fulfilling this low power demand through the bulky discrete converters to keep the fully charged state, results in a large energy waste.

From this perspective, interest rises for monolithic converters interfacing the high voltages (HV) that are optimal for battery [4] or AC-mains [5] powered applications in their low power standby mode. Due to their small size, these converters fit next to the existing watt-range converters for cooperation. In this regard, fully integrated converters transforming the AC-mains are proposed in [5]–[7]. Here, a capacitive voltage division of the high input voltage realizes the interface between the AC-mains and the low on-chip voltages. The capacitive approach, however, confines the power throughput due to the high input impedance formed by the input capacitor. As such, the power density of the converter is limited. The resistive approach from [8] can increase the power density, although the conversion efficiency ($\sim 2\text{--}3\%$) is very low in this case.

On the other hand, switched capacitor (SC) DC-DC converters have proven to be perfectly fit for integration in standard CMOS technologies while realizing a good performance.

Therefore, the idea rises to solve the addressed problems with SC converters. This idea is supported by the ‘universal converter’ proposed in [9]. Since the efficiency of one topology realizing one voltage conversion ratios (VCR) is limited to $V_{\text{OUT}}/(V_{\text{IN}} \cdot \text{VCR})$, the proposed solution needs an SC converter with multiple VCRs. Here, the VCR defines the ideal ratio between the output and input voltage, while V_{OUT} and V_{IN} are the actual converted voltages. This converter with multiple ratios, which is able to convert a wide range of input voltages, should also be able to interface with high voltages.

In general, such a gearbox or recursive SC converter that realizes numerous ratios and also handles large input voltages, is challenging. For instance, [10] presents a 254-ratio converter that can only handle inputs up to 4 V. Furthermore, [8] reports the highest input voltage of 17 V but realizes only one ratio.

In a first step to realize a monolithic SC based HV wide input range converter for mW-range applications, this work presents a stacked SC DC-DC converter handling voltages up to 42 V. The proposed technique is based on connecting multiple basic converters in a stacked configuration. This realizes the high voltage capability, while stack-reconfiguration enables wide range operation. The technique also holds a strong design advantage. After all, only the optimization of a basic converter with fewer ratios and a low input voltage can be considered.

This paper is an extension of the work presented in [11] and contains more information on the design, implementation and results of the stacked converter. Section II explains the concept of stacked power conversion in more detail and adds a discussion on the design parameters. Section III introduces the power combiners and the isolated switched capacitor converters that allow the use of SC-techniques. A detailed discussion of the main building block of the proposed design, the isolated SC converter, follows in section IV. In addition to [11], a design strategy for the isolated core is presented. Sections V and VI discuss the circuit details of the drivers and controllers including the input configuration block. Finally, section VII contains an extended discussion of the measurement results.

II. STACKED POWER CONVERSION

A. Stacked Converter for High Input Voltages

Stacking DC-DC power converters allows transformation of high DC-voltages into low DC-voltages with a large design advantage. The concept of stacking power converters is shown in Fig. 1. Here, N identical basic converters (BCs) are used. The BCs’ inputs are connected in series and their outputs are connected in parallel to the converter output V_{OUT} . Since all BCs are identical, the input impedance of the converter is

Fig. 1: Concept of stacked power conversion.

a serialization of N identical impedances, so that the input voltage V_{IN} divides equally across the BCs into $V_{IN,i}$ (1). Furthermore, since all converters have the same operating point, the output current of all converters ($I_{OUT,i}$) is identical. At the output, the currents of the BCs are summed (2). Similarly, the output power of the stacked converter (P_{OUT}) equals N times the output power of a basic converter ($P_{OUT,i}$).

$$V_{IN,i} = V_{IN}/N \quad (1)$$

$$I_{OUT} = \sum_{i=1}^N I_{OUT,i} = N \cdot I_{OUT,i} \quad (2)$$

Each of the stacked converters has a voltage conversion ratio (VCR) of $M:1$, meaning:

$$\frac{V_{IN,i}}{V_{OUT}} = M \quad (3)$$

Hence, the VCR of the full converter in Fig. 1 equals $(M \cdot N):1$. As a result, the stacked converter can handle voltages that are N times higher than the input voltages of the BCs.

$$\eta_{STACK} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot I_{IN}} = \frac{V_{OUT} \cdot (N \cdot I_{OUT,i})}{(N \cdot V_{IN,i}) \cdot I_{IN}} = \eta_i \quad (4)$$

Stacking, as shown in Fig. 1, holds 2 main advantages. First, (4) shows that the efficiency of the stacked converter η_{STACK} equals the efficiency of the basic converters η_i . This means that a converter with a high VCR ($M \cdot N$), which is generally less efficient than its lower VCR counterparts, can be realized at the higher efficiency of the low VCR (M) converters. Second, only the design of the low VCR core should be considered while stacking automatically allows the down conversion of a much higher input voltage. This results in a strong design advantage: only the single core should be designed while the stacked converter achieves the same performance, delivers N times more power and faces an N times higher voltage.

B. Stacked Converter for Wide Operation Range

Moreover, the advantages of stacking are not only limited to high voltage conversion, since stacking also enables wide input range voltage conversion. The efficiency of a stacked converter built with switched capacitor cores can, for the ideal case, be represented by one of the colored curves in Fig. 2.

For evaluation of the ideal case, each basic converter is replaced by the model in Fig. 3 with $R_{P,M} = \infty$. Here, $R_{OUT,M}$ models the losses set by the load current and that are intrinsic

Fig. 2: Ideal efficiency vs. V_{IN} for stacked power conversion.

Fig. 3: Model of switched capacitor basic converter [12].

to the topology. $R_{P,M}$ represents the shunt losses caused by switching the parasitic bottom plate (BP) capacitors and driving the switches. The efficiency is evaluated by equations (5)-(7), where R_{LOAD} represents the load impedance.

$$R_{OUT,M} = \frac{\frac{V_{IN}}{N \cdot M} - V_{OUT}}{I_{OUT,i}} \quad (5)$$

$$R_{LOAD} = \frac{V_{OUT}}{I_{OUT}} \quad (6)$$

$$\eta_{ideal} = \frac{N \cdot R_{LOAD}}{N \cdot R_{LOAD} + R_{OUT,M}} \quad (7)$$

Each VCR results in a unique efficiency curve in Fig. 2. Considering one such fixed VCR, the converter is efficient for a limited input voltage range ($\sim M \cdot N \cdot V_{OUT}$). Neither it can convert low voltages nor it is efficient for the higher voltages, as shown by the decreasing curves. In gearbox converters, the black curve with the high average efficiency is reached through implementation of multiple VCRs inside the converter. In this case, the converter will change its mode and operate in its most efficient VCR depending on the value of the input voltage. Similarly, by introducing multi-ratio stacked converters, the input operation range can be further optimized in two ways.

First, it is possible to implement multiple ratios inside the basic converters. This allows to change M and to deviate between the efficiency lines of the same color in Fig. 2. Second, it is possible to change the input connections of the BCs by the input configuration block (ICB) in Fig. 4a. This concept changes the number of converters that are connected in series or in parallel at their inputs and is called stack reconfiguration. Figure 4b gives an example of the proposed reconfiguration with 4 basic converters. Connecting all BCs in parallel realizes the ratio $M:1$, while the configuration with 2 stacked blocks at the bottom realizes a $2M:1$ ratio and the full stack $4M:1$. In general, the ratios $k \cdot M$ ($k \in [1, N]$; $k \in \mathbb{N}$) can be realized. During reconfiguration, the efficiency of the converter remains the one of the basic converters (4), explaining the repeating curves in different colors in Fig. 2.

Fig. 4: Stacked converter for wide input range.

C. Design Constraints for Stacked Converters

During the design of a stacked power converter, the following parameters should be determined:

$$N = \text{Total \# basic converters} \quad (8)$$

$$M_M = \text{Maximum VCR in each BC} \quad (9)$$

$$M_i = \text{VCR}_i \text{ in each BC} \quad (10)$$

$$S = \# \text{ stacked blocks} \quad (11)$$

$$P = \# \text{ parallel converters in each stacked block} \quad (12)$$

Here, N mainly depends on M_M and the maximum input voltage that must be handled. In the example of Fig. 4b, the values of S and P are 1 and 4 for the converter at the top, while both S and P equal 2 for the bottom configuration.

$$S \cdot P \leq N \quad (13)$$

When the input voltage changes, the converter stack can be adapted to any form as long as S and P are natural numbers fulfilling (13). Nevertheless, it is preferred to operate the stack with the SP -product equal to N . This constraint ensures an optimal use of the available BCs, as explained subsequently.

$$I_{OUT,i} = \frac{I_{OUT}}{S \cdot P} \quad (14)$$

$I_{OUT,i}$ in (14) represents the current delivered by the operational basic converters. I_{OUT} is the converter's total output current, which remains constant for all operating modes so that a constant output power can be delivered for all V_{IN} . When $S \cdot P < N$ (case 1), the $I_{OUT,i}$ are higher than when $S \cdot P$ equals N (case 2). This means that the BCs should be designed larger for case 1 than for case 2. Consequently, the BCs are oversized and not used at their full potential in case 2. Additionally, the stack cannot use all BCs in case 1, which leads to a lower power density in the stacked converter. To conclude, it is suggested keeping the SP -product equal to N in order to use all BCs to their full potential in all modes.

When choosing the M_i of the basic converter, it is important to keep track of the ratios realized when reconfiguring the stack in addition to the analysis of the internal design. Table I shows an example of the available conversion ratios in the stacked converter for different S , P and M . The table shows that it is not useful to add the $M_3 = 4$ ratio in the BCs since this would result in the same VCRs realized with $M_1 = 2$. Furthermore, the $M_3 = 4$ converter is generally less efficient so that the efficiency of the stacked converter would decrease.

TABLE I

Total voltage conversion ratio for different S , P and M .

S	P	$M_1 = 2$	$M_2 = 3$	$M_3 = 4$
1	4	2	3	4
2	2	4	6	8
4	1	8	12	16

The model in Fig. 3 can be used for the optimization of the design parameters. The power loss of a stacked converter with VCR equal to $(N \cdot M):1$ delivering I_{OUT} and that contains N basic converters with $M:1$ ratio can be evaluated as follows:

$$P_{LOSS} = N \cdot (R_{OUT,M} \cdot I_{OUT,i}^2 + \left(\frac{V_{IN}}{N \cdot M} \right)^2 \cdot \frac{1}{R_{P,M}}) \quad (15)$$

$$= \frac{R_{OUT,M}}{N} \cdot I_{OUT}^2 + \left(\frac{V_{IN}}{N \cdot M} \right)^2 \cdot N \cdot R_{P,M}^{-1} \quad (16)$$

The model accuracy depends on the included loss parameters. For example: consider a Dickson converter, a good candidate for HV designs, with $M:1$ ratio and equally sized capacitors and suppose that the total capacitance in the stacked converter equals C_{tot} . Including the capacitive switching losses and bottom plate losses, the impedances in the model become:

$$R_{OUT,M} = \frac{(M-1)^2}{M^2} \cdot \frac{N}{f_{sw} C_{tot}}, \quad R_{P,M}^{-1} = \frac{\alpha f_{sw} C_{tot}}{N} \quad (17)$$

Based on these equations, a converter with high N and low M is preferred. However, the discussed constraints and desired VCRs should also be taken into account, leading to trade-offs.

III. STACKING WITH SWITCHED CAPACITOR CONVERTERS

A. Problem with Switched Capacitor Converters

Switched capacitor converters form the perfect candidates to use in the stacked converter. They can be small, low cost, efficient, power dense and they are perfect for monolithic integration. The known SC converters, however, are not fit for direct integration in the proposed stacked converter since this will create shorts, as illustrated in Fig. 5.

The problem rises since standard SC converters share the ground terminal between the input and output port, shown by the blue dashed lines. For this reason, switched capacitor converters should be considered 3-terminal elements. As a result, both input terminals of the 2nd converter in Fig. 5 are connected to ground, making the 2nd converter useless while the 1st converter faces the full input voltage. This problem can be solved in two ways, as explained subsequently.

Fig. 5: Stacking standard SC converters results in shorts.

Fig. 6: Power combiners for stacked SC conversion.

B. Power Combiners as a Potential Solution

The shorts arising from stacking standard SC converters can be solved by adding a power combining block between the basic converters' outputs and the stacked converter's output. This power combiner transfers the power generated in the BCs to the output of the stacked converter while it shifts the outputs of the different BCs to the V_{OUT} -domain. The combiners can be realized by connecting one of the circuits in Fig. 6 to each of the N basic converters and connecting the N outputs in parallel to V_{OUT} . In Fig. 6, $OUT_{P,i}$ and $OUT_{N,i}$ form the output of the i^{th} BC and $(V_{OUT} - GND)$ is the stack output.

Combiner A in Fig. 6a stores the output energy of basic converter i generated in phase 1 (Φ_1) temporarily on $C_{C1,i}$ and transfers this energy to the output in phase 2 (Φ_2). The $C_{C2,i}$ are responsible for the energy generated in Φ_2 . Since the voltage across $C_{C1,i}$ and $C_{C2,i}$ is only V_{OUT} , these extra capacitors can be realized as dense MOS-capacitors and thereby limit the influence of the combiner on the power density of the stacked converter. Combiner A, however, strongly degrades the converter's efficiency due to the high bottom plate swing of $C_{C1,i}$ and $C_{C2,i}$, causing the large power loss shown in (18). Here, $P_{BP,A}$ is the BP power loss of the full combiner, α_{MOS} the percentage parasitic BP coupling of a MOS-capacitor and f_{sw} the switching frequency of the converter.

$$P_{BP,A} = 2 \cdot \alpha_{MOS} \cdot f_{sw} \cdot C_{C1} \cdot \sum_{i=1}^N ((i-1) \cdot M \cdot V_{OUT})^2 \quad (18)$$

Combiner B operates differently and as such, limits the BP swing of all extra capacitors to V_{OUT} , so that the power loss decreases. On the other hand, the extra capacitors face a high voltage of $i \cdot (M-1) \cdot V_{OUT}$, with $i=1..N$. Therefore, they should be implemented with a less dense capacitor structure, causing a drop in the power density of the stacked converter.

Additionally, analysis of the efficiency of the stacked converter including the combiner circuits by the theory in [12], reveals a severe efficiency drop. This drop results from the high contribution of the additional combiner capacitors in the slow switching limit impedance of the converter. This impedance is a measure for the losses created by charging and discharging the capacitors and is a good estimate for $R_{OUT,M}$ in Fig. 3 at low switching frequencies.

Investigation of other power combining topologies leads to the same conclusions. Although combiners form a straightforward way to solve the shorts in Fig. 5, they strongly decrease the efficiency and power density of the stacked converter.

Fig. 7: Charge balance of isolated SC converter with $M:1$ ratio.

C. Isolated Switched Capacitor Converters

To solve the previous problems, this work introduces isolated switched capacitor converters. These converters can directly be plugged into the stacked converter of Fig. 1. In the isolated SC converter, the input and output port are isolated so that a 4-terminal converter is obtained. This way, the dashed connections in Fig. 5 are removed, eliminating the shorts.

Compared to the previous solution using combiners, the isolated converters achieve a higher power density and efficiency. More specifically, less additional capacitors are needed to realize the isolated operation compared to the combining function, the bottom plate losses are lower and the charge transfer analysis [12] results in a better $R_{OUT,M}$. The following section gives more details about these isolated SC converters.

IV. ISOLATED SWITCHED CAPACITOR CONVERTERS

This section addresses the properties and the design of the isolated SC converters and introduces the implemented design. The circuit details are discussed in section V.

A. Design Considerations

As it is the case in standard SC converters, the VCR in isolated SC converters is determined by the way the capacitors are connected in the different phases. The isolated converters maintain the same operating principles as the standard designs and can also be analyzed through the theory in [12]. This work only considers 2-phase implementations, for which the core controller generates the phase signals in the V_{OUT} -domain.

The isolated operation imposes two additional design constraints to the SC converter. First, it is important to maintain the charge balance at the input and output port of the converter while the correct amount of charge flows in all terminals, as shown in Fig. 7. Here, $IN_{P,i}$ and $IN_{N,i}$ form the input port of the isolated converter that can be stacked and the output of the stacked converter is $V_{OUT} = OUT_P - OUT_N$. The absolute values of $IN_{P,i}$ and $IN_{N,i}$ depend on the position of the isolated converter in the stack. Second, the top and bottom terminal of each capacitor should be related to a voltage of either the input domain or the output domain in both phases.

Previous constraints are explained further by the design example of the 2:1 isolated SC core in Fig. 8. Isolated SC converters can be designed starting from their standard counterparts, as shown in Fig. 8a. As expected, the design constraints are not met. First, the charge balance is incorrect. Second, the top plate of C_1 is connected to a terminal related to the input domain in Φ_1 , while in Φ_2 it is connected to the output domain. As a consequence, the voltage across C_1 changes in both phases, and no stable operation is obtained.

Adding capacitor C_2 (Fig. 8b) solves both problems. In Φ_2 , C_1 transfers the charge that it received from the input in Φ_1

Fig. 8: Designing a 2:1 isolated switched capacitor converter.

to the output. In order to meet the voltage constraints, C_2 is added to bridge the voltage gap between the input and output port created at the top plate of C_1 , while delivering the correct amount of charge to the output. In Φ_1 , C_2 is used to meet the charge balance specification of terminal $IN_{N,i}$. As a result, Fig. 8b contains a valid 2:1 isolated SC converter.

In Fig. 8c, buffer capacitor C_B is added to the design. Adding C_B does not change the operation and the net charge balance of the converter, but realizes the stable DC-voltage $IN_{N,i} + V_{OUT}$. This allows easier driving of the converter's switches since the drivers can operate in a stable instead of a floating voltage domain (Sec. V-B). Generally, adding flying capacitors to an SC topology decreases the efficiency. Since the bottom and top plate voltages of C_B are fixed, C_B is a non-flying capacitor and does not negatively influence the efficiency. Implementing C_B as low voltage MOS-capacitor limits its influence on the power density of the stacked converter. To maintain the charge balance in both phases, 2 of the presented converters in Fig. 8c should be used with a phase shift of 180° . This is also advantageous for the stacked converter because the output voltage ripple decreases.

Implementation of a multi-ratio isolated SC converter, can be based on the same design principles. Here, the best approach is to reuse the available capacitors as much as possible in the different modes while changing just the phases in which the switches operate, as proposed in [13]. Accordingly, a design in which a capacitor has the same switching behavior in all modes is more efficient than a design in which the behavior of the converter changes severely during mode change.

B. Implemented Design

Taking into account the design constraints of the previous sections and the maximum input voltage to be handled, this work implements a stacked converter with 4 (N) basic converters, now implemented by the isolated SC core in Fig. 9. This

Fig. 9: Isolated switched capacitor converter core.

core has 3 modes by which a VCR of 3:1, 5:2 and 2:1 (M_i) can be realized. The isolated cores can be configured all in parallel ($S=1$, $P=4$), in a double stack of 2 cores ($S=2$, $P=2$) and all stacked ($S=4$, $P=1$). This way, the modes shown in table II can be realized and input voltages ranging from 7.5 V to 42 V can be converted into a 3 V output accordingly.

The configuration of the capacitors and the charge vectors of the isolated SC core in its different modes are shown in Fig. 10. The design of the 3:1 mode is based on the 3:1 Dickson converter, which explains the configuration of capacitors C_1 and C_2 . $C_3 = C_{3A}/C_{3B}$ realizes the voltage isolation as described in previous section, while C_B is again added to realize a stable DC-voltage. Addition of this capacitor also decreases the BP swing and BP loss of C_3 . By splitting C_3 in C_{3A} and C_{3B} and changing its position compared to the other capacitors in the converter, the other VCRs are realized.

Bottom plate losses are dominant in the proposed high voltage converter. In this regard, this work puts an extra design constraint on the BP swing of all capacitors and limits the maximum bottom plate swing to V_{OUT} . To limit the BP-losses even further, the charge recycling technique from [14] is applied to C_1 and C_2 . As a result, each basic converter in the stack consists of 8 phase shifted cores from Fig. 9.

The most efficient and power dense solution is achieved by implementing the capacitors as follows. C_1 (7.3 pF) and C_2 (2×6.7 pF) are realized as high voltage MOM-capacitors. Here, the metal spacing is adapted to the applied voltages, which are $(IN_{P,i} - OUT_P)$ and $(IN_{N,i} - OUT_N)$ respectively. Since C_3 (13.1 pF) and C_B (6 pF) only face V_{OUT} , denser structures are

Fig. 10: Core configuration in different phases and modes.

TABLE II
Operating Modes of Stacked Power Converter

Stack-setting	All //	2x2 stacked	4 stacked
VCR	2:1, 5:2, 3:1	4:1, 5:1, 6:1	8:1, 10:1, 12:1
V_{IN} -range	7.5 V - 15 V	15 V - 30 V	30 V - 42 V*

* limited by technology, theoretically V_{IN} up to 60 V possible

used. C_B is implemented as p-type MOS-capacitor and for C_3 a MIM-structure is chosen. The latter decreases the BP-losses of C_3 compared to a MOS-capacitor implementation. The optimized converter counts a total core capacitance of 1.3 nF.

C. Comparison to Standard Designs

The presented design technique can be extended to other VCRs. The design optimization relaxes strongly in comparison to standard designs. Only one core with less capacitors, switches and VCRs needs to be considered, while the high conversion ratios are automatically achieved by stacking. The question rises if the stacked design outperforms the standard SC designs. This demands the evaluation of different parameters.

Regardless of the number of stacked converters, the efficiency of the stack will always be the efficiency of the BCs, which is not true for the standard designs. An extensive charge analysis of the Dickson topology including BP-losses indeed shows that the maximum efficiency drops with higher M :

$$\eta_{MAX} = 1 + 2\sqrt{\alpha} \frac{M-1}{M} + 2\alpha \frac{(M-1)^2}{M^2} + 2\alpha\sqrt{\alpha} \frac{(M-1)^3}{M^3} \quad (19)$$

Compared to, for instance a 12:1 Dickson converter, the stacked converter only needs one extra flying capacitor. Additionally, 3 HV capacitors from the standard design are replaced with LV capacitors in the stacked design and the switches in the isolated core face lower voltages. This limits the area and efficiency penalty of the isolated core due to the added capacitor while granting access to the advantages of stacking.

Nevertheless, a full comparison between standard SC designs and the presented converter achieving the same VCR demands for a full design of both converters allowing the estimation of all loss components, which is beyond the scope of this paper. It should also be noticed that the answer to the stated question strongly depends on the implemented topology.

V. CONVERTER IMPLEMENTATION DETAILS

The implemented converter contains 4 stackable basic converters. Each of these BCs consists of 8 isolated cores (Fig. 9), which enable a phase shifted operation for charge recycling and a reduced output voltage ripple. The proposed converter transforms a high input voltage and realizes multiple conversion ratios. As a result, specific circuit techniques, which will be discussed next, are applied to drive all switches in the isolated cores correctly.

By using the presented switch-driving techniques, all switching events take place in isolated 3V-domains. Thereby, the power consumed in the cores depends on neither the absolute voltages nor the BCs' position in the stack. As a result, the stacked converter can be expanded without increase in the drive power of the BCs.

Fig. 11: Capacitive level shifter with DC-level generation.

A. Level shifter

The switches in the isolated cores are implemented as a serialization of 2 MOS-transistors in order to sustain all applied voltages. Since a wide range of voltages is applied to the isolated converter (table II), the voltage across the switches exceeds the theoretically calculated value of V_{OUT} . As a result, the maximum operation voltage of one MOS-transistor is exceeded, which is why two transistors are needed. One of these transistors should be driven by a DC-voltage, the other by a phase signal generated by the core controller. Since this controller offers phase signals in the V_{OUT} -domain and the isolated cores operate in a higher voltage domain, the level shifter (LS) presented in Fig. 11a is added to drive the switches correctly. The proposed LS is a capacitive level shifter based on [15] but uses only 1 level shifting capacitor according to [16], leading to an area efficient solution.

The LS realizes 2 functions, illustrated by the signals in Fig. 11b. First, the LS shifts the phase signals of the controller (IN) to the higher voltage domain ($V_L - V_H$) by capacitive coupling through C_{LS} . Second, it generates either V_L or V_H , since only one of the voltages is available inside the isolated converter core. As long as the input (IN) switches frequently, the latch formed by the cross-coupled inverters sends charge to C_{DC} . After a short start-up time, as shown in Fig. 11b, this realizes a stable high voltage domain ΔV_H :

$$\Delta V_H = V_H - V_L = V_{OUT} - V_{DROP} \quad (20)$$

V_{DROP} depends on the ratio between the capacitance of C_{LS} and the capacitance that needs to be driven by the LS at the output (OUT) including the capacitance of the transistors in the cross-coupled inverters of the LS. The larger C_{LS} , the lower V_{DROP} but the larger the power consumption and the size of the level shifter. To conclude, a trade-off between the desired voltage domain size (ΔV_H), efficiency and cost of the level shifter emerges. In order to increase the voltage in the higher domain even more and to increase the speed of the drive signal OUT, the upper inverter of the LS should be sized smaller than the lower inverter. Although an 'asymmetric' circuit is presented, the output voltage of the LS has equal rise- and fall-time, as shown in Fig. 11b. This property depends on the relative sizing of the N- and PMOS transistors in the level shifter, not on the presence of an additional C_{LS} .

Fig. 12: Circuit details of converter core.

B. Stable DC-levels

The discussed level shifters can be used to drive the switches in the isolated cores if a stable DC-voltage is available to connect to either V_L or V_H and if one of the switches' terminals is related to the same voltage. A first DC-level, feeding the drivers of S_{3-5} and S_{7-8} , is available on C_B .

The circuit in Fig. 12a generates an other DC-level facilitating a driver with the above LS for S_2 . Fig. 12a shows switches S_2 of 2 isolated cores, from the same BC, operating with a phase shift of 180° . By splitting S_2 into 2 switches and connecting the phase shifted cores together as shown in Fig. 12a, a DC-voltage is created. Without this extra circuit, S_2 would be connected to 2 switching nodes unrelated to one of the available DC-levels, which demands a more complex bootstrap circuit.

C. Biasing the Transistor Bulk

A final important aspect of the switches in the stacked converter, is the voltage level connected to the bulk of the transistors. In order to avoid latch-up by forwarding parasitic diodes, the bulk of an NMOS/PMOS transistor should always be connected to the drain or source, depending on which terminal has the lowest/highest voltage. When the mode of the BC (M_i) changes during operation, the decision on which terminal that should be selected for the bulk of some transistors can change. To solve this problem, 2 transistors can be added to the transistors in question, as shown in Fig. 12b. Here, the extra transistors choose the lowest terminal (drain X or source Y) and connects it to the bulk of the switching transistor. A PMOS equivalent circuit can be added to the PMOS switches.

VI. CONTROL STRATEGY

The control loop in SC converters ensures a correct voltage conversion for all load conditions. In the presented design, the ICB and the core controller accomplish this function.

A. Core Controller (CC)

The core controller operates at the level of the basic converters. Nevertheless, one shared controller is sufficient for all BCs. The core controller is responsible for the correct core mode. The main function of the CC, however, is to change the switching frequency f_{sw} of the isolated cores according to the load conditions so that a stable 3 V output can be maintained. The CC operates in the output voltage domain and generates 8 non-overlapping clock signals that drive the 8 phase shifted cores. The controller also generates 20 charge recycle signals

Fig. 13: Controller of input configuration block.

Fig. 14: Implementation of Input Configuration Block.

for charge recycling at the bottom plates of C_1 and C_2 . The CC contains a clocked comparator [17] tracking the output voltage, a phase generator based on [14] and a digital block, similar to the one in the ICB, selecting the core mode.

B. Input Configuration Block (ICB)

The input configuration block is responsible for the reconfiguration of the stacked converters (BCs). This block selects the stack mode and provides the correct interconnection of the inputs of the BCs. First, the ICB controller (Fig. 13) decides how many BCs to stack according to table II. It realizes this function by tracking the input voltage ($V_{IN} = IN_A - GND_D$) and comparing a divided version of V_{IN} to reference voltages REF_1 and REF_2 . Here, the resistive dividers from [7] are used to limit the power loss and REF_1 is externally applied to increase flexibility during testing. The controller runs at a lower speed (f_{CLK}) than the CC due to the slowly changing input voltage. As such, one comparator consumes about 223 nW, while the other components only demand power during mode changes. The values of B_1 and B_2 represent the stack mode.

Subsequently, B_1 and B_2 are translated into signals $S_1 - S_9$ according to the table in Fig. 13. These control signals drive the 9 switches in the ICB shown in Fig. 14. The switches are implemented as DMOS transistors and realize the interconnections of the BCs. Once the configuration of the BCs is settled, the ICB remains in a fixed state until the stack mode changes. The transistors in different colors indicate that the ICB is also a modular block. The same switches and interconnection patterns are repeated each time the number of BCs is doubled. This simplifies the expansion of the stacked converter.

In case of mode-changes, short circuit currents arise in the ICB when switches that should change state stay on at the same time, meaning that 2 stack-modes are activated at the same moment. To eliminate this power loss and protect

Fig. 15: Chip Micrograph.

the stacked converter against this unstable condition, non-overlapping clock generators (NOC) are added to the controller. This avoids overlap between control signals $S_1 - S_9$.

The ICB controller also operates in the 3V-domain, so that level shifters are added to drive the switches in the ICB. Because signals $S_1 - S_9$ do not change state often, the fully symmetrical capacitive LS from [15] is used, as shown in Fig. 14. To secure the start-up of the stacked converter, diodes are added to either the left or the right capacitor in the LS. These diodes ensure that the converter starts in a known mode. Furthermore, the high voltage domain generated in the cores might not be fully established during start-up. As this can cause incorrect bulk biasing of the transistors in the upper inverter, the bulk bias circuit of Fig. 12b is added.

The other components in the ICB ensure its correct operation. First, diodes are added to the switches that encounter reverse currents during reconfiguration of the stack. Second, bulk bias (BB) circuits are added to PMOS switches $S_7 - S_9$ to provide the correct bulk voltage in all stacking modes. Since the circuit in Fig. 12b is only operational when the difference between the X and Y voltage is larger than V_T of the transistors, the more complex BB-circuit in Fig. 14 is implemented. More specifically, as switches $S_7 - S_9$ are on in the ‘4-stacked mode’, their low drain-source voltage drop required an alternative solution. Finally, it is important to ensure a correct division of the input voltage between the BCs at all times. A large difference in the input voltages leads to an unbalance in the basic converters and can harm the stack operation. Therefore, the layouts of the BCs are identical to match their input impedances and the capacitors in the ICB help to maintain the balance during switching events.

Last, the influence of the controllers on the performance of the stacked converter is important. Since the ICB controller as well as the CC are realized at converter level, their area and power overhead is low. Additionally, since the size of the controllers does not depend on the output power, this overhead decreases when the BCs are scaled up to increase P_{OUT} . The power consumption of the ICB itself (Fig. 14) is negligible for the total converter due to 2 reasons. First, the ICB is only operational when the stack mode changes by a change in V_{IN} . Compared to the switching events in the BCs, these mode changes are rare. As a result, the ICB remains in the same state for a long time and is considered a static block not consuming switching power. One mode-change consumes about 30 pJ in the ICB and its controller. Second, the transistors in the ICB

Fig. 16: Measured voltages for $V_{IN} = 40$ V at peak P_{OUT} .

Fig. 17: Efficiency at peak P_{OUT} for wide input range.

are sized as large as possible to limit the conduction losses and voltage drop. Hence, the static power consumption of the ICB is limited to $27 \mu W$ on average, which reduces the conversion efficiency with less than 0.5 % on average. Since the mentioned voltage drop influences the input voltage of the stacked converters, the relative sizing of the transistors in the ICB is important to provide equal input voltages.

VII. CHIP MEASUREMENTS

The high voltage converter implementing the new principle of stacking with isolated switched capacitor cores, is fabricated in a $0.35 \mu m$ CMOS technology. Fig. 15 shows the chip micrograph with indications of the main building blocks. The design measures $5.4 mm^2$ and delivers a stable 3 V output for input voltages ranging from 7.5 to 42 V with peak output power of 2.1 mW while the core controller operates at 20 MHz.

Correct operation of the full stacked converter is shown in Fig. 16. Here, an input voltage of 40 V is applied at peak load power and the voltages across the stacked cores are measured. As shown in the graph, each of the 4 stacked converters sees an input voltage of 10 V and a stable 3 V output is generated.

The measured efficiency of the stacked converter for the full input voltage range is shown in Fig. 17. Here, each color indicates a different stack mode. The graph shows a repeating efficiency curve, which confirms the theory of section II-A. Indeed, a stacked converter keeps the efficiency of the single converter, independent of the chosen stack-mode. As a result, stacked power conversion can be considered a good design technique for high voltage wide range power conversion with good efficiency, since only the low VCR isolated converter should be optimized. Theoretically, the presented converter can operate at input voltages higher than 42 V, as indicated by the black dots in Fig. 17. The technology, however, does not ensure safe operation in this voltage region.

Fig. 18: Measured η -contours for variable V_{IN} and P_{OUT} .

A more detailed result of the converter is shown in Fig. 18, which displays contours of constant measured efficiency for varying V_{IN} and P_{OUT} . The repetitive pattern indicated by the different stack modes confirms that the stacked principle is operational and holds independent of the output power.

Table III summarizes the performance of the fabricated power converter and compares the presented work to the state-of-the-art monolithic SC DC-DC converters for high voltages. The stacked design converts the highest V_{IN} that has been reported for monolithic SC designs. Meanwhile, it achieves current I_P and power P_D densities similar to the cited works. The omnipresent voltage-power-technology trade-off in SC converters [8] is still visible when comparing the presented design to [13]. The latter reaches a higher power density but is implemented in a smaller technology node and can only handle voltages that are 5 times lower than the stacked converter. Nevertheless, this work performs better than [19] and as good as [8] while the maximum converted voltage is more than 2 times higher. The presented converter is also operational across a very wide range of input voltages thanks to the multiple VCRs created by mode- and stack-reconfiguration.

The stacked converter achieves the lowest output voltage ripple in comparison to the state-of-the-art converters. The ripple is calculated as the percentage voltage deviation on V_{OUT} . The measured output voltage of one stacked converter sample operating at peak output power with 25 V input is shown in Fig. 19a. Here, the typical ripple behavior in SC converters due to the different charge distribution phases can be noticed. In

(a) Measured V_{OUT} for $V_{IN}=25$ V and $P_{OUT}=2.1$ mW.

(b) Average ripple across full V_{IN} -range.

Fig. 19: Output voltage ripple: measured results.

this case, the ripple measures 2.8 %. Considering all operation modes and all input voltages, the ripple is limited to less than 5 %, as shown in Fig. 19b. The graph shows the measured ripple averaged across different samples and load conditions.

A new design technique for high voltage SC converters aiming for mW-range output power, a typical standby level of electronic applications, was introduced. Extension of the input voltage range can be reached by stacking more BCs if the technology limits are not violated. On the other hand, the presented design is perfectly fit for the 2-step AC-DC conversion approach presented in [20]. The stacked converter allows a higher intermediate DC voltage for the converter in [20] and can increase the performance of the AC-DC converter.

VIII. CONCLUSION

This work introduced stacked DC-DC power conversion using isolated switched capacitor converter cores. Stacking allows high voltage, high VCR conversion while the design is simplified to a single isolated core with a much lower conversion ratio and less VCRs. This isolated SC core separates the input and output terminals of the SC converter and leads to a stacked design without shorts. Wide input range operation is achieved by the input configuration block, which changes the number of stacked cores and this way the VCR of the converter. In the presented high voltage design, special attention is paid to the level shifters driving the switches in the different voltage domains and to the bulk bias circuits.

The presented stacked converter is fully integrated and achieves with its output power of 2.1 mW and 3 V on 5.4 mm² comparable results than the state of the art, while converting a much higher input voltage range of 7.5 V to 42 V with the lowest output voltage ripple.

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TABLE III

Comparison to Monolithic HV SC DC-DC Converters

	[13]	[18]	[8]	[19]	This work
Tech [nm]	90	350	350	180	350
# VCRs	8	17	1	117	9
max VCR	5:1	16:9	4:1	7-b SAR	12:1
V_{IN} [V]	2.5-8	2-13	17	3.4-4.3	7.5-42
V_{OUT} [V]	1.2	5	3.3	≥ 0.45	3
P_D [mW/mm ²]	13.3	1.47	0.44*	0.27	0.4
I_P [mA/mm ²]	11	0.29	0.13*	0.178	0.13
η_{MIN} [%]	66	22	40	50	49
η_{MAX} [%]	75.5	81.5	47.4	72	68.3
Ripple [%]	≤ 10	-	≤ 6	-	< 5

* estimated

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