Efficiency Gain in Plated Bifacial n-Type PERT Cells by Means of a Selective Emitter Approach Using Selective Epitaxy

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Highlights (5 points - 85 characters max including spaces)

- Selective growth of doped regions by epitaxy on laser ablated textured surfaces.
- Metallization by simultaneous plating of n- and p-type contacts in bifacial cells.
- Reduced $J_{0,plated}$ for p-type contacts by doping profile engineering with epitaxy.
- Thermal SiO_2/PECVD SiN_x passivation after epitaxy at the same level than ALD Al_2O_3.
- Gain in FF and V_{oc} for bifacial cells with a selective epitaxial emitter approach.

Abstract

This work evaluates the potential of selective epitaxy to mitigate the recombination losses at the p-type contact regions of plated bifacial n-type PERT cells. Following the growth of a 500 nm, $2.5{\cdot}10^{19}$ cm^{-3} boron doped epitaxial layer at the emitter contact regions defined by laser ablation of the passivating dielectrics, both an increase in V_{oc} (+6 mV) and FF (+1 % absolute) are measured in the final cells compared to the reference with a homogeneous diffused emitter. These results come with an average efficiency gain of 0.3 and 0.5 % absolute for front and rear side illumination, respectively. If the diffused, blanket emitter in the passivated regions is replaced by a thicker, lowly doped epitaxial profile (3 μm, $5{\cdot}10^{18}$ cm^{-3}) to further reduce recombination, an additional rise in implied V_{oc} after metallization of 10 mV is estimated. This increase would be the result of a reduction in $J_{0,pass,emitter}$ (down to 6 fA/cm^2) and $J_{0,plated,emitter}$ (down to 1967 fA/cm^2).

Keywords

Selective epitaxy, plating, bifacial solar cell, passivating contact, p-type contact.

1. INTRODUCTION

The bifacial PERT (Passivated Emitter, Rear Totally diffused) solar cells with the layout presented in Fig. 1 (*left*), and metallized using simultaneous plating of both n-type and p-type contacts, have already reached average efficiency values above 22 % [1]. Nonetheless, a breakdown analysis of the recombination losses reveals that there is still an important contribution of $J_{0,plated}$ (J_0 being the dark saturation current density at an injection level of 10^{16} cm^{-3}) on both p-type diffused emitter (~4000 fA/cm^2) and n-type laser-doped BSF (~1300 fA/cm^2) contacts.

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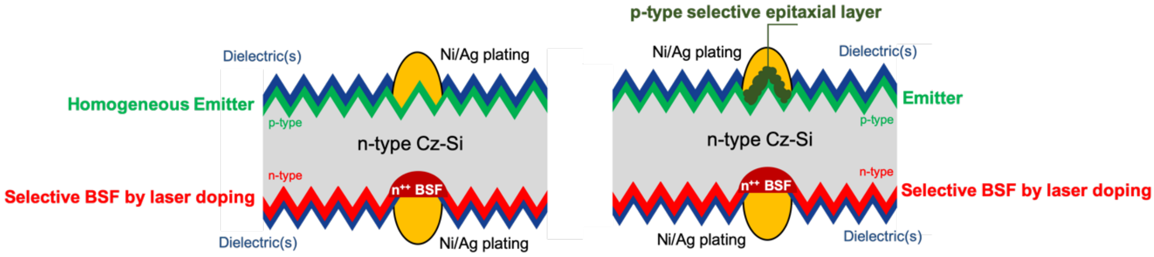

FIG. 1. Layout of the bifacial PERT solar cells of this work with co-plated n-type and p-type contacts: (*left*) reference cell with homogeneous emitter, (*right*) "p^+ epi" cell with a selective emitter by selective epitaxy.

The recombination losses in the contact regions of these bifacial devices, with a metal contact fraction of approximately 1 % for each contact polarity, account for more than 60 % of the total recombination losses. These losses are currently the main factor limiting the open circuit voltage (V_{oc}) and, therefore, the solar cell efficiency within reach for these devices.

A lot of the present research to mitigate the recombination losses at the semiconductor/metal interface of bulk crystalline silicon solar cells focuses on the implementation of polysilicon-based passivating contacts [2–10]. In this work, however, we aim at reducing the recombination attributed to the p-type emitter contact, which of both contacts contributes with the highest losses, by locally introducing in such a region a highly doped p-type epitaxial layer as schematically depicted in FIG. 1 (*right*).

As herein reported, the selective p-type epitaxial emitter approach, which only relies on high doping as a passivating mechanism, still results in higher minority carrier recombination losses than a p-type polysilicon-based contact. For the p-type polysilicon-based contact structure, where the interfacial oxide plays a key role in the passivation of the bulk silicon surface, J_0 values between 4 and 630 fA/cm^2 were measured depending on the specific process technology, test structure in use and characterization methodology [11–20].

Nevertheless, the selective p-type epitaxial emitter brings advantages in terms of integration simplicity as well as collection efficiency of majority carriers at the corresponding electrode. Only one additional step between patterning and metallization is required to selectively grow a local epitaxial layer on the regions to be contacted. In the selective epitaxial growth of silicon by thermal chemical vapor deposition (CVD), the growing layer is the result of a balance between the simultaneous silicon deposition from a silicon source (for example, SiH_2Cl_2), and the silicon etching from a chlorinated source (for example, HCl) upon substrates where only part of the surface is "masked" with a dielectric (stack) while the rest of the surface is "free" of dielectric(s). As shown in FIG. 2, the overall result is the growth of a silicon epitaxial layer solely on the bare silicon surface where the dielectric was opened during a previous patterning step. The remaining surface of the dielectric (stack), which will be kept for passivation and optical purposes at cell level, functions as a "mask" preventing the deposition of the epitaxial layer on that area [21–29]. An equivalent local polysilicon-based contact structure on the front side of a solar cell would require a more complex processing sequence [5]. In addition, the presence of the interfacial oxide would contribute to increase the specific contact resistance for the whole stack *metal/polysilicon/oxide/absorber* compared to the values measured for standard monocrystalline silicon contacts. For p-type polysilicon-based contacts, ρ_c values between 1 and 14 m$\Omega\cdot$cm^2 were already reported [14, 16–19].

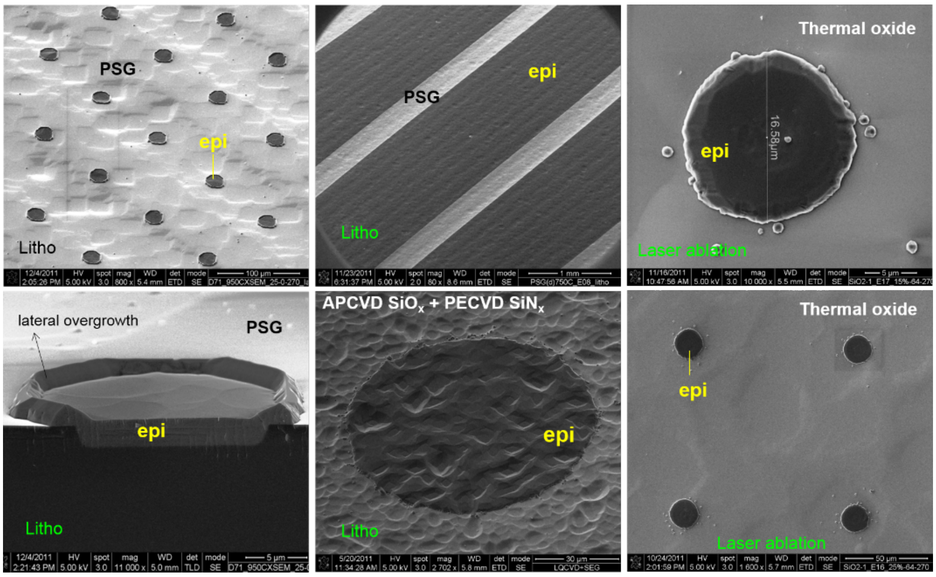

FIG. 2. SEM images illustrating examples of epitaxial layers selectively grown on silicon surfaces using a variety of dielectric masks patterned whether by laser ablation or photolithography.

The application of selective epitaxy to form the p-type local contact in bifacial PERT devices poses two main challenges: (1) the feasibility to selectively grow an epitaxial layer on the silicon surface opened during the dielectric patterning by laser ablation, and (2) the impact of the epitaxial thermal budget on the passivating properties of both front and rear dielectrics. Selective epitaxy has been successfully applied on blanket saw-damage-etched and textured surfaces as well as surfaces patterned by photolithography [21–29]. However, laser ablation of dielectrics to open the contact regions not only introduces damage, and therefore the presence of additional defects [30], but also gives rise to a very rough surface morphology as shown in FIG. 6 (left) which is not ideal for the growth of an epitaxial layer. Besides, dielectrics such as ALD Al_2O_3 and PECVD SiN_x are sensitive to a high thermal budget, and the growth of the epitaxial layer can degrade their passivating properties as a consequence of an increase in interface trap density, hydrogen effusion from the films, crystallization or other forms of chemical, physical and structural damage [31–34].

Taking the previous remarks into consideration, the first part of this work addresses the development of a p-type selective epitaxial deposition process on laser ablated surfaces, which is also compatible with the dielectric stack used for passivation. The second part of this work focuses on the integration of the p-type epitaxial layer in the emitter contact regions of plated bifacial n-type PERT solar cells.

2. MATERIALS AND METHODS

2.1 p-Type epitaxy for the emitter contact regions

Semi-device structures mimicking a bifacial PERT solar cell were fabricated to study the impact on passivation of the laser ablation process, the epitaxial thermal budget and the co-plating process. Those test structures, schematically depicted in FIG. 3, were fabricated on standard n-type monocrystalline Czochralski (Cz) silicon textured wafers (239 cm^2, 180 μm, 6 $\Omega\cdot$cm) with a diffused BBr_3 emitter on the front side (123$\pm$7 Ω/square) and a back surface field (BSF) by $POCl_3$ diffusion at the rear side. Each diffusion process was realized using an approximately 100 nm thick PECVD SiO_x mask on one side to get single side doping and preserve the fully textured surface on both sides of the final structure. A deep (3 μm) and lowly doped ($5\cdot10^{18}$ cm^{-3}) homogeneous (single-side) p-type epitaxial emitter (118$\pm$5 Ω/square) was also alternatively used instead of the BBr_3 emitter when assessing the recombination losses after plating at the emitter contacts.

As shown in FIG. 3 (left), two alternative dielectrics stacks were investigated as potential candidates for the emitter passivation: *(a)* the stack *thermal SiO_2/PECVD SiN_x* and, *(b)* the stack *ALD Al_2O_3/PECVD SiO_x/PECVD SiN_x*.

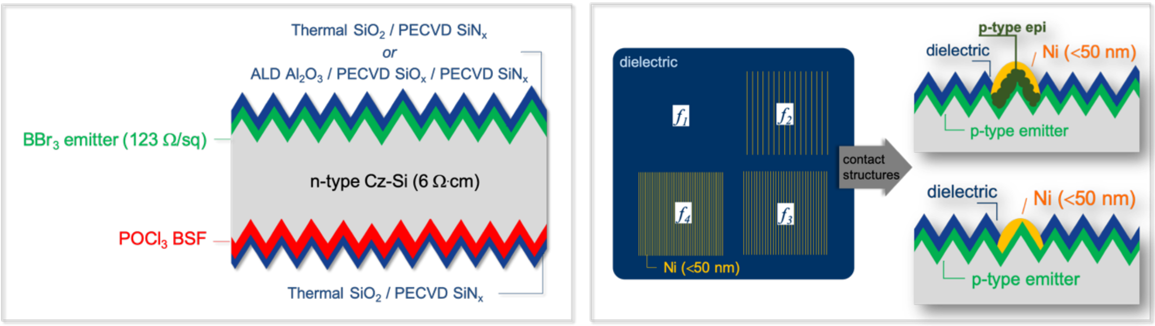

FIG. 3. Schematic of the structures employed to accomplish the growth of a p-type selective epitaxial layer on the laser ablated surface at the emitter contact regions: *(left)* test structure used to assess the impact of the epitaxial thermal budget on the dielectric passivation, and *(right)* test structure used to assess the p-type emitter contact recombination after plating where f_i (between 0 % and 10 %) represents the dielectric open fraction after laser ablation.

The dielectric patterning on the emitter side was performed by picosecond laser ablation using the Talisker™ ultraviolet (355 nm) laser of the Aethon Laser Platform from Coherent. The laser ablation was performed with a fixed laser repetition rate of 200 kHz, a laser fluence in the range 45–90 μJ/cm^2 and a scribing speed between 500–1000 mm/s. The ablation conditions were such that they guaranteed the opening of the dielectric stack with a minimum laser-induced damage.

The p-type epitaxial layers were grown in-house by CVD at reduced pressure (<100 Torr) in an ASM EPSILON® 2000 reactor, a single-wafer batch tool typically used for micro-electronics applications. The deposition took place in H_2 atmosphere using SiH_2Cl_2 as silicon precursor. The doping of the layers was realized in-situ by means of B_2H_6 and, to keep selectivity, HCl was also employed as an etching source. The basic steps of this process consist of: (a) temperature ramp-up from 200 °C to deposition temperature, (b) H_2 bake, (c) selective silicon deposition, and (d) cool-down from deposition temperature to 200 °C. The H_2 bake, taking place before the actual deposition step and at the same temperature, is a critical step which assists in the growth of a high-quality epitaxial layer by removing the native oxide from the silicon surface through hydrogen reduction.

To investigate the impact of the epitaxial thermal budget on the dielectrics' passivation, the structures depicted in FIG. 3 (left) have gone through the epitaxial step in the CVD reactor but without actual growth occurring, that is, in H_2 atmosphere but without silicon and p-type dopant precursors.

The metallization of the contacts was realized by Ni/Ag electroless and immersion plating. This process, which enables simultaneous, contact free, co-plating of n-type and p-type contacts, has been specially developed for bifacial cells in combination with multi-wire interconnection technology [1, 35]. In this work, the standard plating conditions for monocrystalline silicon contacts described elsewhere [1] were applied.

The $J_{0,pass}$ (J_0 for the passivated regions) values herein reported were calculated at an injection level of 10^{16} cm^{-3} using Kane and Swanson approach [36] to fit the injection-level-dependent effective lifetime data measured by PL-QSSPC (Photo-Luminescence Quasi-Steady-State-Photoconductance) at 25 °C in the LIS-R1 multipurpose characterization tool from BT Imaging. In this analysis the parametrization for the intrinsic recombination in crystalline silicon by Richter et al. [37] was implemented. The $J_{0,plated}$ (J_0 for the regions metallized using Ni/Ag co-plating) was extracted at an injection level of 10^{16} cm^{-3} following the method after Deckers et al. [38–39] on dedicated test structures, as shown in FIG. 3 (right), with a variable open fraction after laser ablation patterning, f, between 0 % and 10 %. For each structure with a specific f, the injection-level-dependent effective lifetime was measured by PL-QSSPC. The difference between the saturation current density at the plated junctions and the saturation current density at the passivated junctions ($J_{0,plated} - J_{0,pass}$) was extracted from the slope of the inverse effective lifetime at an injection level of 10^{16} cm^{-3} versus f. In the structures investigated where the recombination at the passivated surface dominates bulk recombination, $J_{0,pass}$ could be extracted from the intercept with the $f = 0$ axis.

The specific contact resistance (ρ_c) for the metal/semiconductor interface was measured on plated textured surfaces using the conventional transfer length method (TLM), originally proposed by Shockley et al. in 1964 [40] and extensively used and discussed in literature [41–43]. In this work, the resistance measurements between progressing pairs of contacts as a function of the pair distance were performed in a Kb·esi tool.

2.2 Solar cell integration

Reference (Fig. 1, *left*) and "p$^+$ epi" (Fig. 1, *right*) plated bifacial n-type PERT solar cells were fabricated on textured n-type Cz silicon wafers (239 cm^2, 180 μm, 3.5 Ω.cm) using the process sequence depicted in FIG. 4. All the devices have a homogeneous BBr_3 diffused emitter (130±2 Ω/square) on the front side. However, unlike the reference, the "p$^+$ epi" cells also incorporate a local $2.5 \cdot 10^{19}$ cm^{-3} boron-doped, 500 nm thick epitaxial layer at the emitter contact regions. The emitter passivation stack for the "p+ epi" cells consists of thermal SiO_2/PECVD SiN_x while for the reference cells is based on ALD Al_2O_3/PECVD SiO_x/PECVD SiN_x.

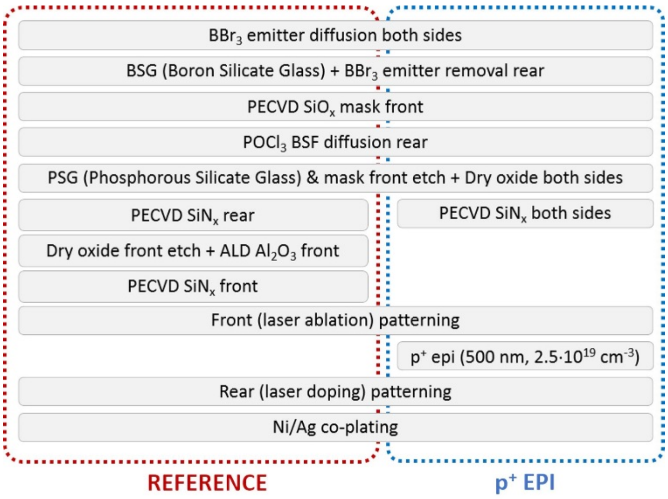

FIG. 4. Fabrication sequence for the reference and "p$^+$ epi" plated bifacial n-type PERT cells of this work.

The cells were characterized in-house by light I-V and dark I-V. These measurements were done in a solar simulator from Wacom Electric Co. using the Grid TOUCH contacting system developed by Pasan S.A. In these internal measurements the AM1.5G spectral irradiance was corrected based on a reference cell calibrated at Fraunhofer ISE CalLab.

3. RESULTS AND DISCUSSION

3.1 p-Type epitaxy for the emitter contact regions

The first goal of this study was to assess the impact of the epitaxial thermal budget on the passivating properties of both front and rear dielectric stacks. With this in mind, the test structures schematically depicted in FIG. 3 (left) have gone through the epitaxial step, without actual growth occurring, to determine the maximum epitaxial temperature and (deposition) time that those dielectric layers could withstand without losing their passivating properties. The results are displayed in FIG. 5 in terms of $J_{0,pass,total}$ ($J_{0,pass}$ for the complete test structure) as a function of epitaxial temperature and (deposition) time for both emitter passivation approaches investigated: FIG. 5 (top) thermal SiO_2/PECVD SiN_x and, FIG. 5 (bottom) ALD Al_2O_3/PECVD SiO_x/PECVD SiN_x. Those results are also compared to the values measured for the reference structure without epitaxial thermal budget, in other words, structures which would not include a p-type epitaxial layer at the emitter contact regions.

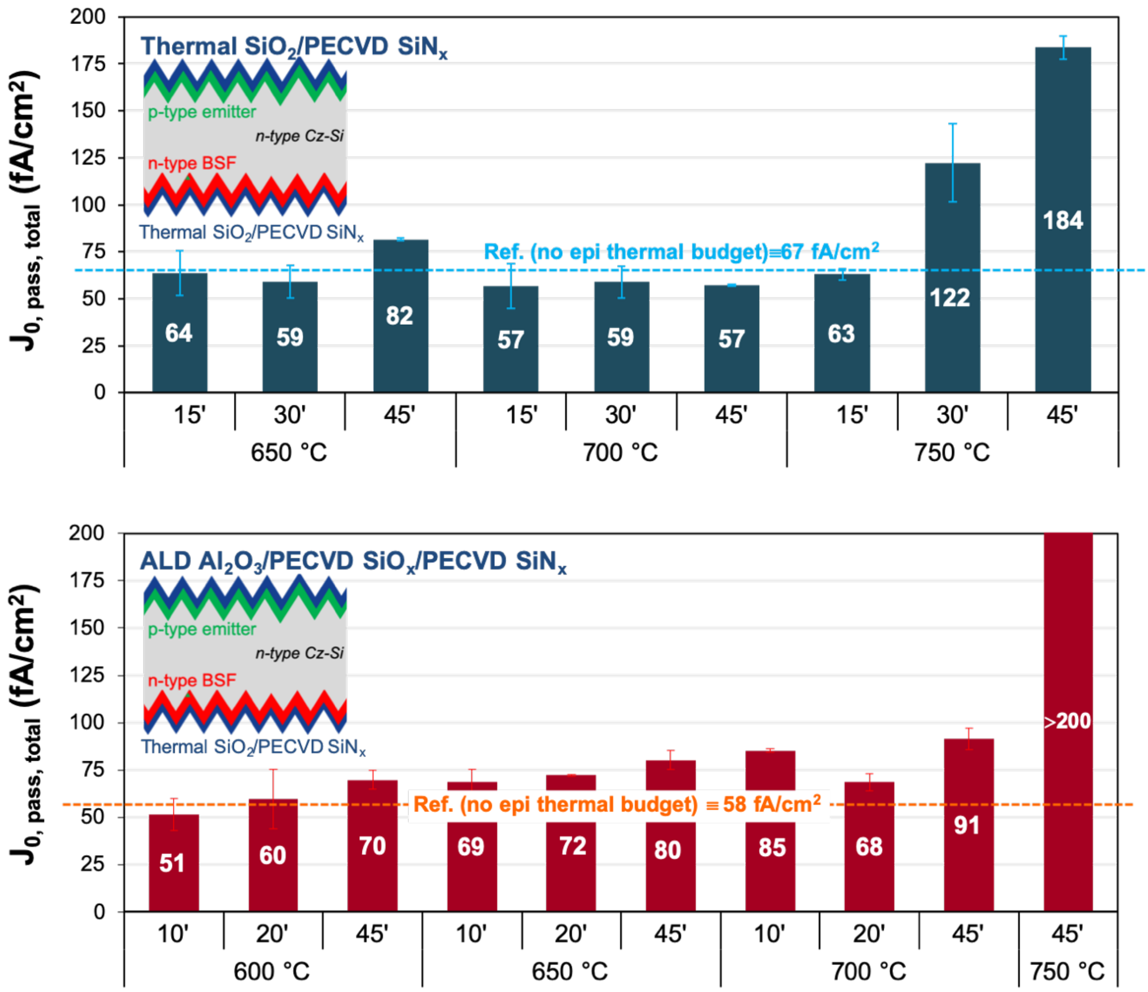

FIG. 5. $J_{0,pass,total}$ (fA/cm^2) extracted at 10^{16} cm^{-3} (average of 3 samples/condition) for test structures after epitaxial thermal budget and for the reference (with no epitaxial step). Emitter passivation by: (top) thermal SiO_2/PECVD SiN_x, and (bottom) ALD Al_2O_3/PECVD SiO_x/PECVD SiN_x.

When using thermal SiO_2/PECVD SiN_x, the results confirm that there is a remarkable increase in recombination after an epitaxial thermal budget above 750 °C (>30 min). A similar study performed on symmetric BSF and emitter structures reveals that this degradation happens simultaneously for both the p-type and the n-type doped regions for which there is a 3-fold and a 6-fold increase in $J_{0,pass}$, respectively, when the epitaxial step is performed at 750 °C compared to the values measured at 700 °C ($J_{0,pass,emitter}$~47 fA/cm^2 $J_{0,pass,BSF}$~10 fA/cm^2 at 700 °C) [44]. In this case, an optimum epitaxial deposition temperature of 700 °C goes together with the suitable conditions to contribute with hydrogen passivation from PECVD SiN_x. Hydrogen is known to be released from this dielectric around that temperature [45–46].

The same investigation on the structures with ALD Al_2O_3/PECVD SiO_x/PECVD SiN_x confirms that selective epitaxy would introduce a thermal budget which is too large to keep the excellent passivation measured for the reference case. Only if epitaxy took place at a temperature below 600 °C, we could not only keep but also improve the performance compared to the reference. At higher deposition temperature the passivation collapses because of different forms of damage (increase in interface trap density, hydrogen desorption from defects, stress or crystallization of the films) [31–34]. When the experiment was realized on symmetric BSF and emitter structures, the results demonstrate that this passivation loss is mainly dominated by the quicker degradation of ALD Al_2O_3. The $J_{0,pass,emitter}$ for symmetric emitter structures passivated with ALD Al_2O_3/PECVD SiO_x/PECVD SiN_x increases more than 10 times after an epitaxial step at 750 °C compared to the values measured at 600 °C ($J_{0,pass,emitter}$~27 fA/cm^2 at 600 °C).

In view of the previous results, the implementation of an epitaxially grown p-type layer at the emitter contact regions of bifacial PERT solar cells focused on the emitter passivation by thermal SiO_2/PECVD SiN_x, and on the development of a selective epitaxial process at 700 °C. At this temperature there is a broad processing window for the (deposition) time (from 10 min up to 120 min tested in this work), for which the emitter passivation by thermal SiO_2/PECVD SiN_x after epitaxial thermal budget is even at the same level than the ALD Al_2O_3-based emitter passivation.

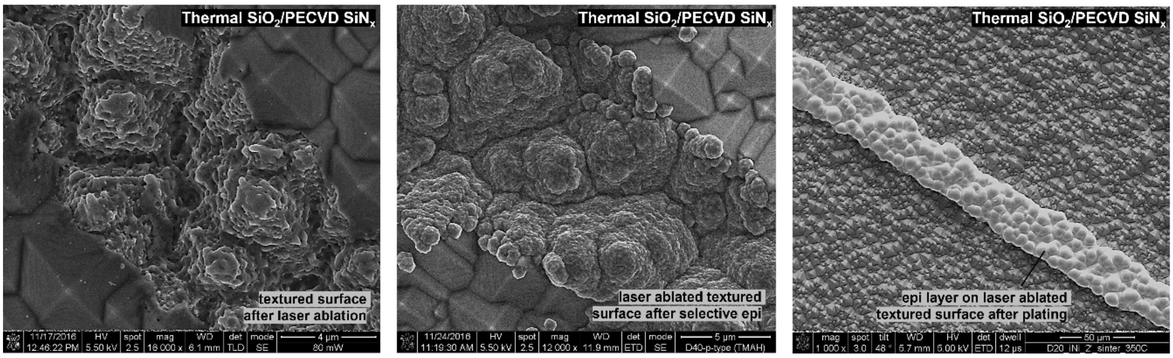

FIG. 6. Top view SEM images: (left) textured surface after laser ablation, (middle) laser ablated textured surface after the selective growth of a p-type epitaxial layer, and (right) p-type epitaxial layer selectively grown on a laser ablated textured surface after plating.

The following step in this development aimed at the patterning prior to epitaxy and the metallization of the grown layers. The thermal SiO_2/PECVD SiN_x patterning was realized using the laser ablation conditions described in section 2.1 where approximately 10 μm wide lines were opened. The top view SEM image of FIG. 6 (left) shows the surface morphology of the laser ablated textured surface prior to epitaxy. As for any doping process, a cleaning step must be introduced between the laser ablation patterning of the dielectrics and the selective epitaxial step. The cleaning is required to remove any impurity or native oxide present on the open silicon surface, which can prevent a selective deposition or unnecessarily degrade the quality of the grown film and therefore its electronic properties. The iPV cleaning we normally use in-house during solar cell processing [47], and which consists of a 2-step sequence based on DIW/O_3/HCl and DIW/HF/HCl was also applied here prior to epitaxy. The SEM image of FIG. 6 (middle) shows the surface morphology of a p-type epitaxial layer selectively grown on a laser ablated textured surface after the iPV cleaning. As shown in FIG. 6 (right), the plating of those layers was proven to be successful. The contact adhesion was tested to be as good as for the reference case without epitaxy, and the ρ_c for an epitaxial layer of $2.5{\cdot}10^{19}$ cm^{-3} and 500–750 nm was also at the same level as the reference (1.6 mΩ·cm^2). With respect to the recombination losses, FIG. 7 shows the $J_{0,plated}$ values which were measured after plating for the p-type emitter contacts herein investigated. The reference structure consisting of a plated, laser ablated BBr_3 (123 Ω/square) contact contributed with the highest recombination losses ($J_{0,plated,reference}$~3994 fA/cm^2). The plated contact incorporating a 500 nm, $2.5{\cdot}10^{19}$ cm^{-3} p-type epitaxial layer between the metal and the laser ablated BBr_3 (123 Ω/square) emitter could enable a twenty-five percent reduction in the recombination losses ($J_{0,plated,epi/BBr3}$~3063 fA/cm^2) compared to the reference. If, in addition, the BBr_3 diffused emitter (123 Ω/square) was replaced by a deep (3 μm) and lowly doped ($5{\cdot}10^{18}$ cm^{-3}) p-type epitaxial emitter (118 Ω/square), the recombination at the emitter contact regions would be even further reduced ($J_{0,plated,epi/epi}$~1967 fA/cm^2) to half of the value measured for the reference contacts.

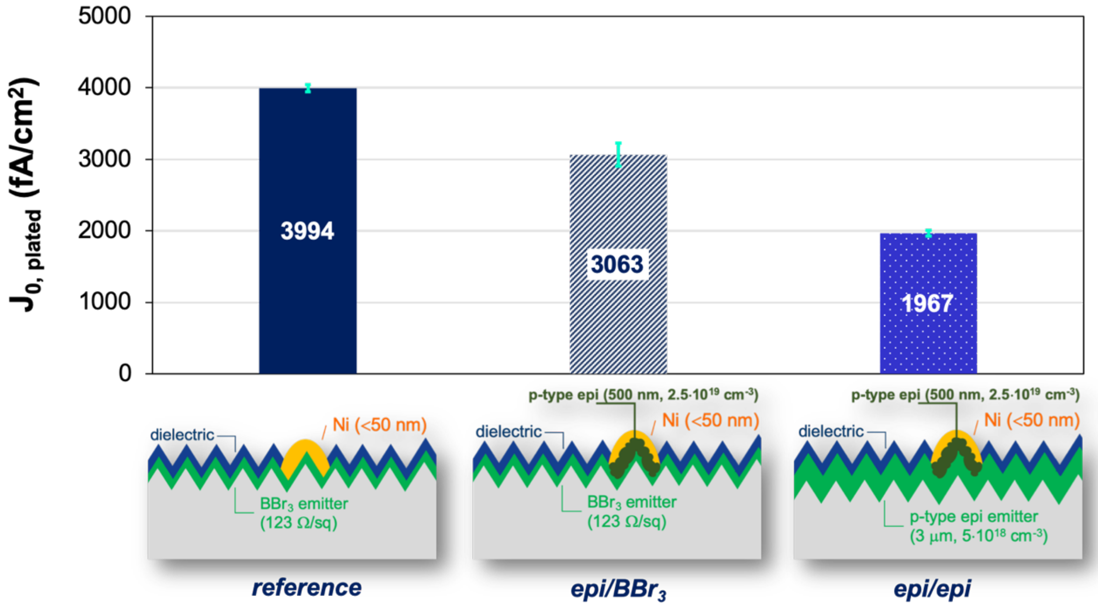

FIG. 7. $J_{0,plated}$ (fA/cm^2) extracted at 10^{16} cm^{-3} (average of 4 samples/condition) for the three type of plated p-type emitter contacts investigated: reference, epi/BBr_3 and epi/epi.

These results align with the general trend already reported in literature [48–49] where the recombination losses for the metallized regions decrease with increasing surface dopant concentration and junction thickness. The p-type epitaxial layer locally grown at the emitter contact regions is more highly doped than the BBr_3 diffused emitter. Secondary Ion Mass Spectrometry (SIMS) confirmed that the p-type epitaxial contact layer has a uniform doping of $2.5\cdot10^{19}$ cm^{-3} through its whole thickness of 500 nm, while the BBr_3 diffused emitter underneath has a Gaussian profile with a surface concentration (N_s) about $9\cdot10^{18}$ cm^{-3}. The impact of the increase in junction thickness is especially remarkable for the case where the BBr_3 diffused emitter (<1 µm, $N_s \cong 9\cdot10^{18}$ cm^{-3}, 123±7 Ω/square) is replaced by the thicker and more lowly doped p-type epitaxial emitter (3 µm, $5\cdot10^{18}$ cm^{-3}, 118±5 Ω/square). Further reduction in $J_{0,plated,epi/BBr3}$ or $J_{0,plated,epi/epi}$ could be expected if the selective epitaxial deposition process would be adapted to increase the doping level of the locally grown p-type epitaxial contact layer above the current value of $2.5\cdot10^{19}$ cm^{-3}.

3.2 Solar cell integration

The results of TABLE I confirm the overall efficiency gain for the "p$^+$ epi" flow corresponding to an improvement in both V_{oc} (+6 mV) and fill factor (FF) (+1 % absolute).

The V_{oc} increase is the main result of a reduction in $J_{0,plated}$ from 3994 fA/cm^2 for the reference down to 3063 fA/cm^2 for the "p$^+$ epi" group as previously presented in FIG. 7. The $J_{0,pass}$ for the BBr_3 emitter (130±2 Ω/square) in the "p$^+$ epi" flow with *thermal SiO_2/PECVD SiN_x* (21±3.5fA/cm^2) was measured to be at the same level than the one measured for the reference flow with *ALD Al_2O_3/PECVD SiO_x/PECVD SiN_x* (22±0.6 fA/cm^2).

Although the series resistance for both groups was in the same range (0.5–0.6 mΩ·cm^2), the shunt resistance for the "p$^+$ epi" cells was systematically larger (>20 Ω) than for the reference (<10 Ω). TABLE I also reports lower J_{02}, which accounts for the recombination in the junctions, for the "p$^+$ epi" cells. The better values achieved for the shunt resistance as well as the J_{02} may explain the gain in FF for the "p$^+$ epi" flow. In turn, this improvement could be associated to the thickening of the emitter contact by the presence of the p-type epitaxial layer and, thereby, the mitigation of the patterning and metallization-induced damage compared to the reference group.

TABLE I. Average (and standard deviation) I-V results for the reference and "p+ epi" plated bifacial n-type PERT cells of this work (239 cm2). In-house measurements.

Cell type	Illumination side	J_{sc} (mA/cm^2)	V_{oc} (mV)	*FF* (%)	η (%)	*n*	J_{02} (10^{-9} A/cm^2)
Reference (8 cells)	Emitter	40.4 $\pm$ 0.0	673 $\pm$ 1	79.5 $\pm$ 0.6	21.6 $\pm$ 0.2	1.12	11.7
	BSF	38.5 $\pm$ 0.4	672 $\pm$ 2	79.2 $\pm$ 0.6	20.5 $\pm$ 0.2		
p^+ Epi (14 cells)	Emitter	40.1 $\pm$ 0.1	679 $\pm$ 2	80.4 $\pm$ 1.0	21.9 $\pm$ 0.3	1.03	3.4
	BSF	38.5 $\pm$ 0.2	678 $\pm$ 1	80.3 $\pm$ 0.2	21.0 $\pm$ 0.2		

When the bifacial cells are illuminated from the rear side, the improvements in the "p^+ epi" flow correspond to an absolute efficiency gain of 0.5 %, while this one is limited to 0.3 % absolute for front side illumination. The smaller efficiency gain in the latter case is because of a lower short circuit current density (J_{sc}) for the cells with a selective epitaxial emitter for which the emitter contact line width (~19 µm) is wider than for the reference (~15 µm). This increase in the line width is the consequence of the lateral overgrowth of the 500 nm epitaxial layer on the open dielectric region as depicted in FIG. 8. At cell level this J_{sc} loss could be minimized by correcting the line pitch at the emitter contact without compromising the FF.

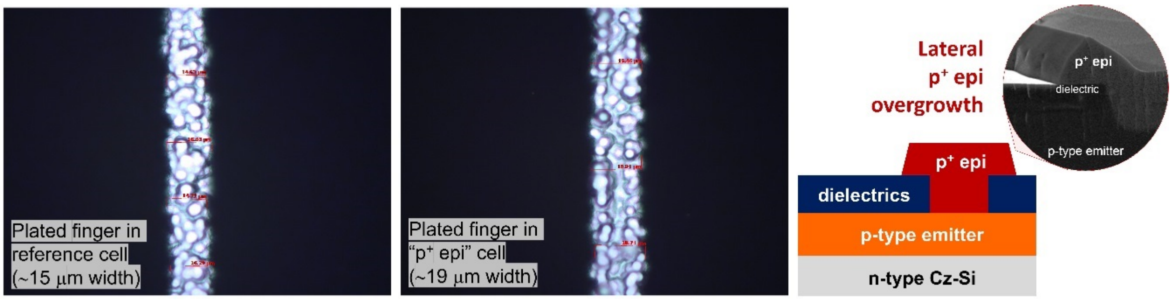

FIG. 8. (*left*) Optical microscope image of a plated finger in a reference cell, (*middle*) Optical microscope image of a plated finger in a "p+ epi" cell, and (*right*) schematic of the lateral epitaxial overgrowth at the edge of the contact lines opened in the dielectric stack.

In this work, the best "p^+ epi" solar cell achieved a power conversion efficiency of 22.1 % (J_{sc} = 40.1 mA/cm^2, V_{oc}= 680 mV and FF = 81.0 %, in-house measurements for illumination from the emitter side). However, further improvements could still be realized, if we consider that the incorporation of the epitaxial layer in the contact regions enables an independent optimization of the passivated emitter profile from that one in the metallized areas. With this strategy in mind, for example, an increase in implied V_{oc} after metallization of at least 10 mV could be estimated when replacing the BBr_3 diffused emitter by the thick (3 µm) and lowly doped ($5\cdot10^{18}$ cm^{-3}) p-type epitaxial emitter (118±5 Ω/square) already presented in section 2.2. The gain in implied V_{oc} would be the result of: (*a*) a lower $J_{0,pass,emitter}$=6±1 fA/cm^2 because of the significant reduction in Auger recombination, and (*b*) a lower $J_{0,plated,epi/epi}$= 1967±42 fA/cm^2 because of the thicker doped region under the metal contact.

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4. CONCLUSIONS

This work demonstrates the feasibility of selective epitaxy to locally grow doped layers on laser ablated textured surfaces, and the potential of the technology to reduce the recombination losses at the p-type emitter contacts of bifacial plated n-type PERT solar cells. A selective epitaxial deposition process at 700 °C and compatible with an emitter passivation by thermal SiO_2 and/or PECVD layers was developed. By means of this process, and in 1-single step between dielectric patterning by laser ablation and metallization by plating, a 500 nm, $5{\cdot}10^{18}$ cm^{-3} p-type epitaxial layer was locally grown at the emitter contacts. The bifacial devices with the locally grown p-type epitaxial layer demonstrated an average gain both in V_{oc} (+6 mV) and FF (+1 % absolute) compared to the reference without epitaxy, reaching a maximum solar cell efficiency of 22.1 % (for illumination from the emitter side). This improvement is associated to the reduction in $J_{0,plated}$ for the epitaxial case. The $J_{0,plated}$ for the reference structure consisting of a plated, laser ablated BBr_3 (123 Ω/square) contact was about 3994 fA/cm^2 while for the contact additionally incorporating a 500 nm, $2.5{\cdot}10^{19}$ cm^{-3} p-type epitaxial layer was reduced to 3063 fA/cm^2. Besides, if the BBr_3 diffused emitter (123 Ω/square) was replaced by a deep (3 μm) and lowly doped ($5{\cdot}10^{18}$ cm^{-3}) p-type epitaxial emitter (118 Ω/square), the $J_{0,plated}$ would be even further reduced down to approximately 1967 fA/cm^2 which, if integrated, could also contribute to a further improvement in the solar cell efficiency.

5. REFERENCES

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