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Phase-Control Techniques for Sub-Sampling Phase-Locked Loops

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Abstract—Local oscillators with phase-control can be applied in a wide range of applications, from antenna phased arrays to synchronization. In this work, two techniques for introducing phase-control to a sub-sampling phase-locked loop (SSPLL) are presented. By means of a biasing voltage or a tuning current, it is possible to continuously control the output phase of the SSPLL within a 180-degree range. To evaluate both techniques, a proof-of-concept circuit was developed, simulated and measured, achieving good agreement with theory.

Index Terms—Antenna phased arrays, LO beamforming, phased-locked loops (PLL), sub-sampling, synchronization.

I. INTRODUCTION

Phase-control of a Phased-Locked loop (PLL) is a highly desirable property. It can be used in a large variety of applications, from PLL-based modulation [1] to analog beamforming [2], [3] and synchronization of multi-chips [4], [5]. For instance, the use of PLLs with phase-control capabilities to implement Local Oscillator (LO) path beamforming transceiver architectures is one possible solution for the complex LO distribution issues reported by LO-beamforming architectures [6], [7]. By distributing a lower-frequency reference to each channel and locally synthesizing the RF frequency on each path with the desired phase, the routing of high-frequency LO is severely reduced.

Synchronization between different antenna-paths in a large array is also an issue with reported solutions relying on mutual-coupling between PLLs to synchronize [5], [8] which in turn amplifies the LO distribution issues throughout the array. The use of PLLs with phase-control potentially solves synchronization issues without amplifying distribution issues [9].

Recently, a new PLL architecture was introduced in the literature [10], where sub-sampling phase detectors (SSPD) are used instead of the traditional tri-state phase-frequency detector (PFD). The architecture was quickly adopted in literature due to its improvement in PLL figure-of-merit, mainly due to the absence of a frequency divider from its main feedback path.

In this work, we present techniques to introduce phase-control on a sub-sampling PLL through the feedback loop. A major advantage of the proposed techniques is its simplicity, as it does not require complex hardware [7] or rely on a precise time-delay [4], [5]. The utilization of phase control in a sub-sampling PLL also brings the benefits of such architecture

Fig. 1. Sub-sampling phase detector (SSPD) (a) conceptual schematics and (b) transfer function.

[10] when compared to a standard charge-pump PLL [6]. To evaluate the feasibility of the proposed techniques, a proof-of-concept circuit was developed, simulated and measured, showing agreement with theory.

II. PHASE-CONTROL FOR SUB-SAMPLING PLLS

A. Sub-Sampling PLL

The concept of a SSPD was introduced in [10] and is pictured in Fig. 1(a). It consists of two track-and-hold circuits to acquire the current phase of the voltage-controlled oscillator (VCO), followed by a voltage-to-current converter (transconductance amplifier), to transform its phase information into input for the loop filter. Considering a sinusoidal VCO signal given by

$$V_{VCO} = A_{VCO} \sin(2\pi f_{VCO} t + \phi(t)) \quad (1)$$

where f_{VCO} is a multiple of the reference frequency (i.e. $f_{VCO} = N f_{REF} = N/T_{ref}$), the output current characteristics of the SSPD are given by

$$i_o(nT_{ref}) = g_m 2A_{VCO} \sin(\phi(nT_{ref})) \quad (2)$$

where g_m is the transconductance of the V-to-I converter. The phase transfer characteristics of the SSPD is pictured in Fig. 1(b), where N is the multiplication factor of the PLL. The equilibrium point of the system is its ideal locking point, given when $i_o = 0$, which leads to $\phi = 0^\circ$.

The SSPD can be employed in a PLL. The main advantage of its usage is the absence of a frequency divide-by- N block, which increases the phase-noise contribution of the CP by N^2 , proven in [10]. However, since the SSPD does not differ between reference harmonics, an auxiliary frequency locked loop (FLL) is necessary to lock at the desired reference harmonic. A classical CP-PLL is added to bring the output

Fig. 2. Block diagram of the Sub-Sampling Phased-Locked Loop.

to the right frequency and a dead-zone between the phase-frequency detector (PFD), and the CP is added to deactivate the auxiliary loop at the desired frequency, as pictured in Fig. 2. Notice that, although this architecture has a frequency divider, it is on the auxiliary path, which is turned off when phase-lock is achieved. In order to control the output phase of the SSPLL, we must be able to change the equilibrium point of the system (shown in Fig. 1(b)). Here we present two different methods to implement the phase-control.

B. Voltage-Based Phase-Control Technique

Consider the system from Fig. 3(a), where a digitally controlled voltage source V_b is introduced at the negative input of the SSPD (highlighted in gray). The output current is now given by

$$i_o(nT_{ref}) = g_m [A_{VCO} \sin(\phi(nT_{ref})) - V_b] \quad (3)$$

The feedback loop acts to compensate the introduced perturbation by changing its equilibrium phase-locking point, which is obtained when i_o equals zero. The equilibrium phase-locking point is then shifted to

$$\phi = \sin^{-1} \left(\frac{V_b}{A_{VCO}} \right) \quad (4)$$

Hence, by changing the voltage V_b , it is possible to control the phase locking point, and by extension, the output phase of the SSPLL. The phase transfer characteristic under voltage-based phase-control is represented in Fig. 3(b). At first glimpse, one could argue that a second locking-point is also available to be the equilibrium point of the system. However, that point is not stable due to the negative slope of the sinusoidal curve, bringing the system to the correct locking point. This property also limits the phase tuning range within $180^\circ (\pm 90^\circ)$.

C. Current-Based Phase-Control Technique

Consider now the system from Fig. 4(a), where a digitally-controlled tuning current i_{TUN} is introduced at the loop's input (highlighted in gray). The SSPD must compensate the tuning current so that the system can achieve equilibrium. The equilibrium phase of the system under a current perturbation is now given by

Fig. 3. SSPLL with voltage-based phase-control (a) block diagram and (b) phase transfer function.

Fig. 4. SSPLL with current-based phase-control (a) block diagram and (b) phase transfer function.

$$\phi = \sin^{-1} \left(-\frac{i_{TUN}}{2g_m A_{VCO}} \right) \quad (5)$$

which shows that, by adjusting the tuning current, it is possible to control the output phase. The phase transfer characteristic of the system under current-based phase-control is represented in Fig. 4(b). The same stability property is seen here, which limits the phase tuning range to 180° as well.

An important limitation of the proposed phase-control techniques is the requirement of a sinusoidal or quasi-sinusoidal waveform, as the phase-control can only be guaranteed in a one-to-one voltage/current to phase correspondence. A saturated waveform would reduce the phase-range within its slope region, as the saturated region would lead to various phase values for the same voltage/current values.

Fig. 5. Block diagram of the Sub-Sampling Phased-Locked Loop.

III. PROOF-OF-CONCEPT PROTOTYPE

A circuit prototype was designed using components off-the-shelf (COTS) to verify the proposed techniques. Due to the limitations of a COTS prototype, we have focused on demonstrating the feasibility of the proposed techniques instead of benchmarking the performance of the circuit itself. The circuit diagram of the prototype is pictured in Fig. 5, where some biasing blocks were omitted to improve readability.

As the aim of the prototype is to demonstrate the feasibility of the technique, a lower frequency circuit was designed, with a frequency range between 1 MHz and 2 MHz, and a reference at 0.2 MHz. To implement the digital functions of the circuit presented in the FLL, the standard 7400 family was used. The charge pump was implemented using standard bipolar transistors (BC547 and BC557). The SSPD implementation was performed using a LM13700 as a differential operational transconductance amplifier (OTA) and NLAS4157 as a switch. To control the SSPD, a standard two-phase with non-overlap circuit was used. Although a sinusoidal Voltage-Controlled Oscillator (VCO) is required for the control techniques, it was not available at the desired frequency. Therefore a square-wave VCO with a low-pass filter was used to emulate one.

To implement both techniques in the same prototype, the choice for a single-ended version of the SSPD was made. During the measurement of the Current-based phase control, the biasing voltage V_b is kept constant to cancel the common-mode voltage of the VCO. The prototype board and the measurement setup are represented in Fig. 6.

IV. EXPERIMENTAL RESULTS

To evaluate the COTS prototype, the time difference between the reference and the output frequency rising edge (Δ_T) was characterized, as a square-wave VCO output was also available. Fig. 7 pictures a couple of the measurements for the Voltage-based technique. When changing the biasing voltage

Fig. 6. Prototype board and measurement setup for the proposed system.

from 2.504 V to 3.187 V, Δ_T increased from 13.58 ns to 217.3 ns. Such data was collected through SPICE simulations and measurements, using both proposed techniques and using different frequency multiplication factors ($N = 5, 6$ and 7). Furthermore, to compare different frequencies and better analyze the results, the time-difference was transformed into phase-shift and both the bias voltage and the tuning current were normalized with respect to their denominators.

A. Voltage-Based Phase-Control

The relative phase-shift with respect to the normalized biasing voltage is presented in Fig. 8. A good agreement with the theoretical developments is achieved. For the measurement results, a gain error is readily observed, together with non-linearities. Since the input waveform of the SSPD is not a perfect sinusoidal, some deviations are obtained from the ideal characteristic. It shows that the system is rather sensitive to VCO's linearity, but the ability of continuous tuning allows room for a pre-distortion of the biasing voltage.

B. Current-Based Phase Control

The relative phase-shift with respect to the normalized tuning current is presented in Fig. 9. Once again, a good agreement with theoretical developments is achieved. Since the transconductance g_m was estimated using linear regression, the gain error was mitigated. The same issues with non-linearities are observed for the current-based method, with the addition

Fig. 7. Measured waveforms for $N=5$ ($f_{VCO} = 1$ MHz): (a) reference, (b) VCO output with $V_b = 2.507$ V, obtaining $\Delta_T = 13.58$ ns (c) VCO output with $V_b = 3.187$ V, obtaining $\Delta_T = 217.3$ ns.

Fig. 8. Simulated and measured relative phase-shift vs. normalized bias voltage for different multiplication factors under voltage-based phase-control.

Fig. 9. Simulated and measured relative phase-shift vs. normalized tuning current for different multiplication factors under current-based phase-control.

of the transconductor distortion, since a large input swing is required. By using a differential version of the SSPD, non-linearity issues are expected to be reduced.

A comparison between a few different phase-control techniques is presented in Table I. The proposed technique achieves frequency independence with low complexity when

TABLE I
COMPARISON BETWEEN PHASE-CONTROL TECHNIQUES

Ref.	[4]	[7]	[6]	This work
Technique	Reference Path Delay	Divider Path Delay	CP-PLL Loop Ctrl	SS-PLL Loop Ctrl
Resolution	Coarse	Fine	Continuous	Continuous
Phase Range	360°	360°	360°	180°
Frequency Dependence	Yes	Yes	No	No
Complexity	Low	High	Low	Low
Suitable for Integration	No	Yes	Yes	Yes

compared to delay techniques, with the addition of using a lower phase-noise architecture as a basis. The main drawback is the limited range and a non-linear phase-control relationship.

V. CONCLUSION

Two different techniques to implement phase-control in a sub-sampling PLL have been shown. Both techniques are low-cost and can achieve a 180-degree phase-shift. A proof-of-concept prototype with COTS was designed, simulated and measured, and we could show the feasibility and challenges of the techniques presented. For future works, an integrated circuit design is planned to address the high-frequency design challenges of the system, such as broad-bandwidth track-and-hold circuits.

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