A Cost-Efficient 28 GHz Integrated Antenna Array with Full Impedance Matrix Characterization for 5G NR

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***Abstract*— A 2x2 integrated antenna array operating at 28 GHz with 4 GHz bandwidth is presented. Conventional PCB technology is used to realize the antenna board, with low fabrication cost by minimizing the number of layers and vias. To overcome limited bandwidth and high mutual coupling, several techniques are used: proximity coupled feedings, slotted patches, and defected ground. The S-matrix and radiation patterns of the standalone antenna prototype are measured before being attached to the IC. The performed S-matrix measurement is a very first of a kind among so far reported integrated arrays at 28 GHz. The measurements confirm a mutual coupling level less than -12 dB. This characterization is used to estimate the performance of the driving power amplifiers. The analysis confirms that the antenna array is well-matched to the IC output, and as a result, the performance of the array does not degrade under beam scanning. The integrated antenna can be used as a tile module to construct larger arrays in arbitrary configurations.**

***Index Terms*—Beam-Forming, Antenna-in-Package, integrated antenna, mm-waves measurements, load pull.**

I. Introduction

Antenna-in-Package (AiP) has been widely adopted by chip manufacturers to develop highly integrated antenna systems, currently in high-demand with 5G deployment. AiP is very attractive as it offers the best balance between size, performance and cost [1]-[3]. The performance improves by embedding the antenna in the package, which reduces the overall interconnect loss [1]. The cost, however, depends on the chosen substrate technology, which can be printed circuit board (PCB) [2],[4]-[6], low-temperature co-fired ceramic (LTCC) substrate [7], glass substrate [8] or organic built-up substrate [1],[9]. Generally, the most cost-efficient approach is to use conventional PCB technology, especially if a small number of dielectric layers are used.

In this paper, we present a detailed antenna design realized with conventional PCB technology. Since stack-ups for AiPs must contain structures for both antenna and IC connectivity, some additional layers are used to implement low-frequency traces. In contrast to the designs in [5],[9], that used in total twelve and fourteen metal layer substrates, respectively, we used a simple stack-up with only two core layers attached by a prepreg layer, simplifying fabrication and lowering costs. The manufacturing costs are further reduced by only employing througstackh-hole and blind vias, completely avoiding back-drilling, in contrast with [11].

The introduced array would be used in combination with a four-channel analog beam-forming transceiver IC. Estimating the performance of the power amplifiers (PAs), while they are integrated with the antenna array, motivated us to measure the impedance matrix of the array. Although these measurements

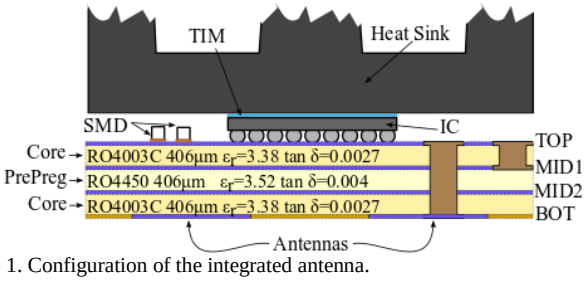
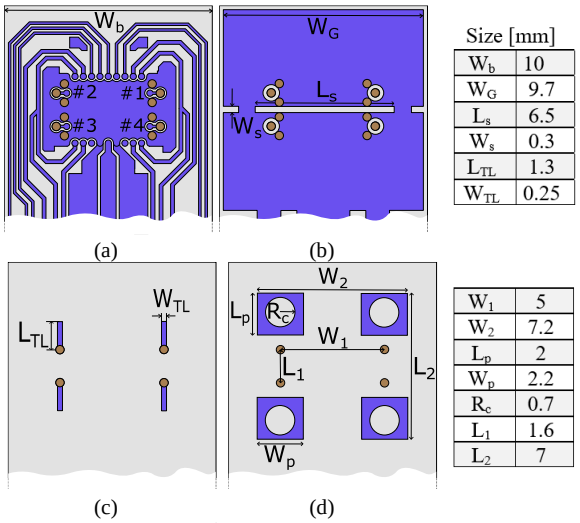


Fig. 1. Configuration of the integrated antenna.



Size [mm]	
W_b	10
W_G	9.7
L_s	6.5
W_s	0.3
L_{TL}	1.3
W_{TL}	0.25

W_1	5
W_2	7.2
L_p	2
W_p	2.2
R_c	0.7
L_1	1.6
L_2	7

Fig. 2. Topology and size of the antenna board, indicating metal layers and vias, (a) top layer, (b) first middle layer, (c) second middle layer, (d) bottom layer.

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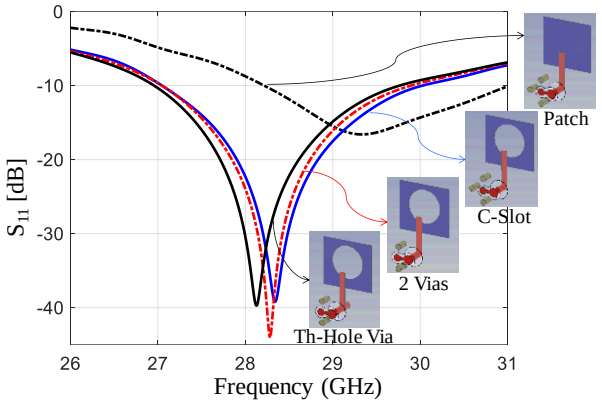


Fig. 3. Step-by-step design of the integrated antenna and its connection to the IC RF I/O. The design starts with an L-probe fed patch and ends with the patch with a circular slot, with minimum number of vias and avoiding back drilled vias.

at first sight may seem quite trivial, in literature no reported full array characterization at 28 GHz for verifying the AiP performance without IC can be found. Only a single element was characterized before in [1] and [14]. For the first time, the scattering matrix, including reflection coefficients and mutual coupling levels, of a standalone antenna array, without being attached to the IC, is fully characterized in this frequency range.

The organization of this paper is as follows. In Section II, the problem definition is given. The antenna design is presented in Section III. Section IV presents the fabricated prototype and measurement results, which are then used for an antenna-PA co-analysis in Section V.

II. Problem Definition

The goal is of this work to realize a cost-efficient and high-performance modular integrated antenna array at 28 GHz, with both Base Transceiver Station (BTS) and handset 5G communication application capabilities. In order to find an optimum balance between performance and cost, many issues need to be studied and characterized in a holistic manner during the design and development phases of the integrated antenna. In section III, we present a detailed design addressing all the following categorized challenges.

A. Antenna type and array configuration

First of all, our goal is to design a tile beam-forming antenna module to be used also in the development of larger planar arrays. Therefore, in contrast to the endfire radiating antennas in [4],[16] that are only suitable for handset applications, the antenna has to radiate to broadside. Therefore, a microstrip patch is a proper antenna type, also because it is compatible with the single ended RF I/Os of the driving IC of [11].

In addition, to achieve classical beam-forming, the array elements are chosen to be identical and with very low mutual coupling. However, we use a 2×2 array configuration with perfect symmetry with respect to both E and H planes in order to have similar beam steering characteristics in the four quadrants. Fortunately, the phase shifting ability of the driving IC supports this idea, compensating the 180° phase difference between elements.

B. Integration with IC

Since the antenna elements are driven by a four-channel analog beam-forming transceiver IC, the antennas should be optimized for both transmit and receive mode. Not only the output (input) impedance of each channel / port in these cases is different, but also the beam-forming procedure changes the active impedances of the antenna elements. Therefore, a co-analysis using load-pull measurement data of the IC is required.

As shown in Fig. 1, the wafer-level-chip-scale-packaged (WLCSP) IC is connected to the substrate using solder bumps realizing low interconnection loss transitions, which is very critical in mm-waves. A heat-sink is needed for cooling the transceiver IC.

C. AiP board and its fabrication

The board contains antenna elements and their feeding lines, also the IC and its connections. This two kind of structures must be electromagnetically isolated. To avoid mutual coupling between the antennas and the heat-sink, the antennas must radiate towards the other side of the substrate, in contrast to [13], where the antennas radiate towards the same side.

Another practical point to consider is the thermomechanical integrity. This feature has been addressed by choosing a symmetric stack-up substrate based on Rogers RO4003C material, which not only is a low-loss substrate but also has an expansion coefficient very similar to that of copper. This allows the material to exhibit excellent dimensional stability versus temperature variations.

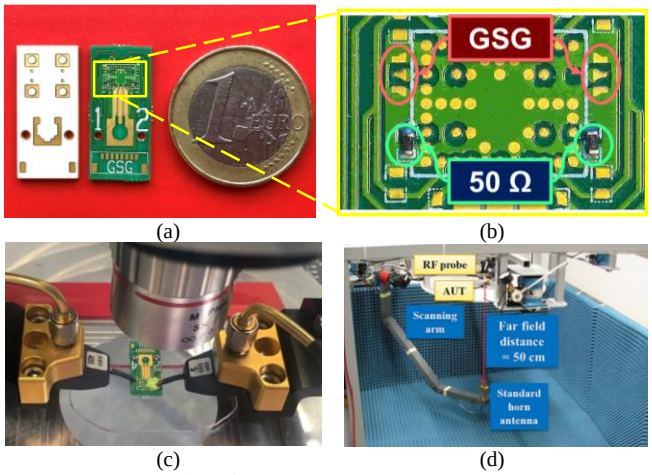
In addition, to cope with conventional PCB technology limitations, the design has the following constraints: a minimum via diameter of 250 µm, a feasible aspect ratio of 1:8, and the number of vias is kept as low as possible.

III. Antenna Topology

Fig. 2 shows the geometry of the proposed 2×2 antenna array, based on a proximity coupled L-probe fed patch antenna [16], which is wideband and has high gain. It was designed in a four-layer PCB stack-up, which comprises two 406 µm thick core substrates, attached by a 406 µm thick prepreg of RO4450. Its permittivity and tangent δ are approximately 3.52 and 0.004, respectively. The core material is RO4003C with a permittivity and tangent δ of 3.38 and 0.0027, respectively. The top and bottom copper layers are 25 µm thick and gold finished, while the intermediate copper layers are 20 µm thick. The total thickness of the board is 1.3 mm.

The initial design in Fig. 3 is a 2×2.2 mm^2 rectangular patch on the bottom layer, fed by a 1.6×0.25 mm^2 L-probe placed on the second middle layer, with the ground for the patches on the first middle layer. In addition, to minimize the number of layers, the first middle layer acts as ground for the low-frequency traces as well. It also isolates the antenna from non-radiating parts. The top layer contains the low-frequency structures for IC connectivity and a grounded co-planar waveguide (GCPW) to connect the IC RF I/O to a SMPM connector. Therefore, the layout of the top layer depends on the IC pinning, while the other three layers are used for the antenna structure.

Fig. 3 shows the step-by-step design procedure. To reduce



(a) (b) (c) (d)

Fig. 4. a) Both sides of the fabricated antenna board, b) the GSG pads and 50 Ω loads in the enlarged picture, c) probe-based set up, d) mm-wave anechoic chamber [10].

TABLE I
COMPARISON WITH REPORTED INTEGRATED 28 GHZ ANTENNAS

Ref.	Freq. [GHz]	No. of layers/Antennas / Vias	Pol. ɣ	Original [S] Measurement	Fab. Tech.
[1]	26.7-30	14 / 64 / many	D	N	OBS+
[2]	28.5-30.5	4 / 32/ many	S	N	PCB
[4]	26.3-29.75	10 / 4/ many	S	N	PCB
[5]	28-32	12 / 64/ many	S	N	PCB
[7]	26.3-29.8	11 / 16/ many	S	N	LTCC
[9]	30.3-31	14 / 16/ many	D	N	OBS
[21]	28-29.6	8 / 8/ many	D	N*	PCB
This work	**25.8-29.8**	**4 / 4 / (3 per element)**	**S**	**Y**	**PCB**

+ : organic built-up substrate , ɣ : Single/ Double
* In [21] a test package is designed and measured using a GSG probe, but this test package is different from the original AiP structure.

the size, a circular slot is implemented in the rectangular patch. This circular slot in combination with the proximity coupled feeding leads to wideband performance. This approach is simpler and more reliable than using the technique of increasing the number of layers, or the technique of using an air cavity, as was done in [1].

Since the antennas are placed at the bottom, while the IC is placed at the top of the AiP board, the RF signals must be routed through vertical transitions supported by multiple vias. This may affect the antenna impedance matching and potentially excite parallel-plate modes [9]. Therefore, the antenna and the transition from IC RF I/O to the antenna were jointly designed. To minimize the number of vias, the signal is directly transferred to the second middle layer, in contrast to [2],[5] where a CPW line is used in the transfer. The transition was optimized to minimize the number of vias and to avoid back-drilling. Fig. 3 shows the effects of these modifications.

In the next step, a half-wavelength spaced 2×2 array was designed based on the antenna element described above. The unconventional but symmetric array configuration, in which the bottom-two elements are mirrored in H-plane, is fully in line with the IC, which electronically compensates for the 180° phase difference. To reduce mutual coupling between the elements a defected ground is used, as in [12]. This is in contrast to [1], [9], [11] where fence cubes surround the patches. This method was chosen for simplicity and low fabrication cost.

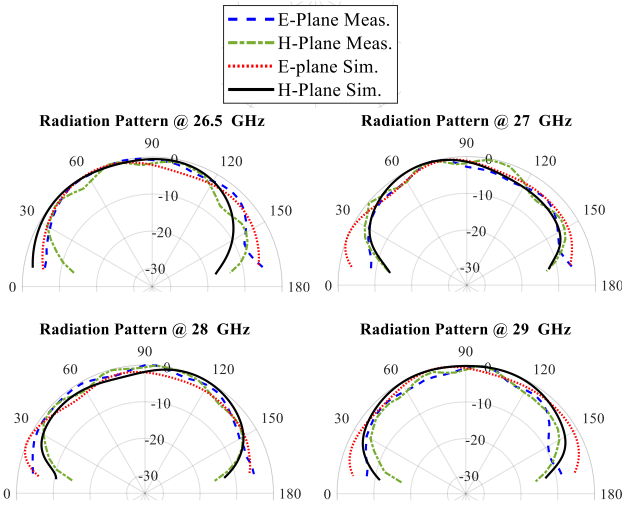


Fig. 5. Measured and simulated element radiation patterns.

Since the polarization of the patches is linear and vertical, a horizontal slot in the ground is sufficient to achieve the reduced mutual coupling, as pictured in Fig. 2(b). The antenna parameters, its dimensions and the numbering of the elements are indicated in Fig. 2. The finalized tile is 10×23 mm2 large. It is extended on one edge, while keeping the antenna array at the opposite side. The extra area is used to fit the connectivity components of the IC in the board.

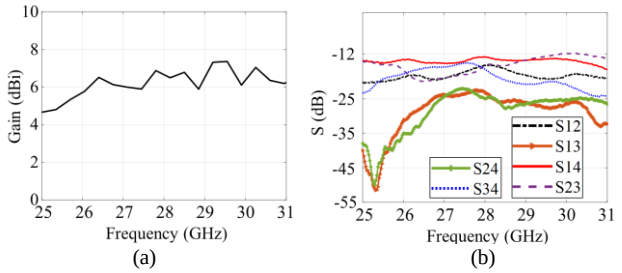
IV. REALIZATION AND MEASUREMENTS

Fig. 4(a) exhibits a photograph of the fabricated antenna array prototype. To measure the fabricated array without the IC in a probe-based antenna chamber, two sets of pads are included into the design to support simultaneously GSG-400 µm probes. In addition, the other two RF I/Os are terminated with 50 Ω SMD resistors (see Fig. 4 (b)).

The full S-matrix and embedded radiation pattern measurements were done in the KU Leuven antenna lab using the mm-wave antenna measurement set up, as developed for far-field 60-GHz measurements [10].

Using the automated rotating arm, as shown in Fig. 4 (d), the embedded radiation pattern of each element was individually measured. Since the radiation patterns near horizon are mostly affected by set-up interference, the existing metal disk, on which the antenna is mounted during the measurements, has been included into the simulation. Both the E and H plane measured results are in good agreement with simulations, as shown in Fig. 5. Fig. 6(a) displays the simulated embedded element gain, which is higher than 5.5 dBi in the frequency range of 26 to 30 GHz.

Fig. 4(c) shows the S-parameter measurement set-up. During the measurements two GSG probes with a pitch of 400 µm land on the included pads, connecting the antenna elements to the vector network analyzer. The measurement system was calibrated up to the probe-tips using SOLT standards. The measured and simulated reflection coefficients are in good agreement, as Fig. 7 shows. The measured -10 dB bandwidth of the antenna elements is from 25.8 to 29.8 GHz (14.4 % with a center frequency of 27.8 GHz).



(a) (b)

Fig. 6. a) Simulated element gain in the array, b) Measured mutual coupling between elements.

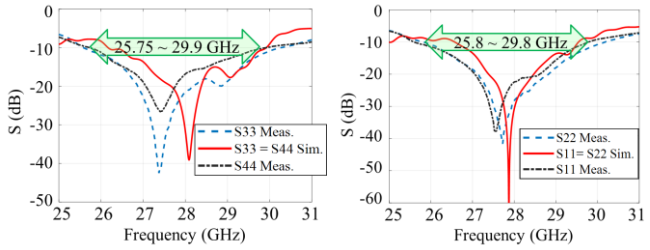
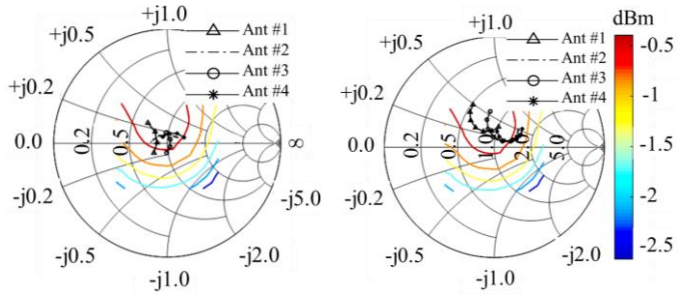


Fig. 7. Reflection coefficient of the elements.



(a) (b)

Fig. 8. Active impedances of the antenna array elements overlaying with the normalized IC output power contours, achieved from a load-pull measurement. Scan angles a) $0^0 < Az < 30^o$ & $El = 0^o$, b) $0^0 < El < 30^o$ & $Az = 0^o$.

As two probes land simultaneously, the proposed measurement setup allows the characterization of mutual coupling between the elements. The measured mutual coupling levels are plotted in Fig. 6 (b), proving that the coupling level is less than -12 dB across the whole frequency range. The highest values are seen for S_{14} and S_{23}, which corresponds to mutual coupling between elements in a column. As seen from the S_{13} and S_{24}, the diagonal elements are almost isolated with mutual couplings less than -23 dB.

Table I compares the proposed integrated antenna with the previously reported arrays in this frequency range. A reasonable bandwidth is achieved with less layers and vias, resulting in cost reduction. In addition, as mentioned before, we measured the full S-matrix of the array for the first time.

V. Co-Analysis of the Integrated Antenna Array

Since the antenna is to be connected to the transceiver IC, in this section, a co-analysis of the AiP using the measurement data of the driving IC and the antenna array is presented.

The IC performance, especially in the transmit mode, is highly dependent on the antenna representative load at the IC channel outputs. This stems from the fact that the PA performance depends on its output load. Therefore, although IC and antenna are designed to be matched to 50 Ω, due to mutual coupling, the active impedance of the antenna, and consequently the PA output, might deviate from the optimal conditions when the antenna scans. As a result, the overall array performance might degrade. Therefore, a co-analysis of the antenna-IC combination is needed. If the active circuit schematic is available to the active antenna designer, this can be done at circuit level, where the active circuit and the antenna are simulated simultaneously, using available CAD tools [17]. However, this is computationally not feasible, since a transceiver IC might include a huge number of transistors in each channel.

In [18]-[20] efficient co-analysis methods were proposed for evaluating performance of an active circuit in the presence of an antenna array. The developed methods do not suffer from the computational complexity when using CAD tools. The methods can be used both in the design stage, using simulation data of the array, and in the experimental phase, using measured antenna array data. The latter yields more accurate results, since it includes all the manufacturing tolerances. Using the same idea, here we employ a top-level analysis technique, where load-pull measurement data of the IC are captured to perform a co-analysis of the antenna-IC interactions, and to derive the antenna array design criteria.

The load-pull contours in Fig. 8, which are provided by the manufacturer (not publically available), represent the normalized PA output power versus its load in a Smith chart. Assuming that the IC channel characteristics are identical, the load-pull measurements are performed for one channel. The measured S-parameters of the antenna array have been used in the active impedance calculation.

Fig. 8(a) and (b) show the overlay of the active impedances at 28 GHz of each antenna element, with load-pull contour plots of the IC channel normalized output power. The plots reveal that the IC output power does not vary significantly if the antenna array scans towards azimuth and elevation scan angles of $0^0 < Az, El < 30^o$. In the extreme cases, the IC output power drops by less than 0.5 dB. This analysis confirms that the antenna array does not affect the IC output dramatically, and as a result, the performance of the antenna array under beam scanning does not degrade significantly. It is worth saying that if the scanning angle range increases, the IC performance deviates from the optimal operation and needs to be considered in the prediction of the antenna array performance.

VI. Conclusion

In this paper, we demonstrated a very cost efficient integrated antenna array at 28 GHz. The step-by-step design of this four-layer PCB antenna was presented. The impedance and radiation pattern of the antenna were evaluated in a mm-wave anechoic chamber. For the first time, a full S-matrix measurement was performed, showing a bandwidth of 4 GHz and mutual coupling levels less than -12 dB. In addition, measured array results were combined with measured load-pull results of the driving power amplifiers to assess how the interconnections affect the power amplifier performance.

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