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A 15-43.5 GHz Switched-Bit Phase Shifter for 5G Mobile Handsets

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Abstract—In this work, a broadband 15-43.5 GHz phase-shifter (PS) for 5G mobile applications is presented. To achieve broadband operation, the PS construction is based on all-pass networks (APNs). The proposed design was implemented in 0.25 μm BiCMOS and achieved an insertion loss (IL) of 9.5 ± 0.3 dB at 27 GHz and 13.2 ± 0.4 dB at 40 GHz, allowing operation in both 24-30 GHz and 37-43.5 GHz 5G bands.

Index Terms—5G, all-pass networks (APNs), beamforming, phase-array transceivers, phase-shifter (PS).

I. INTRODUCTION

PHASE-SHIFTERS (PSs) are a critical block of any phased-array systems, which in turn are becoming ubiquitous technology with the release of 5G systems, both for base-stations and mobile handsets [1]. While the former requires a large number of antenna elements, the latter allows just a few elements in the array, due to physical space and power constraints. The smaller number of antenna elements relaxes the specifications for phase-shifting blocks, where 45° resolution appears to be enough to provide reasonable scan coverage [2], [3]. Fig. 1(a) shows the radiation patterns of a 2×2 antenna array using a 45° step phase-shifting element. Notice that, by changing the reference path, as pictured in Fig. 1(b) and Fig. 1(c), a 2 bit, 45° phase-shifter is sufficient to provide a $\pm 60^\circ$ scan range under 3 dB gain variation.

Lowering the requirements on resolution allow us to pursue complete coverage of the large 5G spectrum. Therefore, to address the two main 5G bands (24-30 GHz and 37-43.5 GHz), this work presents a broad-band, 2-bit, 45° resolution phase-shifter. The proposed design uses all-pass networks (APNs) to achieve the broadband requirements, since APNs showed excellent bandwidth performance in lower-frequency designs [4], but were little explored in mm-waves, due to prohibitive synthesis values. Recently the APN synthesis at mm-waves has been tackled in [5] using a linear-phase synthesis approach, which will be applied here in a different phase-shifter topology to reduce area while compromising the losses.

II. PHASE-SHIFTER DESIGN

The proposed phase-shifter is pictured in Fig. 2. Since the resolution is quite coarse, a switched-type phase-shifter

Fig. 1. (a) Simulated array patterns under 45° resolution PS, (b) Negative scan angle with top element leading and (c) Positive scan angle with top element lagging.

Fig. 2. Block diagram of the proposed phase-shifter.

(STPS) approach is suitable, as it does not require a large numbers of cascading stages, which potentially leads to high insertion losses. To address the area challenge from [5], a traditional switched-bit architecture was used, since large part of the area in [5] was used to route the SP4T to the networks. The switched-bit approach reduced this routing with the cost of an extra switch and two networks within the signal path.

The APN switched-bit PS was designed using NXP's 0.25 μm SiGe:C BiCMOS technology with a peak f_T/f_{MAX} of 216/177 GHz [6]. The technology supports six metal layers and Metal-oxide-Metal (MIM) capacitors. A 50 Ω microstrip line using the uppermost and undermost metal layers was used with $h \approx 14$ μm and $W \approx 20$ μm .

To synthesize the APNs, the procedure from [5] was used. The choice for a 4th order network was done to achieve a $\pm 2^\circ$ phase variation within the selected bandwidth of 20-45 GHz. The chosen APN schematic is pictured in Fig. 3a. To simplify the overall design, both stages used the same reference path (APN3). The synthesized values were obtained using the synthesis parameters: $n = 4$, $\tau = 1$ and $\delta = 0.01$ rad, the phase offsets $\phi_{os} = 90^\circ, 45^\circ, 0^\circ$ and network parameters

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Fig. 3. Schematic of (a) APNs, (b) SPDT switch and (c) DPDT switch.

TABLE I

COMPONENT VALUES FROM SYNTHESIS, L AND M IN pH, C IN fF

	ϕ_{os}	Q_{pole}	L_{a1}	M_1	C_{a1}	C_{b1}	L_{a2}	L_{b2}	C_{a2}	C_{b2}
APN1	90°	0.55	614.4	336.6	55.5	760.9	276.1	113.6	90.8	281.6
APN2	45°	0.55	437.8	234.8	40.6	538.1	253.5	108.6	86.8	243.5
APN3	0°	0.60	282.4	159.9	24.5	353.8	301.5	92.9	74.3	637.4

$Z_o = 50\Omega$ and $f_{scale} = 30$ GHz. The Q_{pole} factor was adjusted amongst different networks to achieve bandwidth alignment, as explained in [5]. The resulting values for the APNs are given on Table I. To compensate inductor parasitics, specially for the larger inductors (L_{a1}), the intra-winding capacitance and the capacitance to the substrate were absorbed into C_{a1} . Such procedure is not as critical for L_{a2} and L_{b2} , as their inductances are quite low, having very small parasitics. Since high-Q MiM capacitors are available, their parasitics are negligible.

The schematic of both SPDT and DPDT are pictured in Fig. 3(a) and 3(b), respectively. In order to provide higher isolation between ports, a shunt-series configuration of MOS transistors were used, with channel length of $0.2 \mu m$, where the series transistor (M_{se}) is optimized to reduce overall insertion loss, while the shunt transistor (M_{sh}) improves

Fig. 4. On-chip photograph of the all-pass network based switched-type phase-shifter.

Fig. 5. Measured S-parameters of the phase-shifter.

isolation. Inductors L_1 , L_2 and L_3 tune the node capacitances. To guarantee a large V_{gs} during both on and off states, the source and drain nodes of all transistors were biased with $V_b = 2.5$ V and the gate was switched from 0 to 5 V, having always $V_{gs} = 2.5$ V. DC block capacitor $C_2 = 1$ pF guarantees that for the shunt MOS. Biasing is delivered by 10 k Ω resistors to avoid RF-leakage.

The on-chip photograph of the phase-shifter can be seen in Fig. 4. The total area without the pads is 0.37×0.75 mm² (≈ 0.28 mm²).

III. MEASUREMENT RESULTS

The proposed phase-shifter was measured using the network analyzer Agilent 67 GHz PNA E8361A with a Cascade Microtech Summit 12000B-S probe station. G-S-G probes with $125 \mu m$ pitch were used and were calibrated using a SOLT approach. The effects of the RF pads were de-embedded from the measurement using a symmetrical T-parameter matrix obtained from a back-to-back structure placed on the wafer.

The measured S-parameters of the phase-shifter for all settings is pictured in Fig. 5. S_{21} has a large variation across the band, from -6 dB up to -18 dB, however, variation within phase settings is very small. At mid-band (25.5 GHz), the

Fig. 6. Measured insertion phase, phase difference and phase error for all setting of the phase-shifter.

losses are 9 ± 0.15 dB. The total RMS gain error, also pictured in Fig. 5, is kept under 0.5 dB up to 47 GHz. S_{11} and S_{22} are kept < -10 dB up to 53 GHz.

The phase characteristics are pictured in Fig. 6. The phase states were obtained w.r.t. a reference state (11) and the phase difference between other states and the reference is also plot in Fig. 6. Notice a clear swing around the ideal phase state values (45° , 90° and 135°). The phase-error with respect to their ideal phase states values is also shown. Notice that the phase error is kept under 10° over the 15-43.5 GHz frequency range. The RMS phase error, also pictured in Fig. 6, is kept under 5° from 15-43.5 GHz.

Finally, a zoom within the main 5G bands (24-30 and 37-43.5 GHz) for both S_{21} and phase states is presented in Fig. 7. Although both S_{21} and phase states present large variations over the 15-43.5 GHz, when a smaller bandwidth is zoomed one can notice a very small variation within those bands. For both bands, a variation of ≈ 2.5 dB across the bands, with a variation between different phase settings of ± 0.5 dB from 24-30 dB and ± 0.6 dB from 37-43.5 GHz. Furthermore, the phase states remain almost flat throughout the bands, allowing an uniform beamforming with low-distortion.

The performance of the proposed PS is compared with state of the art mm-wave phase-shifters in Table III. The proposed PS achieved the highest bandwidth, in percentage, reported for mm-wave 5G applications in the literature. Compared to the parallel architecture from [5] lower area is achieved with the price of higher insertion loss.

IV. CONCLUSION

This paper presented a 2-bit, 45° , broad-band APN based switched-bit STPS. The proposed solution achieved a bandwidth of 15-43.5 GHz with a RMS phase error below 5° while consuming zero static power, being suitable for 5G mobile handset applications across the main 5G spectrum.

Fig. 7. Measured S_{21} and phase difference plot zoom within the main 5G bands, 24-30 GHz and 37-43.5 GHz.

TABLE II
STATE OF THE ART BROAD-BAND MM-WAVE PSS

Ref.	[3]	[7]	[5]	This work
Tech.	40 nm CMOS	0.18 μ m BiCMOS	0.25 μ m BiCMOS	0.25 μ m BiCMOS
Freq. (GHz)	22 – 36	15 – 35	14 – 50	15 – 43.5
Rel. BW (%)	49.7%	87%	136%	112.2%
Resol. ($^\circ$)	45°	22.5°	45°	45°
No. of Bits	3	4	2	2
RMS Ph. Err. ($^\circ$)	$< 12.8^\circ$	$< 13^\circ$	$< 9.7^\circ$	$< 5^\circ$
RMS Gain Err. (dB)	< 0.6	< 2.2	< 0.94	< 0.5
IL (dB)	5 to 8	-5 to 13.5	5 to 16	6 to 18
Loss mid. band (dB)	7 ± 1	4 ± 2	7.2 ± 0.3	9 ± 0.15
Return Loss (dB)	< -7	N/A	< -7	< -10
P_{DC} (mW)	0	25.2	0	0
Area (mm^2)	0.132	0.19	0.48	0.28

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