A 14-50 GHz Phase Shifter With All Pass Networks for 5G Mobile Applications

Eduardo V. P. Anjos, *Student Member, IEEE,* Dominique M. M.-P. Schreurs, *Fellow, IEEE,* Guy A. E. Vandenbosch, *Fellow, IEEE,* and Marcel Geurts

***Abstract*—In this work, an ultra-broadband phase-shifter (PS) with a 14-50 GHz bandwidth (defined by a phase-error below 1/2 LSB) is presented to address the multi-band requirements of 5G milimeter-wave (mm-wave) systems. The PS construction is based on all-pass networks (APNs), which have shown broad bandwidth capabilities in a lower frequency range. Aiming towards 5G mobile applications, the proposed 2-bit, 45° phase resolution PS was implemented in $0.25\ \mu m$ BiCMOS, manufactured and measured, achieving an insertion loss (IL) of 7.4 $\pm$ 0.26 dB at 28 GHz and 10 $\pm$ 0.22 dB at 39 GHz, with an RMS gain and phase error $<$ 0.27 dB and $< 4^\circ$ from 24-30 GHz, respectively, and $<$ 0.33 dB and $< 6^\circ$ from 37-43.5 GHz, demonstrating its capabilities to cover the 5G mm-wave spectrum.**

***Index Terms*—All-pass networks (APN), beamforming, broadband, milimeter-wave (mm-wave), multi-band, phase-array transceivers, switched-type phase-shifter (STPS), 5G.**

I. Introduction

THE 5th Generation of telecommunication systems (5G) is expected to roll out in the upcoming years to the general public. In order to achieve the expected two-fold increase in data-rate, 5G will heavily rely on millimeter-wave (mm-waves) technology [1], [2]. However, the frequency band is not yet a consensus. As different regions have different spectrum availability, different bands have been rolled out for auction across the globe. For example, the EU has defined the 24.5-27.5 GHz bandwidth [3], while the FCC, from the US, has defined several bands from 24.25 GHz to 28.5 GHz, as well as a higher one from 37-40 GHz [4]. Overall, two main bands have been delimited, 24.25-29.5 GHz and 37-43.5 GHz, while spectrum discussions are still ongoing [5, pp. 6-8].

The exploration of the mm-wave spectrum comes with challenges, such as high propagation losses and costly components, and the key enabling technologies to overcome those challenges are the implementation of antenna phased-arrays and beamforming [6], [7]. In particular, implementations of integrated phased-array transceivers with analog beamforming capabilities using high-volume fabrication processes such as SiGe [8] and even CMOS [9] have been presented, paving the way of mm-wave antenna arrays on commercial 5G applications [10].

This project has received funding from the European Union's Horizon 2020 research and innovation programme under the Marie Sklodowska-Curie grant agreement No. 721732.

Eduardo V. P. Anjos, Dominique M. M.-P. Schreurs and Guy A. E. Vandenbosch are with TELEMIC, Department of Electrical Engineering, KU Leuven, Leuven 3001, Belgium (E-mail: eduardo.anjos@kuleuven.be).

Marcel Geurts is with NXP Semiconductors, 6534AE, Nijmegen, The Netherlands.

Manuscript received January 7, 2019; revised .

The basic building-block for analog beamforming systems is the phase-shifter (PS), and while many state-of-the-art (SOTA) solutions [11]–[13] using standard design approaches provide low-loss, high-resolution and zero static power consumption, they fall short with respect to bandwidth, leaving a large part of the 5G spectrum uncovered. Therefore, a shift in design approach is needed to address the bandwidth challenge.

One possible solution to cover all required bands is the use of All-Pass Networks (APNs). They have been proven to be quite effective with respect to bandwidth on a lower frequency range, up to few GHz [9], [14]–[21]. Although the use of APNs dates back to the 1950's, its application for phase-arrays was initially proposed by Adler and Popovich [14] in the 1990's, where a 3-8 GHz bandwidth switched type phase-shifter (STPS) with 45° resolution was presented. Tang and Mouthaan extensively explored higher order networks [15]–[17], focusing on covering one to two octaves of bandwidth in the low GHz frequency range. These works implemented the APN-based STPS using discrete components due to large inductances and capacitances of the networks and also due to high Q components available off-the-shelf.

The push for an integrated APN STPS design was recently done in [18], [19], [22], initially at S and C-bands using GaAs [22] and then using $0.18\ \mu m$ CMOS technology [18], [19] covering a bandwidth from 1.62-3.89 GHz. However, due to lossy switches and low-Q inductors in CMOS, an insertion loss (IL) greater than 12 dB for the latter was achieved. As mm-wave applications require integrated solutions, the conventional APN STPS approach does not seem attractive and thus they were not attempted, to the best knowledge of the authors. Nonetheless, the benefits of APNs in mm-waves were explored in generating quadrature vectors on a vector-sum block in [9], [20], [21], successfully covering X, Ku and K band [9], and further explored at V band [20]. Furthermore, the Ka band vector-sum block using APNs in [21] achieved a 15-35 GHz bandwidth, much larger when compared to standard STPS solutions, which demonstrates APNs bandwidth capabilities at mm-waves.

In this work, we present a STPS for 5G mobile applications using APNs. Due to particular aspects of the intended application, a 2-bit, 45° resolution PS was implemented using an innovating architecture: four APNs in parallel with SP4T switches. The relaxed resolution requirements of the specific application allowed us to push the SOTA with respect to bandwidth, achieving a 14-50 GHz bandwidth with a measured RMS phase error of less than 9.5°. To enable such PS configuration, we explore the linear-phase APN synthesis procedure

developed by Herrmann [23] and Challener [24] and introduce a bandwidth alignment procedure to make sure all APNs cover the same frequency range. Also, it should be highlighted that for the first time a variable to control feasibility was employed as a synthesis parameter to allow implementation of APNs at mm-wave frequencies.

This manuscript is organized as follows. Section II discusses the specifications for 5G mobile PSs. Section III reviews the linear-phase All-Pass Network synthesis, revisits Herrmann's work, which is rather outdated and not available in English, and introduces the novel bandwidth alignment procedure proposed by the authors. Section IV describes the PS design, and measurement results are presented in Section V, followed by a conclusion in Section VI.

II. Specifications for 5G Mobile Application PSs

A. Phase Resolution

The use of antenna-arrays and beamforming is not only expected in base-station applications, but also at the user side as a way to radiate more power. In mobile handsets, due to limited availability of space and power, the number of antenna elements are expected to be much smaller than base station arrays [25]–[27]. For example, in [25] a 2×4 antenna module using a 45° resolution PS in CMOS technology was presented. The array can be further reduced when using SiGe technology, as it has higher power capabilities when compared to CMOS, where similar radiated power values were obtained in using a 2×2 antenna array [27].

Such smaller array has quite a broad beamwidth, which does not require fine resolution steps to cover a wide scan range. Fig. 1(a) shows the simulated normalized antenna patterns for a 2×2 array of ideal patches using 45° phase-shifting steps. Notice that a $\pm 60^\circ$ scan range is achieved under a 3 dB gain variation. Furthermore, a 180° step is not required for such array configuration, since negative scan-angle values can be achieved by changing the reference path, as shown in Fig. 1(b) and Fig. 1(c), highlighting that 2 bits are sufficient for a $\pm 60^\circ$ scan range coverage.

B. PS Topology

Another crucial aspect for mobile applications is the power consumption, and therefore active PS configurations, such as Vector Modulators (VM) [9], [20], [21] are not suitable for mobile handsets. Passive PSs have zero static power consumption, but generally higher IL and larger area. Since high IL typically require compensation, the IL represents indirectly power consumption for passive PSs. Two main approaches are typically used to implement passive PSs: 1) reflection type phase shifters (RTPS) and 2) switched type phase shifters (STPS) [28].

RTPS, shown in Fig. 2(a), operate by means of splitting the signal with a quadrature hybrid coupler, reflecting the signal using a reactive impedance Z_R and combining both reflected signals at the output. The phase-shift is achieved by varying the reactive impedance Z_R, which has been shown to achieve a full 360° range with fine resolution and low loss

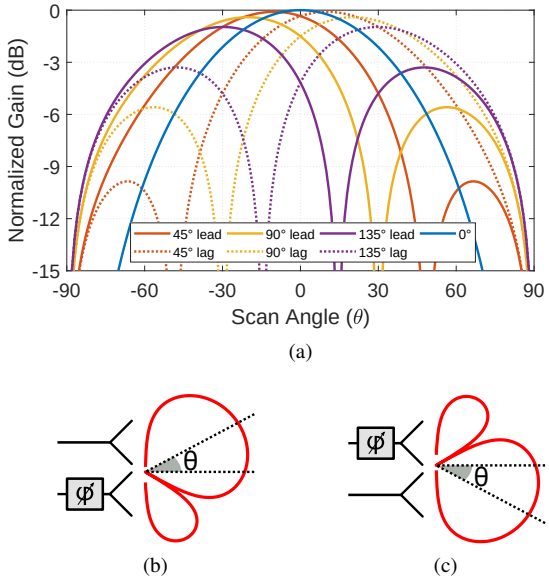


Fig. 1. (a) Simulated array patterns under 45° resolution PS, (b) Negative scan angle with top element leading and (c) Positive scan angle with top element lagging.

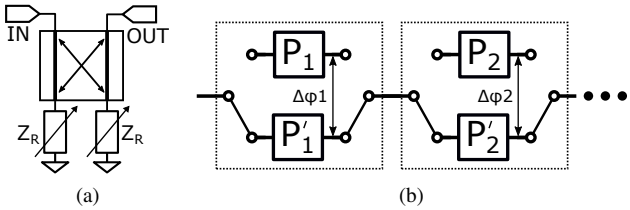


Fig. 2. Passive PS topologies (a) RTPS and (b) STPS.

[13]. However, their bandwidth is limited by the hybrid coupler performance.

STPS, shown in Fig. 2(b), work by switching between different signal paths with a phase-difference between those paths [11], [29]–[32]. The increase of phase resolution in STPS is done by cascading many stages, leading to higher losses and an increase in area. Thus, STPS are more suitable for lower resolution applications. An important aspect is that, since switches are typically broadband [33], the STPS bandwidth is typically limited by the implementation method used for the phase-shifting paths. Conventional methods use high-pass/low-pass (HP-LP) filters or bypass/low-pass (ByP-LP) filters, which only guarantees the phase-shift for a single frequency. By using APNs in the phase-shifting paths, we expect to achieve broadband capabilities using STPS.

The main advantage of the conventional approaches over APNs is the ability of embedding the switch within the network [11]. By doing so, a more compact design is achieved and less switches are required. As APNs rely on a constant-impedance capability, external switches must be used to allow path selection, which can lead to larger area and higher losses, even for a 2-bit STPS.

Considering the STPS topology pictured in Fig. 2(b) using APNs, the signal path would go through 3 switches (2 back-to-back switches can be combined in a DPDT) and 2 networks, where each block contributes to losses. To reduce IL, we

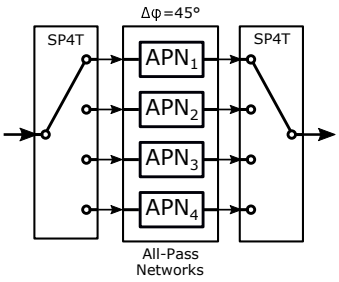


Fig. 3. Block diagram of the proposed PS.

propose to parallelize the networks, as pictured in Fig. 3. This way, the signal path sees 2 switches and 1 network, greatly reducing IL. At the same time, the used area is not increased as the total number of networks is preserved. Although the proposed topology seems straightforward, traditional APN synthesis does not allow the parallelizing of networks (they synthesize a pair of networks together), thus requiring a novel synthesis approach to enable such novel architecture, discussed in Section III.

C. Wide-band vs. Dual-band PS

One could argue that a simpler way to address the 5G bandwidth requirements is the use of a switchable dual-band PS instead of a wide-band one. Although a more straightforward approach, it would require the addition of at least two extra switches in the signal path, the same problem we are aiming to solve by parallelizing the networks. Even using SOTA switches in technologies optimized for switches, such as CMOS SOI [34], at least an extra 3 dB loss would be added to the signal at mm-waves. The additional loss in the signal path introduced by switching between bands would require extra compensation by amplifiers, which in turn require more power consumption, critical for mobile applications. Furthermore, after accommodating both PSs and switches, the area savings might not be significant, even when compared to a bulkier design approach such as the use of APN. For example, by taking two SOTA $0.16\ mm^2$ PS from [13] as example, with two $0.04\ mm^2$ switches from [34], the total area would be $0.4\ mm^2$ (without counting possible interconnects) with a loss of $\approx$ 10.7 dB at 28 GHz, compared to the area of $0.48\ mm^2$ with 7.2 dB of loss from the proposed PS, trading off $0.08\ mm^2$ for 3.5 dB of IL. Furthermore, as discussions are still ongoing regarding the 5G spectrum [5], a wide-band solution is prepared to accomodate future requirements.

III. APN Synthesis

APNs (also known as constant-resistance networks) were first proposed as a phase-shifting network on a patent granted to Hodgson in 1941 [35]. The initial focus was on generating wideband phase splitting solutions for single sideband modulation systems around the late 1940's. Saraga [36] initially proposed empirical methods based on graphical solutions to generate the desired phase splitting networks. Synthesis procedures were then proposed respectively around the same time by Darlington [37] and Orchard [38], whose methods approximated the phase difference between two all-pass networks to a constant over the band of interest. By using Chebyshev polynomials, it was possible to create an equiripple phase difference profile between the two networks. Their method synthesized both networks simultaneously, given a maximum phase variation and network order, maximizing bandwidth for those inputs. It worked without any restriction on the phase characteristics of each network individually. Moreover, only real poles were obtained using either Darlington or Orchard's method. Regarding implementation, lattice networks were typically used.

A. Linear-Phase Network Synthesis

The networks proposed by Orchard and Darlington were sufficient for audio signal transmission, but the issue of a non-constraint phase, and by extent a non-uniform group delay, became a concern when video signal transmissions were attempted. To overcome this challenge, linear-phase networks were required, and in 1969, Herrmann [23] proposed a novel method to synthesize them. Herrmann's technique consisted in approximating an APN $H_{AP}(j\omega)$ by an ideal network $H_{ID}(j\omega)$, described by

$$|H_{ID}(j\omega)| = 1 \tag{1}$$

$$\angle H_{ID}(j\omega) = -(\omega\tau + \phi_{os}) \tag{2}$$

where τ is the phase slope and ϕ_{os} the phase offset. By synthesizing two networks with same phase slope and $\pi/2$ phase offset difference, a quadrature phase-splitting can be obtained. The APN $H_{AP}(j\omega)$ can be described by its poles and zeros, using $s = j\omega$,

$$H_{AP}(j\omega) = \frac{D_n(-s)}{D_n(s)} \tag{3}$$

where $D_n(s)$ is a n^{th} order Hurwitz polynomial. It can be described by

$$D_n(s) = \sum_{l=0}^{n} a_l s^l = A\prod_{k=1}^{n}(s - p_k). \tag{4}$$

The phase of the APN can be described by

$$\angle H_{AP}(j\omega) = -2\arg\{D_n(j\omega)\} \tag{5}$$

$$\angle H_{AP}(j\omega) = -2\sum_{k=0}^{n}\tan^{-1}\left(\frac{\omega - \mathrm{Im}\{p_k\}}{\mathrm{Re}\{p_k\}}\right) \tag{6}$$

By defining an approximation error function, $\varepsilon_{ph}(\omega)$, given by

$$\varepsilon_{ph}(\omega) = \angle H_{ID}(j\omega) - \angle H_{AP}(j\omega) \tag{7}$$

$$\varepsilon_{ph}(\omega) = -(\omega\tau + \phi_{os}) + 2\sum_{k=0}^{n}\tan^{-1}\left(\frac{\omega - \mathrm{Im}\{p_k\}}{\mathrm{Re}\{p_k\}}\right) \tag{8}$$

it is possible then to find solutions which minimize the error function in a Chebyshev sense within a given frequency interval $\langle\omega_L, \omega_H\rangle$. In different words, given a maximum error bound δ, where

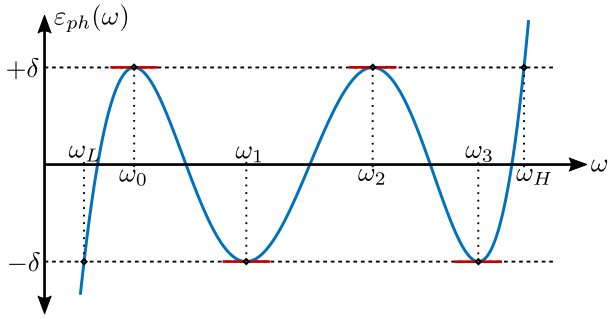


Fig. 4. Phase error characteristics for a 4^{th} order network.

$$|\varepsilon_{ph}(\omega)| \leq \delta, \qquad \omega_L \leq \omega \leq \omega_H \tag{9}$$

solutions can be found that maximize the frequency interval $\langle \omega_L, \omega_H \rangle$ [23]. Herrmann then proposes an algorithmic procedure to approximate the error function $\varepsilon_{ph}(\omega)$ given a set of initial constraints such as filter order n, phase slope τ, phase offset ϕ_{os} and a maximum error bound δ. His method relies on the equiripple characteristics of the Chebyshev approximation where $\varepsilon_{ph}(\omega)$ has n turning points for a n^{th} order polynomial. As an example, Fig. 4 pictures the characteristics of an error function for a 4^{th} order APN with four turning points.

To have an equiripple behavior of the phase error function, $\varepsilon_{ph}(\omega)$ must be bound within $\pm\delta$. Since the turning points are local maxima and minima of the function, if they are bound within $\pm\delta$, and the frequency interval limits are also bound, the error function $\varepsilon_{ph}(\omega)$ will be bound within $\pm\delta$. Furthermore, in order to a specific frequency be a turning point, the derivative of the error function must be zero at that frequency. Based on those properties, we can build a system of equations.

Considering an n^{th} order network, we can define a vector of frequency points consisting of the frequency interval limits ω_L, ω_H and the turning points ω_1 to ω_n

$$\boldsymbol{\omega} = [\omega_L, \omega_1, \omega_2, \ldots, \omega_n, \omega_H]^T \tag{10}$$

Our goal is to find the value of the poles of the APN, given by the pole vector

$$\boldsymbol{p} = [p_1, p_2, \ldots, p_n]^T \tag{11}$$

The phase error is also a function of the poles, thus the notation $\varepsilon_{ph}(\omega, \boldsymbol{p})$ will be used. The equation system can be described by

$$\varepsilon_{ph}(\omega_i, \boldsymbol{p}) = (-1)^i \delta \quad \forall\ 0 \leq i \leq n+1 \tag{12}$$

$$\frac{d}{d\omega}\left[\varepsilon_{ph}(\omega_i, \boldsymbol{p})\right] = 0 \quad \forall\ 1 \leq i \leq n, \tag{13}$$

which results in $2n+2$ equations and variables. As suggested by Herrmann, the following equation system can be solved using the Gauss-Newton method. In order to improve convergence, a good initial guess must be given for both $\boldsymbol{p}$ and $\boldsymbol{\omega}$. An effective procedure for finding initial guesses can be found in his work [23]. As mentioned before, his procedure synthesizes individual networks, which does not guarantee that multiple networks with different offsets, required to obtain a phase difference between them, will operate within same frequency range. A procedure to align their bandwidth is proposed later in this section.

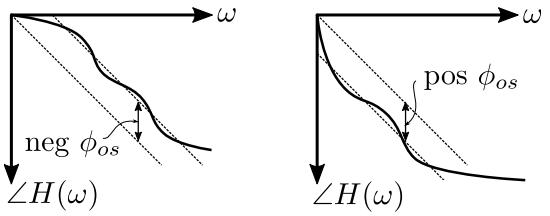


Fig. 5. Network classification due to their offset type. (a) Type 1 and (b) Type 2.

TABLE I
SUMMARY OF SYNTHESIS POSSIBILITIES W.R.T ORDER AND TYPE

Acronym	Order	Type	Chebyshev Sol.	Causal Sol.
EOT1	Even	Type 1	Unique	-
OOT1	Odd	Type 1	No	Unstable
EOT2	Even	Type 2	No	Infinite
OOT2	Odd	Type 2	Unique	-

B. Network Types and Quasi-Chebyshev Solutions

Herrmann's synthesis procedure finds the Chebyshev approximation for the error function provided that the order of the polynomial equals the number of turning points. Furthermore, Hausner and Furlani [39] have demonstrated the uniqueness of such Chebyshev solution. However, such constraint imposes limitations on the possible solutions by Herrmann's method.

As pointed out by Challener [24], the number of turning points is directly related by the type of phase offset ϕ_{os} of the network, since the phase curve has an asymptote at $-n\pi$ as $\omega \to \infty$. A negative offset ($\phi_{os} < 0$), called here a type 1 network, pictured in Fig. 5a, has always an even number of turns. A postive offset ($\phi_{os} > 0$), called here a type 2 network, pictured in Fig. 5b, has always an odd number of turns. Herrmann's method can therefore find Chebyshev approximations for Even Order Type 1 (EOT1) networks and for Odd Order Type 2 (OOT2) networks. However, in his work, he explicitly included only synthesis tables for the OOT2 case, as he claimed to achieve higher bandwidth with an lower n when compared to EOT1 networks [23]. A summary of the synthesis possibilities is shown in Table I.

Continuing the work from Herrmann, Challener [24] investigated practical aspects when implementing such networks. Odd order networks can be constructed by a cascade of 1^{st} and 2^{nd} order sections to achieve the desired pole-zero configuration. However, while 2^{nd} order sections can be implemented using unbalanced structures, 1^{st} order sections are limited to Lattice implementations. Furthermore, due to parasitic components in inductors and capacitors, it is impossible to implement a truly odd-order network, which makes even-order networks more attractive. Nonetheless, EOT1 networks face the issue of having lower bandwidth when compared to their

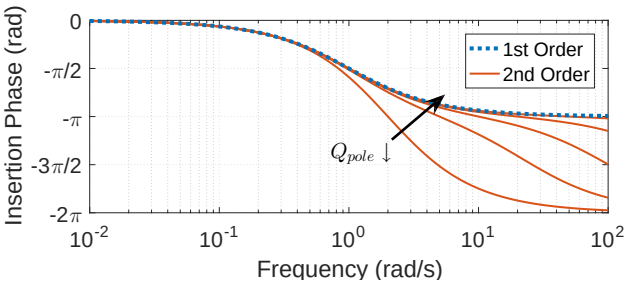


Fig. 6. Phase curve of 1^{st} and 2^{nd} order APN section for different Q_{pole}.

lower order OOT2 counterparts, which motivated Challener to investigate Even Order Type 2 (EOT2) networks. Although EOT2 networks do not have Chebyshev solutions, he noticed that it was possible to approximate the phase of an EOT2 network to a lower order OOT2 in a quasi-Chebyshev fashion, by approximating the phase behavior of an 2^{nd} order APN section to the one of a 1^{st} order section. Consider a 2^{nd} order APN section described as

$$G_{2ord}(s) = \frac{s^2 - \frac{\omega_o}{Q_{pole}}s + \omega_o^2}{s^2 + \frac{\omega_o}{Q_{pole}}s + \omega_o^2} \tag{14}$$

For higher frequencies, where $s^2 \gg \omega_o^2$, we have

$$G_{2ord}(s) \approx \frac{s^2 - \frac{\omega_o}{Q_{pole}}s}{s^2 + \frac{\omega_o}{Q_{pole}}s} = \frac{s - \frac{\omega_o}{Q_{pole}}}{s + \frac{\omega_o}{Q_{pole}}} \tag{15}$$

Thus, by making Q_{pole} very small, its higher frequency pole/zero is pushed outside the frequency interval of interest $\langle \omega_L, \omega_H \rangle$. The phase curve for 2^{nd} order sections with different Q_{pole} values vs. a 1^{st} order section is pictured in Fig. 6. Q_{pole} can then be an input to the synthesis procedure, reducing the number of variables and making the system solvable. Notice that in this case, the solutions are not strict Chebyshev approximations.

Although the effects of reducing Q_{pole} are quite positive with respect to bandwidth, it has a lower bound [24]. When implementing the 2^{nd} order APN section using magnetically coupled inductors, as pictured in Fig. 7, the use of small Q_{pole} leads to a very-high coupling coefficient k between inductors. As k is radically dependent of the technology used, a lower bound for Q_{pole} can be found when k is max:

$$Q_{pole} \geq \sqrt{\frac{1 - k_{\max}}{1 + k_{\max}}} \tag{16}$$

The most valuable takeaway from the use of Q_{pole} as a synthesis variable is the ability to control the implementation feasibility of the networks. Q_{pole} can then be adjusted to a higher value when high coupling coefficient is not available, which is the case of integrated circuit implementation. Notice that it is not possible to directly control feasibility of the networks with the Chebyshev solution from Herrmann. In this work, we also explore the use of Q_{pole} to control the central frequency of the APNs without sacrificing phase error, thus achieving bandwidth alignment.

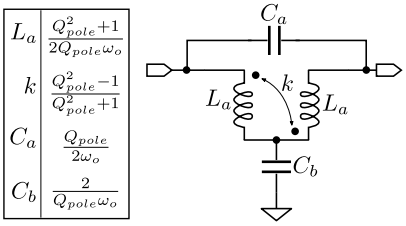


Fig. 7. 2^{nd} order APN implementation.

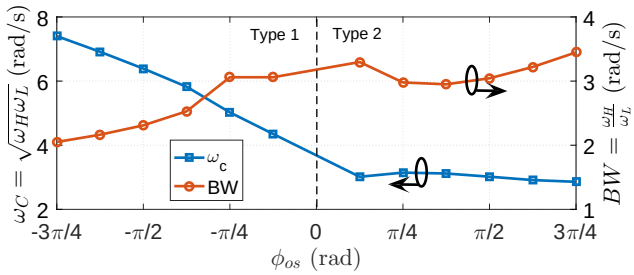


Fig. 8. Central frequency (ω_c) and bandwidth (BW) w.r.t. phase offset (ϕ_{os}) of synthesized APNs with ($n = 4, \tau = 1, \delta = 0.01\ rad, Q_{pole} = 0.25, Z_o = 1\ \Omega, f_{scale} = 1$).

C. Parallel APNs with Bandwidth Alignment

To implement the proposed PS, it is crucial that the four possible paths for the signal can cover the same frequency band. Since the presented synthesis procedure was only utilized to design a pair of networks, this issue has never been raised. Previous works only utilized one of the network types to implement the APNs (OOT2, EOT1 or EOT2). However, in our case, few issues arise: to implement a 135° phase-shift using only EOT2 networks, we would require a APN with $\phi_{os} = 3\pi/4$. Values for ϕ_{os} close to $+\pi$ require lower-frequency poles, which in turn requires very large inductors and small capacitors. In those cases, the intra-winding capacitance of the inductors is typically higher than the synthesized value, leading to unrealizable networks. On the other hand, implementing it only with EOT1 would lead to values for ϕ_{os} close to $-\pi$, requiring higher-frequency poles, and by extent very small inductors which cannot be realized in practice.

A closer inspection of the bandwidth ($BW = \omega_H/\omega_L$), central frequency ($\omega_c = \sqrt{\omega_H \omega_L}$) and phase offset ($\phi_{os}$) relationship revealed some interesting properties of the synthesized APNs. We synthesized APNs using the same parameters ($n = 4, \tau = 1, \delta = 0.01\ rad, Q_{pole} = 0.25, Z_o = 1\ \Omega, f_{scale} = 1$), and performed a sweep w.r.t. the phase offset (ϕ_{os}). The results are pictured in Fig. 8. A steady increase in central frequency was observed for type 1 networks, while type 2 networks had a more stable behavior. The BW, on the other hand, is kept stable up to $\phi_{os} = -\pi/4$, and start dropping rather fast beyond that. Therefore, to use both EOT1 and EOT2 APNs in the design, and to avoid the use of ϕ_{os} values close to $+\pi$, we selected the following values for ϕ_{os} : $[-\pi/4, 0, +\pi/4, +\pi/2]$. The remaining issue now, in order to cover the same bandwidth, is the alignment of central frequency. Since the EOT1 has a unique Chebyshev solution, it cannot be adjusted to change its central frequency. Conveniently, the other three APNs are EOT2, which have

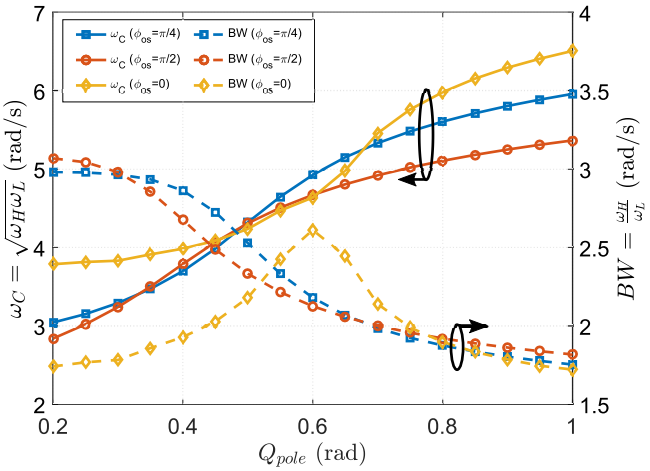


Fig. 9. Central frequency (ω_c) and bandwidth (BW) w.r.t. parameter Q_{pole} for selected phase-offsets $\phi_{os} = [0, +\pi/4, +\pi/2]$ of synthesized APNs with ($n = 4, \tau = 1, \delta = 0.01\ rad, Z_o = 1\ \Omega, f_{scale} = 1$).

Q_{pole} as an extra parameter to be tuned to align the central frequency. Fig. 9 shows how the Q_{pole} parameter affects the central frequency and bandwidth of the APNs. Notice that, as Q_{pole} goes high, the central frequency of the band goes higher as well, while inductors get smaller and capacitors larger, increasing the APNs feasibility in an integrated circuit design. However, the main drawback is the loss of bandwidth, as shown by Challener [24] and also pictured in Fig. 9. Therefore, a trade-off between bandwidth and feasibility is observed, while the phase error is kept constant. In order to synthesize the N APNs in parallel with the desired bandwidth alignment, we propose the following procedure:

1) Define the synthesis parameters n, τ, δ, filter parameters Z_o, f_{scale} and phase offsets $\phi_{os1}, \phi_{os2}, \ldots, \phi_{osN}$.
2) Select an EOT1 network (negative ϕ_{os}) as the bandwidth reference - since it has a Chebyshev solution and the parameter Q_{pole} is not available to be tuned.
3) Perform the synthesis procedure as described in Section II-A.
4) Obtain the center frequency of the reference network $\omega_{c_{ref}}$.
5) While synthesizing the subsequent $N-1$ networks, sweep Q_{pole} until $\omega_c = \omega_{c_{ref}}$, bearing in mind its lower bound from eq. 16 to allow IC implementation.
6) If after sweeping Q_{pole}, the resulting bandwidth is not sufficient, it means that the selected phase error δ is not feasible for the attempted bandwidth. Re-adjust the values and repeat from Step 1.
7) If bandwidth is sufficient, scale the resulting APNs to the desired Z_o and f_{scale}.

The proposed synthesis procedure was utilized in this work to implement the APNs of the PS, which is described in depth in the following Section.

IV. Phase-Shifter Design

The APN based STPS was designed using NXP's 0.25 μm SiGe:C BiCMOS technology with a peak $f_T/f_{\max}$ of 216/177 GHz [40]. The technology supports six metal layers and Metal-oxide-Metal (MIM) capacitors. A 50 Ω microstrip line was designed using the highest and lowest metal lines, with a height of $\approx 14\ \mu m$ and a conductor width of 20.25 μm.

TABLE II
Component Values from Synthesis

	APN1	APN2	APN3	APN4
Type	Type II	Type II	Type II	Type I
ϕ_{os}	$+90°$	$+45°$	$0°$	$-45°$
Q_{pole}	0.55	0.55	0.60	-
L_{a1} (pH)	614.58	437.88	282.84	245.14
M_1 (pH)	336.64	234.8	159.91	38.67
C_{a1} (fF)	55.58	40.61	24.5	41.29
C_{b1} (fF)	760.98	538.15	353.88	227.04
L_{a2} (pH)	276.18	253.51	301.59	163.71
L_{b2} (pH)	113.6	108.6	92.99	110.29
C_{a2} (fF)	90.88	86.88	74.39	88.23
C_{b2} (fF)	281.67	243.52	637.46	104.12

A. APNs

To design the four APNs with a $45°$ phase difference between them, the procedure from Section III was used. The choice for a 4th order network was done to achieve a $\pm 2°$ phase variation within the selected bandwidth of 20-45 GHz. The synthesized values were obtained using the following parameters: $n = 4, \tau = 1$ and $\delta = 0.01$ rad. The Q_{pole} factor was adjusted amongst different networks to achieve bandwidth alignment, as explained in Section III-C. After obtaining the prototype networks, they were scaled to a 50 Ω characteristic impedance and the common central frequency was scaled to 30 GHz. The resulting values for the four APNs are given on Table II.

The chosen network configuration is pictured in Fig. 10. Since the synthesis procedure generates complex poles instead of real poles, simpler networks without capacitor-T or inductor-T (such as T or pi) are not realizable. However, since the selected manufacturing process has high-Q MIM capacitors available, the capacitor-T network is used whenever possible to reduce the number of inductors, typically low-Q components in an integrated design process. However, when $Q_{pole} \leq 1$ for an APN section, capacitor-T implementations are also not allowed, as it would require a negative capacitor. The magnetic coupled inductor is then selected to implement a negative inductance value for the $Q_{pole} \leq 1$ sections given by the synthesis. Nonetheless, the proposed synthesis procedure allows only $Q_{pole} \leq 1$ sections, as Q_{pole} is a variable that we control. However, as we explained in the previous section, by increasing Q_{pole}, bandwidth is sacrificed, which justifies our choice of mutually coupled inductors.

Naturally, as perfect inductors and capacitors are not feasible, those synthesized values were a starting point for the physical design procedure. The ideal circuits offered a guideline on how to tune inductors and capacitors to achieve the expected behavior. The design procedure was initially performed separately by each 2^{nd} order section, with the mutual inductance APN section implementing a lower-ω_o pole

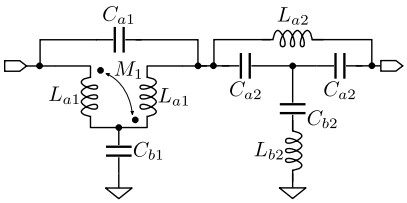


Fig. 10. Schematic of the APNs.

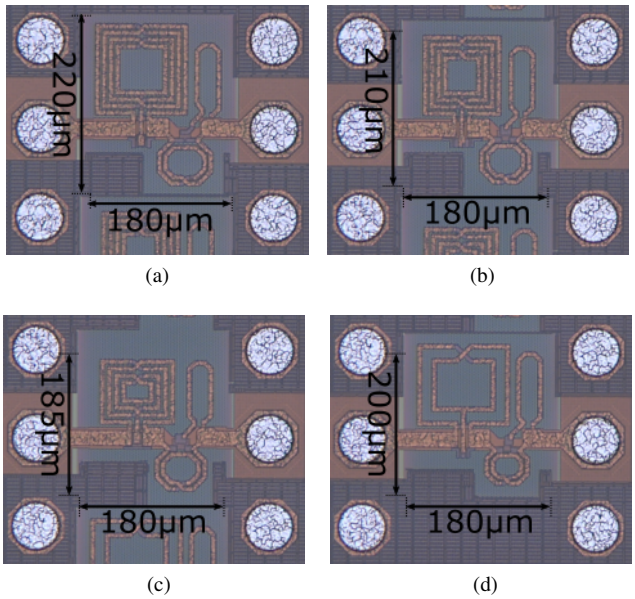


Fig. 11. On chip photographs of the four APNs, where (a) APN1, (b) APN2, (c) APN3 and (d) APN4.

and the capacitor-T APN section a higher-ω_o pole. Since the inductors of the higher-ω_o APN section are relatively small, their design is quite straightforward, consisting simply in designing the correct inductance values. EM simulations using Keysight's ADS Momentum [41] were performed to design the inductors.

For the lower-ω_o APN section, the design procedure required more iterations. First, the parameters of an inductor with center-tap, such as line spacing, number of windings, center tap length and area were tuned around the ω_o of the pole to achieve the inductance and coupling values specified by the synthesis procedure (shown in Table II). With the initial inductor design selected, we then obtain both intra-winding capacitance and capacitance to the substrate and absorb them into the parallel capacitor C_{a1}. After designing both APN sections individually, they were combined together with the microstrip line, with a new round of simulations and tuning to optimize performance. The inductors of both sections were packed tightly together to reduce overall area. The final APNs on-chip photographs are shown in Fig. 11. The APNs were placed as individual test structures on the chip to evaluate their performance separately from the switches. They all have a similar area, around $0.04\ mm^2$.

B. SP4T Switch

The design of the Single-Pole-4-Throw (SP4T) switch was largely inspired on the work from Cetinoneri [33]. The

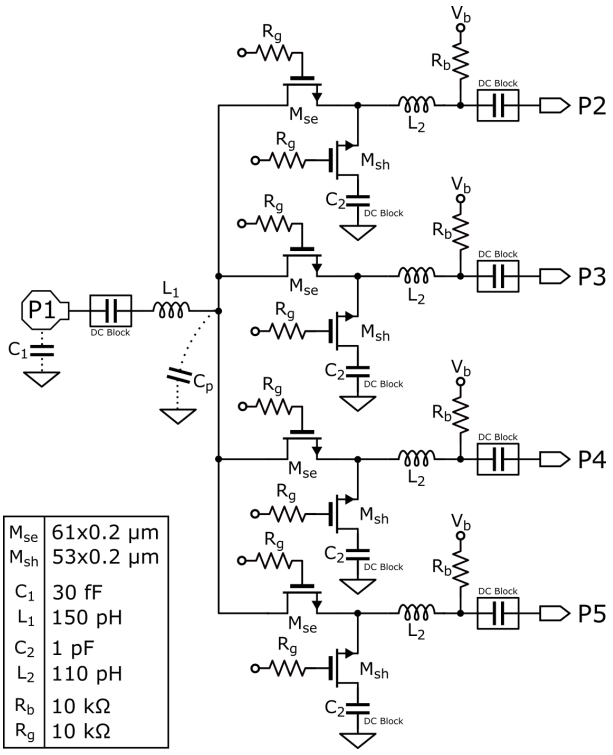


Fig. 12. Circuit schematic of the single-pole four-throw (SP4T) switch.

schematic of the switch is pictured in Fig. 12. In order to provide higher isolation between ports, a shunt-series configuration of MOS transistors were used, with channel length of $0.2\ \mu m$.

The channel width of the series transistor (M_{se}) is optimized to reduce overall insertion loss, while the channel width of the shunt transitor (M_{sh}) trades off isolation and input capacitance.

The output is matched to $50\ \Omega$ by means of L_2, which tunes the shunt capacitance to the substrate of the output node. The large parasitic input capacitance on the input node is matched through the Pi-network formed by $C_1 - L_1 - C_p$ [33].

Since double-well nMOS transistors were not available in the selected process, a special biasing was used. By biasing V_b with $2.5\ V$ and switching the gate from 0 to $5\ V$, the MOS transistor goes into a deep-off/deep-on state, having always $V_{gs} = \pm 2.5\ V$. The output node is biased with $2.5\ V$ through resistors $R_b = 10\ k\Omega$, to prevent signal leaking. Since there is always one path turned on, the input node is always at $2.5\ V$ as well. A DC block capacitor $C_2 = 1\ pF$ is placed to keep both sides of the shunt transistor M_{sh} at $2.5\ V$ when it is on, and to block a potential path from the biasing voltage to ground.

The input and output ports are DC-isolated via a DC-block capacitor $(10\ pF)$. In order to prevent signal leakage at the transistor's gate, a resistor $R_g = 10\ k\Omega$ was also placed.

The on-chip photograph of the SP4T is pictured in Fig. 13. A standalone test structure of the switch was placed at the chip, with ports P2 and P3 terminated with $50\ \Omega$ resistors. Since the capacitance C_1 had a similar value to the pad capacitance of the G-S-G to microstrip transition, we decided to use the pad as part of the matching network. However, when used in a

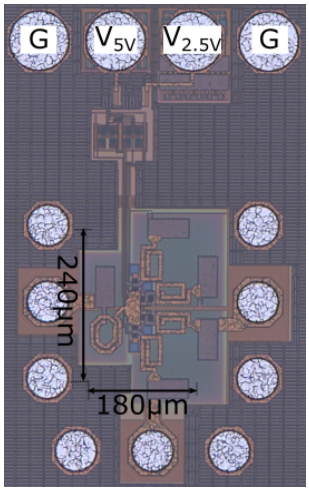


Fig. 13. On-chip photograph of the standalone single-pole four-throw (SP4T) switch. Output ports P2 and P3 were terminated with 50 Ω resistors to simplify characterization.

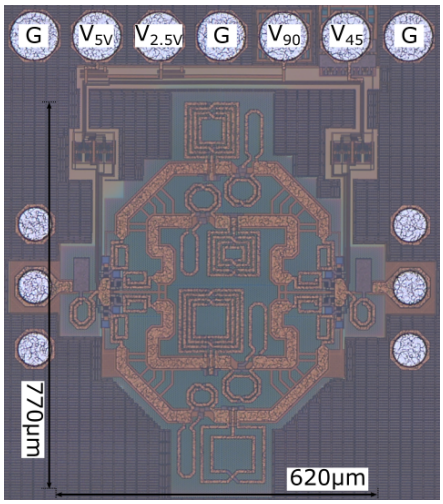


Fig. 14. On-chip photograph of the APN based STPS.

front-end, C_1 could be easily replaced by a MIM capacitor without increasing circuit area.

C. APN Based STPS

The APN based STPS was built using the building blocks presented. The on-chip photograph of the PS can be seen in Fig. 14. As the APNs are passive structures and work independently of bias, the DC-block capacitors on the SP4T outputs (P2-P5, see Fig. 12) were removed. The SP4T is connected to the APNs via microstrip lines as described before. In order to compensate the extra length needed to connect the edge networks, the transmission lines of the middle ones were bended. The resulting PS is bi-directional and consume zero static power. The total area without the pads is $0.62 \times 0.77\ mm^2$ ($\approx 0.48\ mm^2$) with an effective area occupied by the design of $0.35\ mm^2$. Although it seems a large area when compared to other solutions, the layout could be made more compact. The empty area around the design could fit the control logic for the switches.

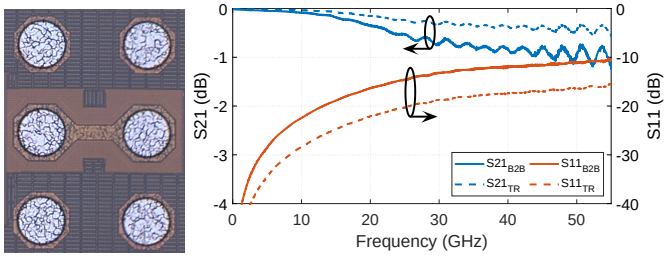


Fig. 15. (a) Back-to-back structure for de-embedding of G-S-G pads and (b) Measurement results of the G-S-G to microstrip line transition and back-to-back test structure.

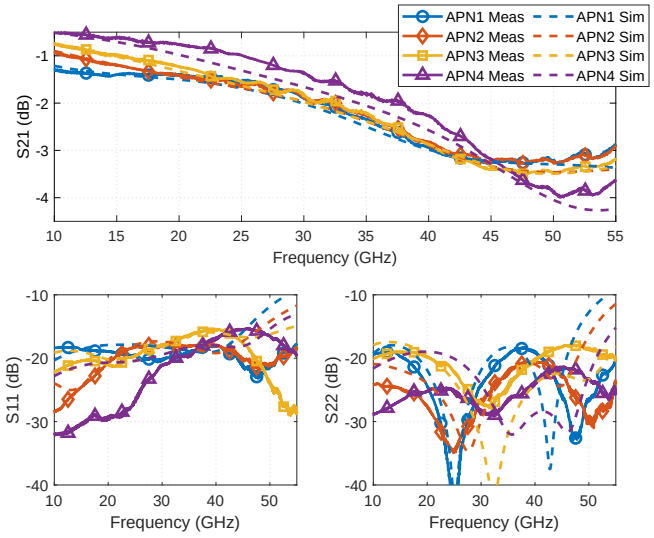


Fig. 16. Simulated and measured S-parameters of the four standalone APNs.

V. Measurement Results

The test structures pictured in the manuscript were measured using the network analyzer Agilent 67 GHz PNA E8361A with a Cascade Microtech Summit 12000B-S probe station. G-S-G probes with 125 μm pitch were used and were calibrated up to probe-tips using a SOTL approach. A dc probe-card was used when required. The measurements are compared with simulations performed in Spectre, where the EM partitions of the circuits were simulated in ADS Momentum and imported to Spectre.

A. APNs

Since the APNs were designed without the pads, a back-to-back structure was also placed to de-embed their effects from the APN measurements, pictured in Fig. 15(a). The performance of the transition was obtained through a symmetrical T-parameter matrix. The measurement results are pictured in Fig. 15(b), where the transition achieved a $S_{11} < -15$ dB up to 55 GHz.

The APNs were characterized using S-parameter measurements, pictured in Fig. 16. All measurement results for the APNs were de-embedded from the effects of the G-S-G to microstrip transition. The results follow the trend from

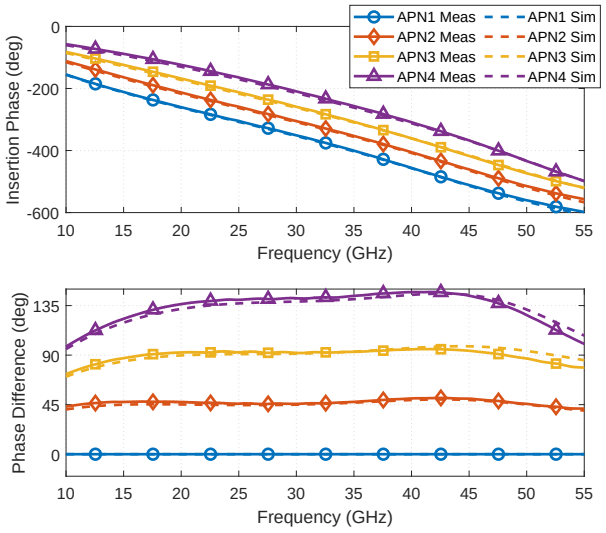


Fig. 17. Simulated and measured insertion phase of APNs and phase-difference between APNs and reference (APN1).

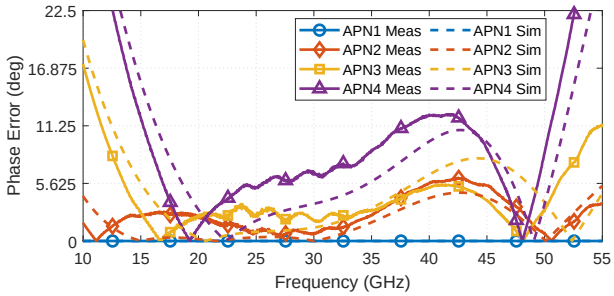


Fig. 18. Simulated and measured phase error of the standalone APNs.

simulations, with a IL of 1-4 dB observed within the 13-53 GHz frequency range. This is mainly due to IL from the inductors. For all APNs, the measured loss is 1.51 ± 0.26 dB at 28 GHz and 2.55 ± 0.32 dB at 39 GHz. The slight difference in loss observed in APN4 can be explain by the use of a two-turn inductor against four-turn inductors on the other three APNs. The return loss is kept under -15 dB across the bandwidth. This is the main characteristic of the APNs, also called constant resistance networks, which shows an overall 50 Ω profile of all APNs. Some disagreement between measurement and simulation can be explained by the simple de-embedding method used, which is more effective for IL.

The insertion phase of all four networks is presented in Fig. 17. Notice that their phase slope is equal with an offset observed between the settings, as expected from the synthesis theory, validating the proposed synthesis procedure. The measured insertion phase also follows the trend from simulations, which also validates the APN design procedure described in Section IV. To obtain the phase-difference $\Delta\phi$, we have taken the highest offset APN as a reference path (APN1), thus for the i'th APN $\Delta\phi_{\text{APNi}} = \angle S21_{\text{APNi}} - \angle S21_{\text{APN1}}$. Notice a clear swing around the ideal phase state values (45°, 90° and 135°).

To better grasp the phase performance of the APNs, the phase error ε of the i'th APN, defined by $\varepsilon_{\text{APNi}} = \Delta\phi_{\text{APNi}} - 45\times(i-1)$ is shown in Fig. 18. Notice that the maximum phase error is kept under 12° over a 15-50 GHz bandwidth, less than half of the LSB (22.5°). At 28 GHz, the maximum phase error is 5.8° and at 39 GHz, the error is kept under 11.8°. Considering the bandwidth defined by a phase error under 1/2 LSB, the APNs reach a 13-53 GHz band. The maximum difference between simulation and measurement inside the band of interest is kept under 3°, once again validating the design procedure.

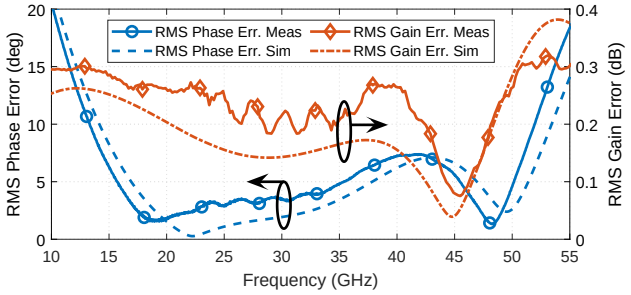


Fig. 19. Simulated and measured RMS gain and phase error between the four standalone APNs.

The RMS gain error between the networks, defined by $\Delta|S_{21}|_{\text{RMS}} = \sqrt{\left(\sum_{i=1}^{4}(|S_{21}|_{\text{APN}_i} - \overline{|S_{21}|_{\text{APN}}}\right)^2)/4}$, with $\overline{|S_{21}|_{\text{APN}}} = \sum_{i=1}^{4}|S_{21}|_{\text{APN}_i}/4$, is pictured in Fig. 19. The RMS gain error of the APNs is 0.22 at 28 GHz, 0.26 at 39 GHz and kept under 0.35 dB across the whole frequency range. The RMS phase error, defined by $\Delta\phi_{\text{RMS}} = \sqrt{(\sum_{i=1}^{4}\varepsilon_{\text{APN}_i})^2/4}$, is also pictured in Fig. 19. The maximum RMS phase error is kept under 7.5° from 14 to 50 GHz, with a maximum of 3° at 28 GHz and 6.9° at 39 GHz. Both RMS gain and phase error follow the simulations.

B. SP4T

As mentioned before, the SP4T switch was placed as a standalone device to be characterized as well. From Fig. 12, ports P2 and P3 were terminated with a 50Ω resistor, port P4 was kept on and port P5 was kept on isolation. The S-parameters were measured by placing three G-S-G probes and first using a termination at P5 to characterize the S-matrix between P1 and P4, and measured a second time terminating P4 and obtaining the transfer from P1 to P5. The S-parameters of the on-path (S_{41}, S_{11}, S_{44}) as well as the isolation are pictured in Fig. 20. The insertion loss varies from 2 to 5.5 dB over the 15-50 GHz band. S_{11} and S_{44} are kept under -10 dB up to 47 GHz, guaranteeing good matching with the APNs. The isolation between ports (S_{51}) is kept higher than 13 dB. A small ripple is observed here due to the fact that this port was placed on a 90° orientation, which required the rotation of the calibrated probe, causing small artifacts in the measurements. Furthermore, measurements follow simulation trends.

C. APN-based STPS

To characterize the APN-based STPS, a dc probe card was used together with the G-S-G probe to proper bias and control

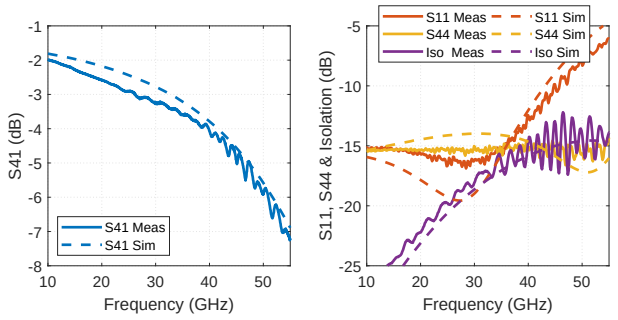
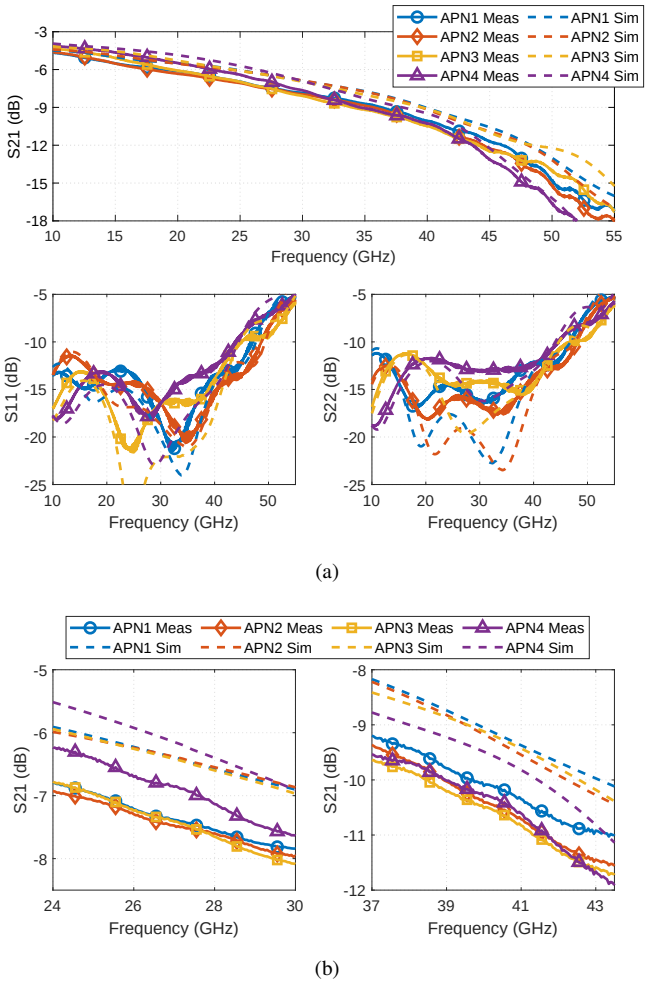


Fig. 20. S-parameters of the on-path and isolation between ports of standalone SP4T.



(a)

(b)

Fig. 21. Simulated and measured (a) S-parameters of all setting of the PS and (b) S_{21} zoom in the 5G bands.

the device. To simplify characterization, the input pad capacitance was part of the matching network, thus de-embedding was not necessary here. The measured S-parameters of the PS for all settings are pictured in Fig. 21(a). S_{21} has a large variation across the band, from -5 dB up to -16 dB. However, when zoomed in the 5G bands, as pictured in Fig. 21(b), the variation is much smaller, around 2 dB from 24-30 GHz and 2.7 dB from 37-43 GHz. At 28 GHz a loss of 7.4 ± 0.26 dB is observed for all settings, while at 39 GHz the losses are 10 ± 0.22 dB. Both S_{11} and S_{22} are kept < -10 dB up to

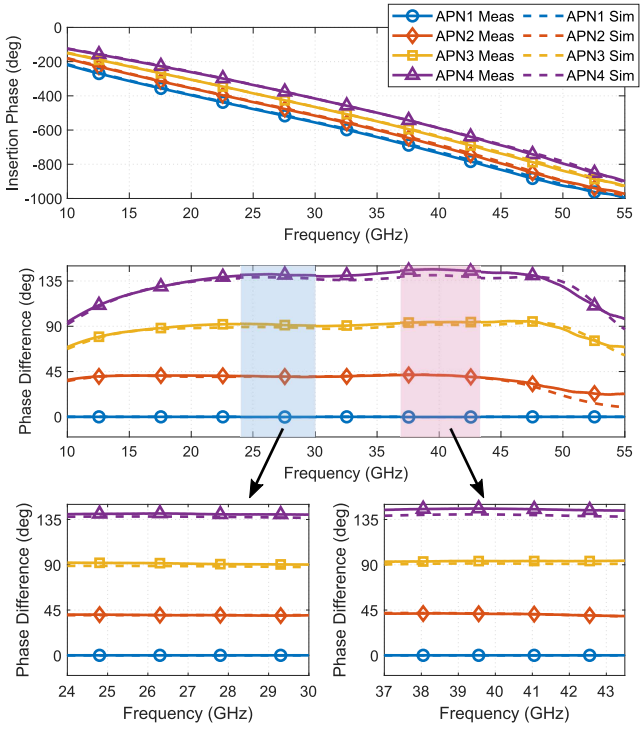


Fig. 22. Simulated and measured insertion phase and phase-difference of all setting of the PS, with a phase-difference zoom in the 5G bands.

44 GHz, and < -7 dB up to 50 GHz for all settings. The return losses are limited by the SP4T switch performance. When compared to simulation, S_{21}, S_{11} and S_{22} all follow the trend from simulations, with S_{21} showing an absolute IL difference of ≈ 1 dB, likely due to simplifications in the EM model.

The insertion phase and phase difference ($\Delta\phi$) for all settings is presented in Fig. 22. As expected, both curves have a similar behavior as the APN curves. Once again, a clear swing around the ideal phase state values (45°, 90° and 135°) is observed. A zoom in the 5G bands is also pictured in Fig. 22, which shows a nearly constant phase-difference. Although the average $\Delta\phi$ does not match perfectly the ideal phase state values (from 24-30 GHz, 0° 40°, 91° and 140°; from 37-43.5 GHz, 0° 42°, 93.5° and 144.8°) the phase variation around the average is kept $< \pm 1°$ from 24-30 GHz and $< \pm 0.9°$ from 37-43 GHz. The phase error between ideal and obtained phase-states is pictured in Fig. 23, which is kept under 11.25° from 15-47 GHz. The bandwidth where the phase error is $< 1/2$ LSB (22.5°) is from 14-50 GHz. The phase error at 28 GHz is $< 5.2°$ and $< 10.7°$ at 39 GHz. Measurements follow closely the simulations for the phase-curves, with the maximum difference below 6°.

The RMS gain and phase error, defined previously, are pictured in Fig. 24. The RMS gain error of the proposed PS is < 0.5 dB up to 45 GHz and < 1 dB up to 51 GHz, with an RMS gain error of 0.21 dB @ 28 GHz and 0.15 dB @ 39 GHz. The RMS phase error is kept under 10° from 14-50 GHz, with a RMS phase error of 3.6° at 28 GHz and 5.9° at 39 GHz. Measurements also follow simulations for the RMS errors.

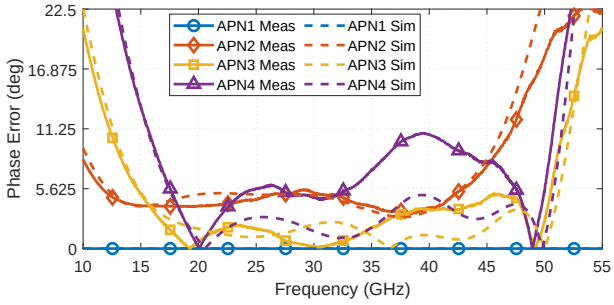


Fig. 23. Simulated and measured phase error for all setting of the PS.

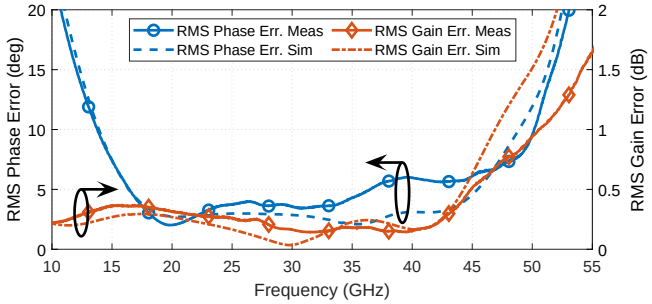


Fig. 24. Simulated and measured RMS gain and phase error of the PS.

As the broadband capabilities of the proposed PS are directed towards covering a broad range of possible 5G frequency channels rather than being used for a single broadband signal, an important assessment is to observe the behavior of the proposed design w.r.t. various channel bands. To evaluate the behavior within individual channels, we have divided the 14-50 GHz frequency range into 800 MHz slots, from 14 to 50 GHz, and observed both IL and phase error behavior for all PS settings within these slots by splitting both quantities into a mean error over the channel ($\overline{IL}$ and $\bar{\varepsilon}$, respectively) and a variation over that mean (Δ_{IL} and $\Delta\varepsilon$, respectively). Therefore, for the k'th channel, we can describe IL by $IL[k] = \overline{IL}[k] \pm \Delta_{IL}[k]$ and phase error by $\varepsilon[k] = \bar{\varepsilon}[k] \pm \Delta\varepsilon[k]$. Ideally, the IL and phase difference within a slot should remain constant to guarantee a uniform beamforming and low distortion effects, thus $\Delta\varepsilon$ and Δ_{IL} should be as small as possible.

Both $\overline{IL}[k]$ and $\bar{\varepsilon}[k]$ can be easily evaluated through Fig. 21 and 23. For $\Delta_{IL}[k]$ and $\Delta\varepsilon[k]$, the maximum between all settings is plotted per channel in Fig. 25. The proposed PS achieved a Δ_{IL} of < 0.25 dB from 14 up to 43 GHz, and a $\Delta\varepsilon$ of $< 1°$ from 17 up to 47 GHz. For every 800 MHz channel across the whole 14 to 50 GHz frequency range, the $\Delta\varepsilon$ was kept under $< 2°$ and Δ_{IL} was kept under 0.5 dB. When the 5G main bands are considered, $\Delta\varepsilon < 0.26°$ and $\Delta_{IL} < 0.16$ dB from 24-30 GHz and $\Delta\varepsilon < 0.39°$ and $\Delta_{IL} < 0.23$ dB from 37-43.5 GHz.

The performance of the APN-based STPS is compared with SOTA mm-wave phase shifters in Table III. We present our bandwidth based on having the maximum phase error under $1/2$ LSB, which means the phase-states are still distinguishable from each other. The proposed PS achieved the highest bandwidth, in percentage, reported for mm-wave 5G applications in the literature, to the best of our knowledge. We have also highlighted the performance within the 5G bands (24-30 GHz and 37-43 GHz). Notice a very competitive performance within those bands even when compared with smaller technology nodes. The main drawback of the APN based approach is the area, which is a point of improvement for future designs.

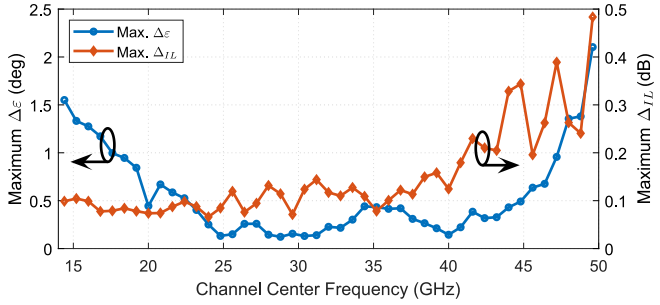


Fig. 25. Maximum measured IL and phase error variation over mean (Δ_{IL} and $\Delta\varepsilon$) values for every 800 MHz frequency slot across the PS frequency operation range. Values are plotted w.r.t. the center frequency of the 800 MHz frequency slot.

VI. Conclusion

This paper presented an ultra broad-band APN based STPS for 5G mobile applications. The requirements from the application were discussed to justify the proposed topology, a 2-bit, $45°$ resolution PS with four APNs in parallel. To allow parallelization of APNs, the linear-phase APNs synthesis was revisited and placed in an up to date context, and a bandwidth alignment procedure was proposed. Using the procedure, the APN based STPS was presented, which achieved a bandwidth from 14 to 50 GHz, the highest bandwidth reported in literature for mm-wave PSs, to the best knowledge of the authors. The proposed solution also achieved a competitive insertion loss when compared band-to-band with literature, while consuming zero static power.

Acknowledgment

The authors would like to acknowledge the support from L. Praamsma during design and M. Webers during measurements. We would also like to thank Dr. S. Bhaumik and Dr. J. Qureshi for fruitful discussions.

References

[1] M. Agiwal, A. Roy, and N. Saxena, "Next generation 5G wireless networks: A comprehensive survey," *IEEE Commun. Surveys Tuts.*, vol. 18, no. 3, pp. 1617–1655, 2016.
[2] A. Puglielli *et al.*, "Design of energy- and cost-efficient massive MIMO arrays," *Proc. IEEE*, vol. 104, no. 3, pp. 586–606, Mar. 2016.
[3] "National 5g spectrum assignment – 5g Observatory." [Online]. Available: http://5gobservatory.eu/5g-spectrum/national-5g-spectrum-assignment/
[4] "The FCC's 5g FAST Plan | Federal Communications Commission." [Online]. Available: https://www.fcc.gov/5G
[5] "Ericsson microwave outlook," Ericsson AB, Dec. 2018, White Paper. [Online]. Available: https://www.ericsson.com/assets/local/microwave-outlook/documents/ericsson-microwave-outlook-report-2018.pdf

TABLE III
STATE-OF-THE-ART MM-WAVE PHASE SHIFTERS

Approach [Ref.]	RTPS [13]	STPS [11]	Tun. TL [12]	STPS [32]	STPS [31]	STPS [30]	VM [21]	This work		
Process	$65\ nm$ CMOS	$0.12\ \mu m$ BiCMOS	$0.13\ \mu m$ BiCMOS	$40\ nm$ CMOS	$45\ nm$ CMOS SOI	$65\ nm$ CMOS	$0.18\ \mu m$ BiCMOS	$0.25\ \mu m$ BiCMOS		
								1/2 LSB	**5G BW1**	**5G BW2**
Bandwidth (GHz)	$26-30$	$30-40$	$26-30$	$22-36$	$25-33$	$27.5-28.4$	$15-35$	$14-50$	$24-30$	$37-43.5$
Rel. Bandwidth (%)	14.3%	28.9%	14.3%	49.7%	27.9%	3%	87%	136%	22.3%	16.2%
Resolution (°)	11.25°	22.5°	5°	45°	11.25°	22.5°	22.5°	45°	45°	45°
No. of bits	5	4	5	3	5	4	4	2	2	2
RMS Phase Err. (°)	$< 0.3°$	$< 11.25°$	$< 0.6°$	$< 12.8°$	$< 5°$	$< 8.98°$	$< 13°$	$< 9.7°$	$< 4°$	$< 6°$
RMS Gain Err. (dB)	< 0.3	< 1.1	< 0.2	< 0.6	< 0.8	N/A	< 2.2	< 0.94	< 0.27	< 0.33
IL (dB)	6.7 to 9.3	10 to 18	9.05 to 9.55	5 to 8	6 to 13	5.4 to 7.7	-5 to 13.5	5 to 16	6.2 to 8.1	9.2 to 11.9
Loss mid. band (dB)	7.75 ± 0.3	12.6 ± 1.1	9.3 ± 0.25	5.6 ± 0.5	7 ± 1	6.6 ± 1	4 ± 2	7.2 ± 0.3	7.2 ± 0.3	10.3 ± 0.2
Return Loss (dB)	< -6.7	< -10	N/A	< -7	< -8	< -12	N/A	< -7	< -12	< -12
Power (mW)	0	0	0	0	0	0	25.2	0	0	0
Area (mm^2)	0.16	0.1144	0.18	0.132	N/A	0.23	0.19	0.48	0.48	0.48

[6] W. Roh *et al.*, "Millimeter-wave beamforming as an enabling technology for 5G cellular communications: theoretical feasibility and prototype results," *IEEE Commun. Mag.*, vol. 52, no. 2, pp. 106–113, Feb. 2014.

[7] S. Han, C.-l. I, Z. Xu, and C. Rowell, "Large-scale antenna systems with hybrid analog and digital beamforming for millimeter wave 5G," *IEEE Commun. Mag.*, vol. 53, no. 1, pp. 186–194, Jan. 2015.

[8] X. Guan, H. Hashemi, and A. Hajimiri, "A fully integrated 24-GHz eight-element phased-array receiver in silicon," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2311–2320, Dec. 2004.

[9] K.-J. Koh and G. M. Rebeiz, "0.13-μm CMOS phase shifters for X-, Ku-, and K-band phased arrays," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2535–2546, Nov. 2007.

[10] B. Sadhu *et al.*, "A 28-GHz 32-element TRX phased-array IC with concurrent dual-polarized operation and orthogonal phase and gain control for 5G communications," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3373–3391, Dec. 2017.

[11] B.-W. Min and G. M. Rebeiz, "Single-ended and differential Ka-band BiCMOS phased array front-ends," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2239–2250, Oct. 2008.

[12] Y. Tousi and A. Valdes-Garcia, "A Ka-band digitally-controlled phase shifter with sub-degree phase precision," in *2016 IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, San Francisco, CA, USA, May 2016, pp. 356–359.

[13] R. Garg and A. S. Natarajan, "A 28-GHz low-power phased-array receiver front-end with 360° RTPS phase shift range," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 11, pp. 4703–4714, Nov. 2017.

[14] D. Adler and R. Popovich, "Broadband switched-bit phase shifter using all-pass networks," in *1991 IEEE MTT-S Int. Microw. Symp. Dig.*, Boston, MA, USA, July 1991, pp. 265–268 vol.1.

[15] X. Tang and K. Mouthaan, "Design considerations for octave-band phase shifters using discrete components," *IEEE Trans. Microw. Theory Techn.*, Dec. 2010.

[16] ——, "Design of large bandwidth phase shifters using common mode all-pass networks," *IEEE Microw. Wireless Compon. Lett.*, vol. 22, no. 2, pp. 55–57, Feb. 2012.

[17] ——, "Large bandwidth digital phase shifters with all-pass, high-pass, and low-pass networks," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 6, pp. 2325–2331, Jun. 2013.

[18] H.-Y. Li and J.-S. Fu, "Analysis of magnetically coupled all-pass network for phase-shifter design," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 9, pp. 2025–2037, Sep. 2014.

[19] ——, "Broadband complementary metal-oxide semiconductor phase shifter with 6-bit resolution based on all-pass networks," *IET Microw., Antennas and Propag.*, vol. 9, no. 11, pp. 1144–1151, Aug. 2015.

[20] S. Y. Kim, D.-W. Kang, K.-J. Koh, and G. M. Rebeiz, "An improved wideband all-pass I/Q network for millimeter-wave phase shifters," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 11, pp. 3431–3439, Nov. 2012.

[21] S. P. Sah, X. Yu, and D. Heo, "Design and analysis of a wideband 15–35-GHz quadrature phase shifter with inductive loading," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 8, pp. 3024–3033, Aug. 2013.

[22] M. Hangai, M. Hieda, N. Yunoue, Y. Sasaki, and M. Miyazaki, "S- and C-band ultra-compact phase shifters based on all-pass networks," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 1, pp. 41–47, Jan 2010.

[23] O. Herrmann, "Quadraturfilter mit rationalem ubertragungsfaktor," *Arch. Elektron. & Ubertragungstech.*, vol. 23, no. 2, pp. 77–84, 1969.

[24] P. Challener, "Design and realisation of practical wideband quadrature networks with linear phase-shift characteristics," *IEE J. on Electron. Circuits and Syst.*, vol. 2, no. 3, p. 65, 1978.

[25] J. D. Dunworth *et al.*, "A 28 GHz Bulk-CMOS dual-polarization phased-array transceiver with 24 channels for 5G user and basestation equipment," in *2018 IEEE Int. Solid-State Circuits Conf. - (ISSCC)*, San Francisco, CA, Feb. 2018, pp. 70–72.

[26] Y. Hsu, T. Huang, H. Lin, and Y. Lin, "Dual-polarized quasi yagi–uda antennas with endfire radiation for millimeter-wave MIMO terminals," *IEEE Trans. Antennas Propag.*, vol. 65, no. 12, pp. 6282–6289, Dec 2017.

[27] M. Salarrahimi *et al.*, "A low-cost analog beamforming antenna for 5G mm-wave handset applications," in *2019 Eur. Conf. on Antennas Propag. (EUCAP)*, Krakow, Poland, Apr. 2019.

[28] A. S. Y. Poon and M. Taghivand, "Supporting and enabling circuits for antenna arrays in wireless communications," *Proc. IEEE*, vol. 100, no. 7, pp. 2207–2218, July 2012.

[29] D. Kang, J. Kim, B. Min, and G. M. Rebeiz, "Single and four-element Ka-band transmit/receive phased-array silicon RFICs with 5-bit amplitude and phase control," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 12, pp. 3534–3543, Dec 2009.

[30] G. Shin *et al.*, "Low insertion loss, compact 4-bit phase shifter in 65 nm CMOS for 5G applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 1, pp. 37–39, Jan 2016.

[31] U. Kodak and G. M. Rebeiz, "Bi-directional flip-chip 28 GHz phased-array core-chip in 45nm CMOS SOI for high-efficiency high-linearity 5G systems," in *2017 IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, June 2017, pp. 61–64.

[32] M. Elkholy, S. Shakib, J. Dunworth, V. Aparin, and K. Entesari, "Low-loss highly linear integrated passive phase shifters for 5G front ends on bulk CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 10, pp. 4563–4575, Oct 2018.

[33] B. Cetinoneri, Y. A. Atesal, and G. M. Rebeiz, "A miniature DC-70 GHz SP4T switch in 0.13-μm CMOS," in *2009 IEEE MTT-S Int. Microwave Symp. Dig.*, Boston, MA, USA, Jun. 2009, pp. 1093–1096.

[34] M. Parlak and J. F. Buckwalter, "A 2.5-dB insertion loss, DC-60 GHz CMOS SPDT switch in 45-nm SOI," in *2011 IEEE Compound Semicond. Integr. Circuit Symp. (CSICS)*, Oct 2011, pp. 1–4.

[35] K. G. Hodgson, "Electrical circuit arrangement for obtaining substantially constan relative phase shifts over a range of frequencies," Britain Patent 547,601, 1941.

[36] W. Saraga, "The design of wide-band phase splitting networks," *Proc. of the IRE*, vol. 38, no. 7, pp. 754–770, Jul. 1950.

[37] S. Darlington, "Realization of a constant phase difference," *Bell Syst. Tech. J.*, vol. 29, no. 1, pp. 94–104, Jan. 1950.

[38] H. J. Orchard, "Synthesis of wideband two-phase networks," *Wireless Engineer*, vol. 27, pp. 72–81, 1950.

[39] A. Hausner and C. M. Furlani, "Chebyshev all-pass approximants for time-delay simulation," *IEEE Trans. on Electron. Comput.*, vol. EC-15, no. 3, pp. 314–321, Jun. 1966.

[40] W. D. van Noort *et al.*, "BiCMOS technology improvements for microwave application," in *2008 IEEE Bipolar/BiCMOS Circ. and Tech. Meeting*, Monterey, CA, Oct. 2008, pp. 93–96.

[41] "Advanced Design System (ADS) | Keysight (formerly Agilent's Electronic Measurement)." [Online]. Available: https://www.keysight.com/en/pc-1297113/advanced-design-system-ads

Eduardo V. P. Anjos (S'15) received the B.Sc. in Electronics and Computer Engineering and M.Sc. in Electrical Engineering from the Federal University of Rio de Janeiro, Brazil, in 2014 and 2016, respectively. He is currently pursuing the Ph.D. degree in Electrical Engineering at ESAT, KU Leuven, Leuven, Belgium.

Since 2017, he holds an Intern position at NXP Semiconductors, Nijmegen, The Netherlands, where he is involved in millimeter-wave circuit design. His research interests include all-pass networks, integrated phased array transceivers, phased array systems and over-the-air measurements.

Dominique Schreurs (S'90–M'97–SM'02–F'12) received the M.Sc. degree in electronic engineering and the Ph.D. degree from the University of Leuven (KU Leuven), Leuven, Belgium.

She has been a Visiting Scientist with Agilent Technologies, Santa Rosa, CA, USA, ETH Zurich, Zürich, Switzerland, and the National Institute of Standards and Technology, Boulder, CO, USA. She is currently a Full Professor with KU Leuven, where she is also the Chair of the Leuven LICT. Her current research interests include the microwave and millimeter-wave characterization and modeling of transistors, nonlinear circuits, and bioliquids, and system design for wireless communications and biomedical applications.

Dr. Schreurs was an IEEE MTT-S Distinguished Microwave Lecturer. She is also the President of the IEEE Microwave Theory and Techniques Society. She was the General Chair of the 2007, 2012, and 2018 Spring ARFTG Conferences. She is currently the President of the ARFTG Organization. She was the Editor-in-Chief of the IEEE Transactions on Microwave Theory and Techniques.

Guy A. E. Vandenbosch received the M.S. and Ph.D. degrees in Electrical Engineering from the KU Leuven, Leuven, Belgium, in 1985 and 1991, respectively. Since 1993, he has been a Lecturer, and since 2005, a Full Professor at the same university.

His research interests are in the area of electromagnetic theory, computational electromagnetics, planar antennas and circuits, nano-electromagnetics, EM radiation, EMC, and bio-electromagnetics. His work has been published in ca. 330 papers in international journals and has led to ca. 385 papers at international conferences.

Guy Vandenbosch has been a member of the "Management Committees" of the consecutive European COST actions on antennas since 1993. Within the ACE Network of Excellence of the EU (2004-2007), he was a member of the Executive Board and coordinated the activity on the creation of a European antenna software platform. After ACE, from 2007 – 2018, he chaired the EuRAAP Working Group on Software. In the period 1999-2004, he was vice-chairman, in the period 2005-2009 secretary, and in the period 2010-2017 chairman of the IEEE Benelux Chapter on Antennas en Propagation. In the period 2002-2004 he was secretary of the IEEE Benelux Chapter on EMC. In the period 2012-2014, he was secretary of the Belgian National Committee for Radio-electricity (URSI), where he is also in charge of commission E. Guy Vandenbosch is a fellow of the IEEE. From September to December 2014, he was a visiting professor at Tsinghua University, Beijing, China. Since 2017 he is a member of the IEEE Electromagnetics Award Committee.

Marcel Geurts was born in Texel, the Netherlands, in 1966. He received his MSc in Electronic Engineering from the Technical university Delft in 1993 on allpass phase shifter for X-band. After his graduation he joined TNO. In 1995 he joined Philips (now NXP) semiconductors, for design-in of fiber optic interface ICs. In 2004 he became system architect for Ku band downconverter, expanding to smart phone LNA's and mmwave components. His current focus is new business. He initiated international cooperation programs and is part of the management of these programs.