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Intra-Grain and Oligo-Grain Top-Contact Organic Thin film Transistors

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ABSTRACT

We describe and demonstrate a micromachined shadowmask that allows the realization of intra-grain and oligo-grain top-contact organic thin film transistors (OTFTs). First experimental results of OTFT's show that for small channel lengths, grain boundary barriers indeed appear to dominate the output characteristics of OTFTs.

INTRODUCTION

Organic thin film transistors (OTFTs) offer a potentially low-cost, large-area technology for low-end applications. Sublimed organic small-molecule thin films offer advantages as active layer in OTFTs compared to solution-processed films. Small-molecule thin films can have higher charge-carrier mobilities due to their crystalline nature and often are of higher purity. However, polycrystalline films have traps at grain boundaries and at the interface with the gate dielectric. Both trap distributions can be expected to depend on growth conditions, providing for a complex relation between morphology and OTFT properties like mobility, threshold voltage, onset voltage and subthreshold slope. Intragrain transistors and transistors having only a limited number of grain boundaries in their channel are a useful tool to study this relation. While photolithographically defined bottom-contacts can easily reach channel lengths comparable to or smaller than the grain size of typical organic thin films, the growth of the organic thin film on top of those contacts is often disturbed by the presence of the contacts. Moreover, contact effects are usually more pronounced than for contacts grown on top of the organic thin films due to the smaller effective contact area of the bottom-contacts [1]. We evaporated metal contacts on top of organic thin films through a micromachined shadowmask to make transistors having channel lengths down to 400nm. This top-contact approach allows to study the properties of intragrain and oligograin transistors without influencing film growth and with little contact effects. The technology to make those micromachined shadowmask will be presented here, together with the first results on organic thin films.

EXPERIMENT

The fabrication of the shadowmask using standard micromachining techniques is explained in figure 1. 500nm SiO_2 is grown on a silicon wafer with (100) surface. Next, 150 nm LPCVD Si_3N_4 is deposited on both sides of the wafer. This nitride will grow almost free of stress on the oxide, apart from some residual tensile stress. On the backside of the wafer large rectangular areas, having a width approximately twice the wafer thickness, are defined approximately parallel to the main crystal axes using photolithography. In those areas, the nitride is removed by CF_4 plasma. In a KOH-solution, a trench is etched fully through the silicon wafer selectively along the (111) surfaces, using the nitride on the backside as an etch mask, and the nitride on the frontside as etch stop layer. Finally, the frontside nitride forms a membrane stretched over the

trench. This membrane can be patterned by various techniques. The easiest way is to protect bridges of nitride stretching over the trench by photolithographically defined patterns of resist and to etch the remaining nitride away in CF_4-plasma. The frontside of this mask can be put on an organic film, and metal can be evaporated through the trenches and the holes in the nitride membrane. The nitride bridges will protect the transistor channels. Channel lengths down to 2 μm can be obtained this way. Alternatively, the frontside nitride membrane can be patterned using direct write Focussed Ion Beam (FIB) to locally sputter the nitride away. This technique allows much finer dimensions and more complicated patterns. However, not all patterns are mechanically stable against the intrinsic tensile stress in the nitride. Corners in the pattern need to be rounded off and should not be too close to each other, limiting the minimum width of the transistor channels. We have simulated stress distributions using the finite element method, and designed and implemented stress relief structures in the nitride to guide the stress away from critical dimensions. Channel lengths down to 400nm with widths of 10μm were succesfully demonstrated, as well as channel widths of 2μm with channel lengths of 2 μm. A third alternative, patterning the frontside nitride by e-beam, is under development.

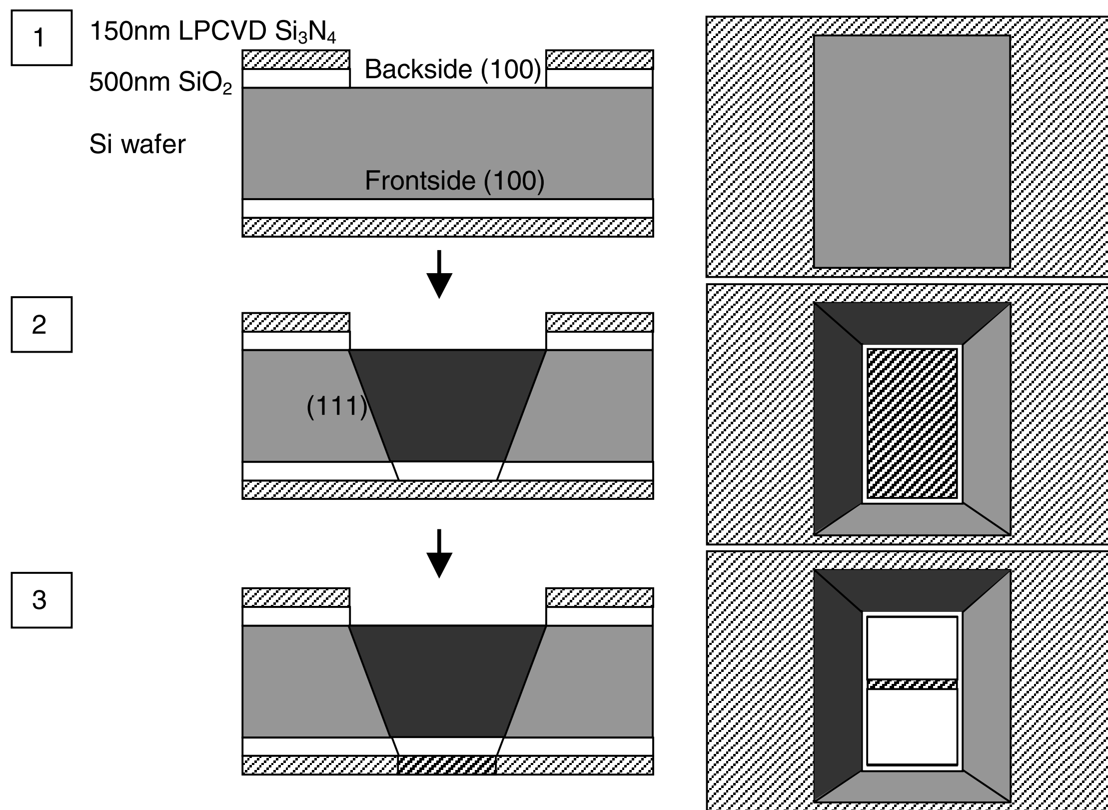

Figure 1. Fabrication of micromachined shadowmask. A (100) silicon wafer is oxidized on both sides, followed by nitride deposition. 1) On the backside of the wafer, the nitride is patterned using photolithography and subsequently etched away in CF_4 plasma. 2) Si is etched away selectively along the (111) planes in a KOH solution, using the nitride as an etch mask. The KOH etch stops at the nitride membrane on the front side of the wafer. 3) The nitride membrane can be patterned using Focussed Ion Beam to sputter the nitride away at the desired places, or using lithography followed by another CF_4 plasma etch.

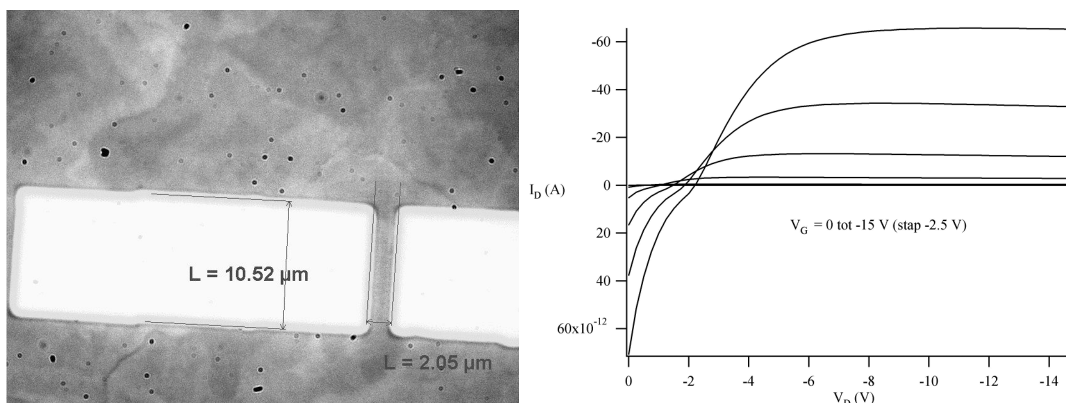

Figure 2. The left figure shows a photograph of a terrylene transistor with a channel length of 2 µm. The right figure is the drain current I_D versus drain voltage V_D characteristics for various gate voltages V_G for the device in the left picture.

Intra-grain transistors

To demonstrate this shadowmask technology, intra-grain OTFTs were successfully prepared. Shadowmasks were patterned using FIB, producing W/L's of 2/2µm and 10/0.5µm. Organic thin films of terrylene were fabricated on top of 20nm thermally grown $Si0_2$ on Si. The substrate functions as gate and gate-dielectric. Terrylene has a relatively high vapor pressure, and therefore more easily allows the growth of thin films with larger grains [2]. Compact grains with diameters of 10µm could be grown. Figure 2 shows an optical picture and the electrical characteristics of one terrylene transistor with shadowmask evaporated gold contacts. The terrylene transistor had W/L=10µm/2µm, and the extracted mobility is ~10^{-5} cm^2/Vs. This low mobility is attributed to the large amount of impurities as indicated by TOFSIMS analysis of the thin film. No clear transistor behaviour could be distinguished in devices with three or more grain boundaries, even with larger W/L. Although the FIB does not allow to easily make many devices nor many shadowmasks, and the terrylene material lacks electronic grade purity, those devices clearly demonstrate that this shadowmask technology is functional. No shorts were detected between source and drain for channel lengths down to 0,5µm.

Oligo-grain transistors

Using photolithographically patterned shadowmasks, transistors could be made with channel lengths L varying between 2 and 50µm, while the channel width is determined by the width of trench etched in the silicon wafer, typically varying between 30 and 150µm. Pentacene thin films were grown on octadecyltrichlorosilane (OTS) treated surfaces of 100nm thermally oxidized highly doped silicon wafers. The oxidized wafers again function as gate and gate-dielectric. On top of the pentacene film, source and drain contacts with varying channel lengths were deposited. Figure 3 shows an AFM picture of the pentacene film, together with the I_D-V_D characteristics of transistors with various channel lengths. It can clearly be seen that the drain current does not saturate for the smallest channel, while the saturation improves for increasing channel lengths. For the given channel lengths and oxide thickness, the lack of saturation cannot be explained by a deviation from the gradual channel approximation. We tentatively attribute this to drain induced grain boundary barrier effects, which show similar characteristics [3].

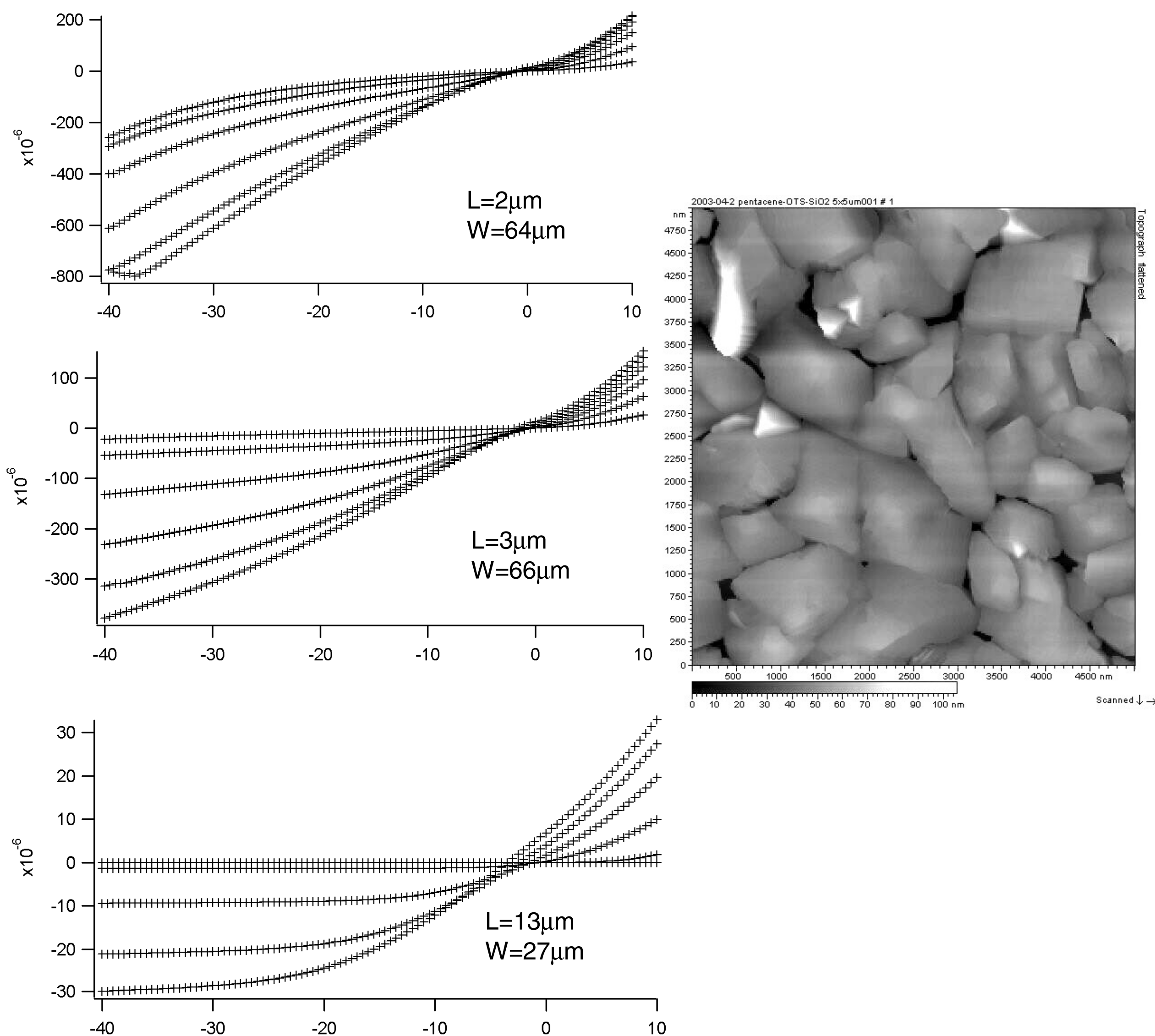

Figure 3. Pentacene transistors with channel lengths of 2, 3 and 13 μm. The gate voltage varies between +10V to –40V in steps of 10V. The saturation regime improves noticeably with increasing channel length. The electrical characteristics are dominated by grain boundary barriers for the smallest channel lengths. On the right is a 5x5μm AFM scan of the pentacene film.

CONCLUSIONS

We have developed and demonstrated a micromachined shadowmask that is used to fabricate short-channel OTFTs, which allow for probing intra-grain and grain boundary effects. Intra-grain devices offer the opportunity to extract the intrinsic charge-carrier mobility, yet also magnify various device-related issues. Oligo-grain devices appear to be dominated by grain boundary barrier effects.

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