On the apparent non-Arrhenius temperature dependence of charge-trapping in IIIV/high-k MOS stack

Vamsi Putcha^{1,2,#}, Jacopo Franco², Abhithosh Vais², Sonja Sioncke², Ben Kaczer², Dimitri Linten² and Guido Groeseneken^{1,2}

¹ESAT, KU Leuven, Belgium, ²IMEC, Kapeldreef 75, Leuven, Belgium, [#]vamsi.putcha@imec.be

Abstract— Operating temperature has a significant impact on the reliability of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). In Si-channel MOSFETs, the effective density of charged oxide defects (ΔN_{eff}) at operating condition typically shows an Arrhenius temperature dependence with $E_A \sim 0.1$ eV. In contrast, apparent non-Arrhenius temperature dependence is reported here for InGaAs devices subjected to BTI stress in a wide range of temperature (77 K to 373 K). This apparent non-Arrhenius temperature dependence is explained here by the presence of *three* distinct populations of electron traps. Capture-Emission-Time (CET) maps are derived from the experimental data, and are modeled by three bivariate distributions of energy barriers for the capture and emission processes. The total ΔV_{th} measured in BTI experiments reflects different contributions from the three defect populations, depending on the chosen temperature range, and on the measurement timing. We show that a correct description of the three defect distributions is crucial to properly assess their impact on the device performance.

Index Terms—BTI, reliability, InGaAs, non-Arrhenius, Capture-Emission-Time map (CET), bivariate defect distributions

I. INTRODUCTION

THE major hurdles arising from unabated downscaling of Metal Oxide Semiconductor Field Effect Transistors' (MOSFETs) dimensions to boost device performance could be alleviated by replacing the traditional Si channel with a suitable high-mobility material like InGaAs [1-4]. For this radical change to happen, it is also necessary to demonstrate sufficient reliability of the InGaAs channel MOSFETs [5-6]. It is well-known that defects in the gate-stack significantly affect device parameters such as mobility, capacitance, and transconductance, in addition to Bias-Temperature-Instability (BTI) [7-9]. In particular, BTI induces a shift in the threshold voltage (V_{th}) as a result of charging of the oxide defects. The nominal target for a 10 year operating lifetime is a maximum V_{th} shift of 30mV at the operating voltage (V_{DD}).

The temperature dependence of the charge-trapping kinetics of defects in the gate-stack – responsible for the instability of the device V_{th} – has been discussed in [10-11]. It was shown that charge trapping into defects in the gate-stack cannot be explained by a direct tunneling process, but can be described by

the Non-radiative Multi-Phonon (NMP) model. According to the NMP model, capture and emission of charge carriers is assisted by absorption/release of phonons [12,13]. The energy contribution from the phonons and the capture cross-section of the defect are dependent on temperature [10] and hence, the amount of charge trapped in the existing oxide defect levels can be calculated more accurately by employing the NMP model.

The charging of oxide defects induces hysteresis of the flatband voltage (V_{fb}) of a MOS Capacitor (MOSCAP), observed by performing double-sweep Capacitance-Voltage curves [14]. A gate-stack comprising InGaAs/Al₂O₃/metal-gate, when subjected to CV-hysteresis measurements in a wide range of temperature (77K to 300K) showed that while ΔV_{fb} is observed to be ~ 20 mV at $T=300\text{K}$ and $E_{\text{OX}} = \sim 7$ MV/cm, it increases to >150 mV at $T=77\text{K}$ for a similar oxide field [14], thereby, demonstrating an apparent non-Arrhenius temperature dependence. A defective interfacial layer was claimed to assist charge trapping/de-trapping into/from oxide defects, through a thermally activated mechanism [14,15]. It has been argued that, as the charging/discharging of interface defects is reduced at $T=77$ K, the charge emission from oxide defects (with the assistance of interface defects) to the channel might be suppressed, thereby resulting in an increased ΔV_{fb} , as compared to that $T=300\text{K}$.

This previously proposed interpretation neglects that the charge capture from interface defects to oxide traps should also be suppressed at lower temperature. Furthermore, the oxide trapping models based on SRH theory stipulate that the charge trapping/emission to/from interface defects is only weakly temperature dependent [13]. Hence, the extent to which oxide traps are charged (or discharged) with assistance from interface defects, should be similar at $T=77$ K and 300 K.

In this paper we show that an increase of the effective density of trapped charge at $T=77$ K, as compared to $T=300$ K, is related to the distribution of activation energies for the oxide defect charge capture and emission processes in the IIIV/high-k gate stack. It can also be noted that the test device used in our study, was observed to have no native oxide layer at the interface between the InGaAs channel and the high-k stack [16]. This is important because the apparent non-Arrhenius temperature dependence is not necessarily a result of interplay

between interface and oxide defects or defects in an unintentionally grown interlayer as argued in [14,15], but related to the presence of bulk oxide defects which have low activation energies for capture and emission. The NMP model can describe the interaction of channel carriers with border traps as well as traps located deeper into the dielectric-stack [12], and reproduce the wide distribution of capture and emission time constants which induces various experimental features such as the frequency dispersion of the capacitance-voltage characteristic in strong accumulation [11] and the complex temperature dependence of charge trapping. The accurate description of the capture and emission activation energy distribution is also crucial to be able to predict the AC and DC responses of the defects under the device operation.

We performed extensive BTI measurements using the standard eMSM technique [17] in order to derive Capture Emission Time (CET) maps [18] and to study the differences in the energy distributions of defects in a typical IIIV/high-k gate-stack. The temporal response of gate-stack defects at different temperatures is studied by measuring the shift in threshold voltage (ΔV_{th}) vs. relaxation time, after stress phases of increasing duration. Extensive eMSM experiments are performed so that information pertaining to ~ 6 orders of stress (up to 10 ks) and relaxation (up to 100 ks) time periods can be obtained to accurately construct the CET maps.

Section II describes the types of devices measured and the experimental procedure implemented to obtain the required information, along with a brief summary of the results obtained from the elaborate experiments. The modeling of BTI data and extraction of analytical CET maps is described in Section III. The atypical temperature dependence of an ensemble of defects in InGaAs gate-stacks, which forms the core of this study, is discussed in Section IV. Finally, the significance of CET maps, its applications in technology projections, and impact on the DC operating lifetime of devices are summarized in Section V. Section VI highlights the final conclusions drawn from extensive experimental data and the synergistic modeling study.

II. EXPERIMENTS AND RESULTS

Quantum-well MOSFETs are used in this study. Device structure (Fig. 1) and fabrication process are the same as that used in [16] with an additional step just before $(\text{NH}_4)_2\text{S}$ passivation treatment in which an optimized number of cycles of a wet-chemistry based digital etch (DE) process (using HCl and H_2O_2) was used to smoothen the rough InP/InGaAs interface [19] and obtain a very smooth channel surface for high-k deposition. The gate-stack comprised a 1nm Al_2O_3

Fig. 1. Structure of the n-type InGaAs quantum well MOSFET used in this work

Fig. 2. (a) IV measurement performed on reference device and a DUT show that there is negligible variability. The $V_{TH,ref}$ is calculated from the “Reference IV” using the max- g_m method. A finely resolved IV with a V_G step of 5 mV is then performed on a fresh DUT to obtain the “Initial IV”, and the $V_{TH,DUT}$ is calculated as the voltage required to reach the same threshold current of the reference device (and hence, $V_{G,sense}$). (b) Voltage waveform applied to the gate of the InGaAs MOSFET under test during an eMSM measurement sequence

interfacial layer, typically deposited on IIIV channels to prevent the formation of detrimental native interfacial oxides [1,6,14], and 3nm HfO_2 . The layers were deposited by ALD at 300 °C, and TMAH and $\text{HfCl}_4/\text{H}_2\text{O}$ were used as precursors for Al_2O_3 and HfO_2 , respectively [20]. The gate metal was formed using PVD TiN, while the S/D contacts were formed using Mo/Al. The devices measured in this study had a gate-length (L_G) of 20 μm and width of 100 μm .

BTI experiments were performed on the MOSFETs at five different temperatures (77K, 233K, 298K, 373K for model calibration, and 150K for model verification) using Keithley K2600 series SMUs. A stress voltage, $V_{G,stress} = V_{th} + 1\text{V}$ was applied on the gate during the stress phase and a sense voltage, $V_{G,sense} = V_{th}$ was applied during the relaxation phase, while the V_{DS} was set to 50 mV throughout the experiment to be able to sense a sizeable channel current. A reference I-V (Fig. 2a) measured on a pristine device, with the same characteristics as the devices-under-test (DUTs), was used to determine a reference threshold voltage ($V_{th,ref}$) using max- g_m method. A fresh DUT was measured at each temperature, and in order to ensure the test devices do not undergo any preliminary stress condition, an “Initial IV” (Fig. 2a) with a restricted V_G sweep range from $V_{th,ref} - 0.4\text{V}$ to $V_{th,ref} + 0.05\text{V}$, was performed to determine the $V_{th,DUT}$, as the voltage required to reach the same threshold current of the reference device. The DUTs were then subjected to BTI stress for time periods ranging from 10 ms to 10 ks, with each stress phase followed by a relaxation phase of appropriate duration (10 ms up to 100 ks) in accordance with the full eMSM measurement scheme shown in Fig. 2b. The drain current measured at a fixed sense V_G (= the fresh device $V_{th,DUT}$) during each relaxation phase from the BTI eMSM experiments, was used to extract the ΔV_{th} [17]. The resulting

Fig. 3. The measured drain current during each of the relaxation phases following a stress phase is processed using Eq. (3) to obtain the ΔV_{th} vs. t_{relax} data. The DUT was stressed for logarithmically increasing stress periods as indicated. Note: Data points at the beginning of some relaxation traces are missing due to the auto-ranging delay of K26xx SMUs

ΔV_{th} vs t_{relax} data are shown in Fig. 3 (black circles) for $T=77$ K, 233 K, 298 K and 373 K.

III. CET MAP MODELING

In order to accurately describe the distribution of defects, it is essential to consider their distribution both in terms of activation energies and capture/emission time constants. Unlike in [21-23], charge trapping into the gate oxide cannot be described solely as a direct tunneling process. There have been numerous reports showing that charge trapping not only depends on the applied gate-bias, but also on the temperature at which the device undergoes the stress condition, as well as the duration (from μ s to months) of the applied stress [4,18,24,25]. As described in [18], the capture (and emission) of an electron into (or out of) a trap is modeled using the non-radiative multiphonon (NMP) model [12], in which the capture and emission time constants are described as,

$$\tau_c = \tau_0 \exp\left(\frac{E_{Ac}}{k_B T}\right) \quad (1)$$

$$\tau_e = \tau_0 \exp\left(\frac{E_{Ae}}{k_B T}\right) \quad (2)$$

where, k_B = Boltzmann constant,

T = Temperature,

τ_0 = effective prefactor,

E_A = effective activation energy

○ Uncharged defect state
● Charged defect state

Fig. 4. The change in the energy and configuration of each defect state is captured by distributing the parameters E_A . The impact of the temperature dependent parameters such as Huang-Rhys factor, lattice relaxation energy and capture cross-section can be captured by modelling an effective E_A with a Gaussian distribution (adapted from [12])

The prefactor (τ_0) and activation energy (E_A) are used to describe the total energy barrier (including the lattice relaxation energy at the defect site [12]) involved in the charge trapping process, and τ_0 incorporates the impact of capture cross-section, which, for example, may affect the extraction of the depth of the trap in the oxide [26]. Eq. 1-2 also show that τ depends exponentially on E_A , as compared to a linear dependence on τ_0 . The analytical formulation of the capture and emission times requires the distribution of parameters, E_{Ac} and E_{Ae} , pertaining to individuality of each defect state (Fig. 4). Hence, the location of defects cannot be determined accurately, as the capture and emission time constants are not solely correlated to tunneling depths [13].

The capture and emission activation energy distribution map is calculated by using a bivariate Gaussian distribution of individual defect's activation energies. It is evident in Fig. 3 that as the temperature was lowered, the relaxation could no longer be described with a single $\log(t_{relax})$ function. The change in slope of the relaxation transients suggests the presence of a multi-modal distribution of activation energies for the charge emission process from different oxide defects, unlike in n-type Si device, where a single $\log(t_{relax})$ trend is observed, and hence, a unimodal distribution can accurately describe the emission process [12]. As will be explained further in this section, it is necessary to account for *at least three* defect distributions in InGaAs/high-k gate stacks. The total ΔV_{th} is calculated by following the process explained in [12,27] and modified to account for the sum of three bivariate gaussian distributions as,

$$\Delta V_{th} = \sum_{i=1}^3 A_i \int_0^{E_c} \int_{E_e}^{\infty} F_{Ri}(E_{Ae}, E_{Ac}) dE_{Ae} dE_{Ac}, \quad (3a)$$

$$F_{Ri}(E_{Ae}, E_{Ac}) = \frac{1}{2\pi\sigma_e\sigma_c\sqrt{1-\rho^2}} \exp\left[-\frac{z}{2(1-\rho^2)}\right] \quad (3b)$$

$$z = \frac{(E_{Ae} - \mu_e)^2}{\sigma_e^2} - \frac{2\rho(E_{Ae} - \mu_e)(E_{Ac} - \mu_c)}{\sigma_e\sigma_c} + \frac{(E_{Ac} - \mu_c)^2}{\sigma_c^2} \quad (3c)$$

$$\rho = \frac{\text{covariance}(E_{Ae}, E_{Ac})}{\sigma_e\sigma_c} \quad (3d)$$

Fig. 5. Optimized distribution map for activation energies of capture and emission process. Each distribution (R_x , $x=1,2,3$) is a PDF of corresponding defect density and is normalized individually to its peak. Color scale may be used to understand the relative height and spread of R_x , while the contribution of individual R_x to total measured ΔV_{th} is summarized in Table I ($\Delta V_{th,max}$)

Table I
OPTIMIZED PARAMETER SET FOR CET MAP MODEL

Parameter	R1	R2	R3
$\langle E_{Ac} \rangle$	0.893 eV	0.211 eV	0.046 eV
σ_{Ec}	0.399 eV	0.08 eV	0.029 eV
$\langle E_{Ae} \rangle$	1.002 eV	0.157 eV	0.141 eV
σ_{Ee}	0.45 eV	0.149 eV	0.017 eV
τ_0	22.41 ns	0.93 ns	70.55 ns
$\Delta V_{th,max}$	0.598 V	0.214 V	0.045 V

where, F_{Ri} = bivariate Gaussian probability distribution function (Eq. 3b-3d), E_{Ac} and E_{Ae} = effective activation energies corresponding to stress and relaxation time periods during the eMSM experiment, $\mu_{c,e}$ = mean of F_{Ri} and $\sigma_{c,e}$ = standard deviation of F_{Ri} for capture and relaxation activation energies respectively, and A_i = pre-factors for normalization, corresponding to total defect density of each sub-population.

The activation energies, E_{Ac} and E_{Ae} used in the Eq. 3(a-d) can be calculated from Eq. 1 and 2. The ΔV_{th} calculated in Eq. 3 can be described as the total contribution of defects that have been charged in a stress phase of duration t_s , (i.e., defects whose capture time constants $\tau_c < t_s$), while they have not yet discharged during the relaxation phase of duration t_r (i.e., defects whose emission time constants $\tau_e > t_r$). The parameters of the three bivariate distributions were numerically optimized to reproduce the experimental data. Fig. 5 shows optimized combination of the three bivariate Gaussian distributions of activation energies, and the corresponding parameter set is summarized in table I. Asymmetry between capture and emission activation energies, which is clearly observable at 77K (Fig. 3a), is also evident from the unequal spread of $R_{1,2,3}$ around the $E_{Ac}=E_{Ae}$ symmetry line in Fig. 5. The ΔV_{th} calculated from the activation energy map of Fig. 4 at the four temperatures (77 K, 233 K, 298 K, 373 K) are shown to reproduce the experimental data remarkably well in Fig. 3 (red lines).

IV. DISCUSSION

It is apparent from Fig. 5 that there are three distinct activation energy distributions that govern the charge trapping in the InGaAs/Al₂O₃/HfO₂ gate-stack. Note that CET map obtained for Si nMOS showed a single defect population [12,28], while the CET map obtained for Si pMOS device in [12,18], showed two distributions of defects, with the second one corresponding to very slow defects with large activation energies (so-called ‘permanent’ component). All three distributions observed in Fig. 5 for InGaAs devices show relatively low activation energies, within the range of the so-called ‘recoverable’ component observed in Si devices (and thus, are labeled as Recoverable₁ (R1), Recoverable₂ (R2), and Recoverable₃ (R3)).

The CET maps are calculated by converting the distribution of activation energies for capture (E_{Ac}) and emission (E_{Ae}) into the corresponding capture and emission times (τ_c and τ_e respectively) using Eq. 1 and Eq. 2, exposing the temperature dependence of the charge trapping process. Fig. 6 shows the CET maps calculated at the four temperatures used in the experiments, and considered for the model calibration. The region marked as ‘measurement window’ in the maps denotes the part of the distributions that contributes to the measured ΔV_{th} while the other region (‘Out of measurement window’) comprises the traps that are either too slow to capture an electron in the experimental window, or they have emission times smaller than the minimum measurement delay.

At 373 K (Fig. 6d), it can be observed that the R2 and R3 components of the total distribution are too fast and cannot be sensed within the ‘measurement window’. All the defects with energy states that lie within the R2 and R3 components capture an electron, but since they also have very small emission time constants, they emit the trapped electron before the first measurement is performed (~10 ms). This delay in measurement of the first relaxation point, also defined here as sense delay (t_{sense}), is crucial to accurately determine the total

Fig. 6. The capture and emission time (CET) maps can be calculated using Eqs. (4) and (5) for different temperatures. The region marked as ‘Out of measurement window’ represents the part of the total distribution that cannot be observed in the experimental window, while the region marked as ‘Measurement window’ represents the defect states that are observed to emit the trapped electrons during the relaxation phase. Each distribution (R_x , $x=1,2,3$) is a PDF of corresponding defect density and is normalized individually to its peak. Color scale may be used to understand the relative height and spread of R_x , while the contribution of individual R_x to total measured ΔV_{th} is summarized in Table I ($\Delta V_{th,max}$)

distribution. If t_{sense} is made too large, then R2 can no longer be measured (for example, if $t_{\text{sense}} \geq 100$ ms at $T=298$ K, in Fig. 6c) and the emission characteristics are dominated by the R1 component. This might lead to an apparently incorrect conclusion that since only one slope is observed in the relaxation transient (as seen in Fig. 3d, for $T=373$ K), there is only one wide distribution of energy states, and therefore a single $\log(t)$ function is adequate to describe the defect distribution in the gate-stack. However, by measuring the gate-stack at lower temperatures, for example at $T=233$ K and with $t_{\text{sense}} \geq 10$ ms (Fig. 6b), the defect states within the R2 component become dominant contributors to the ΔV_{th} (cf. Eqs. (1-2)), while the time constants of the majority of the defect states within the R1 component shift out of the measurement window, and therefore do not contribute to the measured ΔV_{th} .

On further lowering the temperature to 77 K, one would expect negligible ΔV_{th} since both the R1 and R2 components have much larger capture and emission time constants and there should be negligible interaction of electrons with these defects. However, it has been reported earlier [15] that at 77 K, the effective charge trapping in the gate-oxide (ΔN_{eff}) increases as compared to that observed at 300 K. We also observe here that $\Delta V_{\text{th}} @ t_{\text{relax}} \sim 10$ ms is similar to that obtained at $T=233$ K (cf. Fig. 3a and 3b). Another striking feature of the relaxation trend of ΔV_{th} at $T=77$ K is the change in slope at $t_{\text{relax}} \sim 100$ s (Fig. 3a) after the start of the relaxation phase. These observations point towards the presence of a *third* defect population with extremely low capture and emission energy barriers, making this defect population active in the ‘measurement window’ only at T as low as 77 K. More importantly, a narrow emission energy distribution with $\sigma_{\text{Ee}} < \sigma_{\text{Ec}}$ is expected as most of the

relaxation occurs in less than 3 decades in time, while the capture process is observed to be active for more than 6 decades in time.

Since, the low activation energy barriers for R3 result in extremely small capture and emission time constants at 300 K, the possibility that R3 represents an interface trap population rather than an oxide trap population, may also be considered. Charge trapping in defects at the semiconductor/oxide interface is commonly explained using the SRH model [29]. The time constants describing the kinetics of charging/discharging of interface states in the bandgap are given by [29],

$$\tau = \frac{\exp(\Delta E/k_B T)}{\sigma v_{\text{th}} D_{\text{dos}}} \quad (4)$$

where ΔE is the energy difference between trap level E_{trap} and majority carrier band edge E_{CB} , σ (10^{-16} cm²) the capture cross section of the trap, v_{th} (5.6×10^7 cm/s) the average thermal velocity of the majority carriers, D_{dos} (2.2×10^{17} cm⁻³) the effective Density Of States of the majority carrier band, k_B the Boltzmann constant, and T the temperature. It was shown in [15,30,31] that density of interface states increases deeper into the InGaAs bandgap, which should therefore, result in larger τ (possibly falling within the ‘measurement window’) and increased contribution to ΔV_{th} at low temperatures. Consequently, the interface states in the InGaAs bandgap are relevant to our discussion, while the interface states above the E_C of InGaAs act as free conduction band states with $\tau < 1$ ns (from Eq. 4) and would not be active in the ‘measurement window’ (10ms to 10 ks).

The interface states that are expected to interact with channel carriers during the BTI experiment, when $V_{\text{G,sense}} = V_{\text{TH}} \approx V_{\text{FB}}$, (or, $E_{\text{ox}} = 0$ MV/cm), are limited to those with thermal energy difference of one $k_B T$ (~ 6.6 meV at $T=77$ K) from the Fermi level. Eq. 4 suggests that the effective $\langle \tau \rangle$ for these interface states is ~ 2.2 ns. R3 is observed to be active in the ‘measurement window’ (10ms to 10ks) at $T=77$ K, with μ_{EAe} and μ_{EAc} of ~ 46 meV and ~ 141 meV respectively. Hence, it is evident that R3 does not correspond to interface defects as the activation energies for capture and emission to/from the interface defects, as well as their effective $\langle \tau \rangle$ falls outside the window where R3 is observed.

BTI measurements were also performed at $T=150$ K. Fig. 7a shows the CET map obtained for $T=150$ K with the optimized set of parameters from Table I. The R2 and R3 components are seen to move into the measurement window (region with $\tau_c < 10$ ks and $\tau_e > 10$ ms) in accordance with the NMP model. ΔV_{th} vs. t_{relax} calculated from Fig. 7a is shown in Fig. 7b (red lines) along with the measurement results. An excellent match is obtained between the calculation of the CET map model and the experimental data (not used for the model calibration), *without further adjusting any of the model parameters*. In order to validate the consistency of the CET map calibration procedure, we re-calibrated our activation energy map to the datasets pertaining to $T=77$ K, 150 K, 233 K and 298 K: similar distributions of R1, R2, and R3 were obtained (not shown), as proven by an excellent match between the extrapolation to $T=373$ K (based on this second calibration), and the experimental data pertaining to $T=373$ K (not used for this alternative calibration). This result further shows the accuracy of NMP theory to model charge trapping into oxide defects (i.e.,

Fig. 7 a) CET map calculated from the energy distribution map (cf. Fig. 4) for $T=150$ K. The region marked as ‘measurement window’ again shows the part of the total distribution that contributes to the observed ΔV_{th} . b) Plot showing the experimental data (symbols) along with the results obtained from the CET map model for $T=150$ K. It can be seen that the model accurately predicts the experimental data (note: the data pertaining to $T=150$ K were not used to calibrate the model parameters)

Fig. 8. When t_{stress} is small (< 10 ms), a *quasi-inverse* Arrhenius temperature dependence is observed. When the t_{stress} is increased (~ 100 ms to ~ 10 s), there is a transition point which indicates that all the defect states within R3 component are captured and some defect states within the R1 and R2 components start to contribute to ΔV_{th} . There is *negligible* temperature dependence in this stress time range. On further increasing t_{stress} (> 10 s), R2 and R3 components are always charged at all temperatures, while R1 is the dominant distribution, resulting in *quasi-Arrhenius* dependence. Symbols correspond to experimental data obtained at each temperature

temperature dependent inelastic tunneling process which requires additional energy from phonons). We conclude that R3 corresponds to a peculiar oxide trap population existing in the InGaAs/high- k gate stack, while further investigation may be required to determine the microscopic nature of these traps.

V. IMPACT ON DC OPERATING LIFETIME

The apparent non-Arrhenius temperature dependence of gate-stack defects [15] can be understood as a consequence of the presence of the three (partially overlapping) defect populations. The fraction of the defect populations observable within the sensing window does not satisfy the Arrhenius law over a large temperature and stress time window. When we consider the CET map at $T=298$ K (Fig. 6c), it can be seen that for short t_{stress} (< 1 ms), only the defect states within R2 and R3 components can capture and emit electrons. Since R2 and R3 are overlapping trap populations with different temperature dependences (different τ_0 , cf. Table I), they show a *quasi-inverse* Arrhenius temperature dependence (Fig. 8). When the t_{stress} is increased (~ 100 ms to ~ 10 s), there is a transition point which indicates that all the defect states within R3 component are always occupied and part of the defect states within the R1 and R2 component start to contribute to ΔV_{th} . There is *negligible* Arrhenius dependence for these stress durations. On further increasing t_{stress} (> 10 s), R2 and R3 components are always charged at all temperatures, while R1 is the dominant distribution, dictating the V_{th} shift kinetics. Hence, the expected *quasi-Arrhenius* dependence is observed. This shows that only when a limited temperature and stress time window are considered, an ensemble of defects would demonstrate a *quasi-Arrhenius* dependence.

Another aspect that becomes evident from the CET maps is the importance of t_{sense} . Fig. 9 shows the impact of t_{sense} on the observed ΔV_{th} . As described earlier, increasing the t_{sense} lowers the sensitivity to fast charging/discharging defect states (in R2 and R3 components). It can be noticed that when the t_{sense} is 1 ns, a much larger ΔV_{th} would be observed, due to the contribution of the fast defects. With a $t_{\text{sense}} = 50$ ms (red dashed line in Fig.

Fig. 9. The sensing delay (t_{sense}) is important to see the impact of the trapping in the defect states within Recoverable₁ component. As t_{sense} is increased, defect states in R2 and R3 shift out of the observation window and only those in R1 contribute to ΔV_{th} , thereby, eliminating the contribution of fast defect population (for $t_{\text{stress}} < 1$ ms)

9), the defect states of R2 and R3 components will always get charged during stress, but will also get discharged before the measurement starts during every relaxation phase. There is approximately 2x difference between the $\Delta V_{\text{th},10 \text{ yrs}}$ with $t_{\text{sense}}=50$ ms and the $\Delta V_{\text{th},10 \text{ yrs}}$ with $t_{\text{sense}}=1$ ns. Hence, it becomes important to characterize InGaAs devices over a wide range of temperatures, not only to understand the quasi-inverse Arrhenius temperature dependence of gate-stack, but also to obtain the total defect distribution, including the fast states which would be missed in standard delayed measurements, as this is needed to accurately predict the lifetime of these devices under realistic AC operating conditions.

VI. CONCLUSIONS

We have reported extensive BTI measurements in the InGaAs/ $\text{Al}_2\text{O}_3/\text{HfO}_2$ gate-stack for a wide temperature range and modelled the distribution of activation energies for the capture and emission of channel carriers into/from oxide defects, and the corresponding Capture-Emission-Time maps. The optimized CET map was used to predict ΔV_{th} vs. t_{relax} at $T=150$ K: the calculation was shown to match excellently with the experimental data measured at 150K for verification. We conclude that there are *three* defect populations which can be described with three bivariate Gaussian distributions of capture/emission activation energies for defects inside the bulk of the gate-stack. The quasi-inverse Arrhenius temperature dependence observed during hysteresis and BTI measurements is shown to be a result of the presence of these three defect populations. The fastest component (R3) had emission time constants spanning over three decades in time and hence, could not be described as interfacial defects, which according to SRH theory should show very narrow distribution of emission time constants and negligible charging time constants. Finally, the impact of the sense delay (t_{sense}) was described to highlight the impact of the fast R2 and R3 components on the measured ΔV_{th} .

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