Citation	Wouter Diels, Michiel Steyaert, Filip Tavernier (2019) Advanced Design of Schottky Photodiodes in Bulk CMOS for High Speed Optical Receivers IEEE Journal of Quantum Electronics, vol. 56, no. 1, pp. 1-8, Feb. 2020
Archived version	Author manuscript: the content is identical to the content of the published paper, but without the final typesetting by the publisher
Published version	https://ieeexplore.ieee.org/document/8933051
Journal homepage	https://www.photonicsociety.org/publications/journal-of-quantum-electronics
Author contact	wouter.diels@esat.kuleuven.be

(article begins on next page)

Advanced Design of Schottky Photodiodes in Bulk CMOS for High Speed Optical Receivers

Wouter Diels, *Student Member, IEEE*, Michiel Steyaert, *Fellow, IEEE*, and Filip Tavernier, *Member, IEEE*

Abstract—This paper provides theoretical insight on how circular Schottky photodiodes in bulk CMOS can be optimized for certain integrated receiver applications. An optimal photodiode size is analytically demonstrated and the effects of a metal plate reflector are simulated using a transfer-matrix method, both for frontside and backside illumination. Finally, a distributed circuit model is presented, which deviates from the classical lumped model for large photodiodes or sheet resistances. The presented methodologies can also be extended to other types of photodetectors.

Index Terms—CMOS integrated circuits, circuit modeling, Schottky diodes, photodetectors, optical fiber communication.

I. INTRODUCTION

RESEARCH on integration of electro-optics in a process with economic potential for high volume manufacturing such as CMOS is desirable both for multi-mode fiber (MMF) and single mode fiber (SMF) applications. Within receiver applications, 850 nm light for MMF links can readily be detected with PN-photodiodes (PDs) by means of the photoelectric effect in silicon: photons excite electrons from the valence to the conduction band and the resulting electron-hole pair is swept by the electric field in the depletion region of the PN-junction. This has resulted in numerous demonstrations of 850 nm CMOS optical receivers [1]–[6]. However, the relatively large band gap of silicon (1.1 eV) prevents absorption for photons with wavelengths longer than 1.1 μm , meaning that a different type of photodetector is required for the typical SMF communication wavelengths, such as those around 1310 and 1550 nm. One solution has been exploiting the SiGe layer used to strain PMOS transistors, which has yielded (resonant) waveguide photodetectors in silicon-on-insulator (SOI) CMOS with a responsivity up to 0.5 A/W at 1310 nm [7]–[9]. Alternatively, instead of using the SiGe layer, absorption can also be achieved by introducing defects in a (poly)silicon waveguide by means of heavy doping [10]. Another approach, which is also viable for bulk CMOS processes, has made use of internal photoemission (IPE) in Schottky PDs [11]–[13], in which hot electrons in the metal/silicide can cross the Schottky barrier after being excited by photons [14], [15]. All these types of photodetectors do not have modeling in the process design kit (PDK) and have to be modeled one way or another in order to build circuits around them. In [13], a lumped circuit model was proposed for Schottky PDs in various bulk CMOS technologies. Based on measurements of N- and P-type Schottky PDs with a diameter of 26 and 60 μm , process-specific characteristics such as the dark-current-per-area, capacitance-per-area and responsivities for 1310 and 1550 nm were presented. No information was

provided, however, on how to optimally design these devices for specific applications. In this paper, more insight is given on how these devices can be engineered and modeled, given these process-specific parameters. Particularly, optimization of the PD size and the implications of having a metal plate on top of the PD are discussed. Furthermore, a rigorous distributed circuit model is also presented, which provides better accuracy than the lumped circuit model when the silicon sheet resistance of the photodiode is large.

II. SCHOTTKY PHOTODIODE DESIGN

Schottky diodes can be realized in a bulk CMOS process by having lowly doped silicon regions, such as N-well, P-well or P-substrate silicided, forming a silicide-silicon junction in the process [16]. A cross-section of an N-Well Schottky photodiode can be seen in Fig. 1. For an N-type (P-type) diode, the silicide region above the lowly doped silicon forms the cathode (anode), while the lowly doped silicon itself forms the anode (cathode). A strip of silicide in highly doped silicon (N+/P+ regions) around the Schottky junction creates an Ohmic contact to the silicon. Lowly and highly doped silicide areas are isolated by shallow trench isolation (STI). For IPE-based Schottky detectors, light with an energy lower than the band gap energy is absorbed in the very thin (~ 10 nm) silicide layer. A fraction of the resulting excited electrons can then cross the Schottky barrier and contribute to photocurrent. P-type Schottky diodes tend to have a smaller Schottky barrier compared to N-type diodes due to Fermi pinning [17]. While this leads to an increased responsivity, the dark current and the associated shot noise also increase exponentially. For this reason, Schottky PDs in actual receivers are typically N-type. However, the analyses in this paper are valid for both N- and P-type.

Fig. 1: Cross-section of an N-well Schottky photodiode

A. Photodiode area optimization

The area of the photodetector directly determines electrical circuit properties such as the PD capacitance and its dark current. The latter also influences the small-signal resistance and shot noise density. From this point of view, it makes sense to minimize the area. However, the primary objective should be to capture the incoming light as much as possible. To this end, it makes sense to maximize the area. Therefore, there must exist an optimum area for a given light profile.

Consider the circuit and its small-signal equivalent schematic in Fig. 2. It represents a Schottky PD with a simple transimpedance (TI) resistor to convert the current into a voltage. While in practical receivers this conversion is usually performed with a transimpedance amplifier (TIA) e.g. a voltage amplifier in a resistive feedback configuration, a TI resistor yields more intuitive expressions. Furthermore, as far as diode optimization is concerned, a TI resistor and TIA render the same results. In this schematic C_d is the diode capacitance, r_d is the diode resistance, R_s is the diode series resistance and R_{ti} is the TI resistance. The spectral density of the diode shot noise $\overline{i_n^2}$ is written down in (1).

Fig. 2: Equivalent circuit of photodiode and simple TI resistor

$$\overline{di_n^2}(f) = 2q(I_{dark} + I_{PD})df \quad (1)$$

The AC transfer function of the output voltage v_R can be seen in (2). A certain design bandwidth BW fixes the TI resistance (3). For this analysis, it is more insightful to assume zero series resistance R_s and infinite diode resistance r_d .

$$v_R = \frac{\frac{R_{ti}r_d}{R_s + R_{ti} + r_d} i_{pd}}{1 + \frac{r_d(R_s + R_{ti})C_d s}{R_s + R_{ti} + r_d}} \quad (2)$$

$$R_{ti} = \frac{R_s + r_d - 2\pi BW r_d R_s C_d}{2\pi BW r_d C_d - 1} \approx \frac{1}{2\pi BW C_d} \quad (3)$$

Assuming the circuit bandwidth is approximate to that of the intended signal, the magnitude of the output voltage V_{R0} can be expressed as in (4). The photocurrent i_{pd} can be written down as the product of the PD responsivity $\mathcal{R}$ and the optical power absorbed in the PD plane P_{pd} .

$$V_{R0} \approx R_{ti} i_{pd} = \frac{\mathcal{R} P_{pd}}{2\pi BW C_d} \quad (4)$$

The RMS noise voltage at this node is expressed by (5), where k is the Boltzmann constant, T is the absolute temperature and q is the elementary charge. The first term indicates the integrated noise due to the TI resistor itself, while the second term is due to the diode shot noise. As the responsivity of Schottky PDs is relatively low, in high speed receivers, the

total integrated noise is likely dominated by that of the resistor. As such, the second term in (5) can be omitted altogether. However, in order to boost the signal current, the responsivity can be increased by raising the diode bias, even to the point that the dark current exceeds the signal current and its shot noise becomes significant [13]. In this case, the diode shot noise contribution due to the DC photocurrent I_{PD} can be omitted.

$$v_{n,RMS} \approx \sqrt{\frac{kT}{C_d} + \frac{q(I_{dark} + I_{PD})}{4\pi BW C_d^2}} \quad (5)$$

In the case of circular photodiodes, P_{pd} is defined as in (6), where I is the light irradiance in the PD plane in polar coordinates and D is the PD diameter.

$$P_{pd} = \int_0^{D/2} \int_0^{2\pi} I(r, \theta) r d\theta dr \quad (6)$$

C_d and I_{dark} can be defined as in (7) and (8) with C_A and I_A the capacitance-per-area ratio and dark-current-per-area ratio respectively.

$$C_d = C_A \pi D^2 / 4 \quad (7)$$

$$I_{dark} = I_A \pi D^2 / 4 \quad (8)$$

With all expressions defined now, after taking the ratio between (4) and (5), it can be observed that the dependence of the resulting signal-to-noise ratio (SNR) to the diode diameter is as in (9). Therefore, the optimum PD diameter of this term also yields an optimum SNR. The objective function can now be optimized for any light profile.

$$SNR = \frac{V_{R0}}{v_{n,RMS}} \propto \frac{P_{pd}(D)}{D} \quad (9)$$

1) *Uniform light profile*: Because of its simplicity, this irradiance profile is widely used and can be described by (10), where B is the beamwidth of the light and P_{in} is the total optical power in the PD plane. The objective function can then be written as in (11), which reaches a maximum when the PD diameter is equal to the light beamwidth.

$$I(r, \theta) = \begin{cases} \frac{4P_{in}}{\pi B^2} & \text{if } 0 \leq r \leq B/2 \\ 0 & \text{if } r > B/2 \end{cases} \quad (10)$$

$$\frac{P_{pd}}{D} = \begin{cases} \frac{P_{in} D}{B^2} & \text{if } 0 \leq D \leq B \\ \frac{P_{in}}{B^2} & \text{if } D > B \end{cases} \quad (11)$$

2) *Gaussian light profile*: This profile very much resembles the mode profile of a SMF and can be defined as in (12) [18]. In this case, the beamwidth B represents the diameter at which the irradiance has dropped to $1/e^2$ compared to the maximum. The objective function is given in (13), which again reaches a maximum. The optimum photodiode diameter is given in (14), where W_n is the n^{th} branch of the Lambert W function. Both profiles and their objective functions are summarized in Fig. 3. Finally, it can be noted that while a Gaussian profile requires a lower PD size, the optimum itself is larger for the uniform profile.

$$I(r, \theta) = \frac{8P_{in}}{\pi B^2} e^{-\frac{8r^2}{B^2}} \quad (12)$$

$$\frac{P_{pd}}{D} = P_{in} \frac{1 - e^{-\frac{2D^2}{B^2}}}{D} \quad (13)$$

$$D_{opt} = \sqrt{-2W_{-1}\left(-\frac{1}{2\sqrt{e}}\right) - 1} \frac{B}{2} \approx 0.79B \quad (14)$$

Fig. 3: (a) Uniform and Gaussian light profiles (b) Objective functions for uniform and Gaussian light profiles

Schottky PDs in bulk CMOS are intended to be vertically surface illuminated via a butt coupled SMF. Therefore, the PD diameter should be matched to the beamwidth of the irradiance profile in the diode plane in accordance with (14). Fig. 4 shows the simulated beamwidth for a silica SMF with a numerical aperture (NA) of 0.14 and a core diameter of 8 μm . When the light exits the fiber, the Gaussian beam diverges and the beamwidth increases for a traveled distance z as in (15), where B_0 is the beamwidth after exiting the fiber, λ_0 is the wavelength in free space and n is the refractive index of the material in which the light travels.

$$B(z) = B_0 \sqrt{1 + \left(\frac{4\lambda_0 z}{\pi n B_0^2}\right)^2} \quad (15)$$

If the light is sent to a CMOS Schottky photodiode through the silicon substrate (backside illumination - BSI), which is typically 300 μm thick, the beamwidth at the diode plane is between 19 and 21 μm for the wavelength range in Fig 4. When frontside illumination (FSI) is applied, the light has to cross the stack of dielectric layers, which is only approximately 10 μm . While the optimum photodiode diameter is thus lower for FSI than for BSI, there are nevertheless other arguments to opt for BSI, as discussed in the next sections.

B. Light absorption optimization

The IPE quantum efficiency of Schottky PDs, which is also proportional to the responsivity can be written down as the product of three terms as in (16) [19].

$$\eta = \frac{h\nu}{q} \mathcal{R} = A_{abs} F P \quad (16)$$

Fig. 4: Beamwidth for a silica SMF with 0.14 NA and 8 μm core diameter, simulated with Comsol

The first term A_{abs} represents the fraction of the incident light which actually gets absorbed, the second term F is the fraction of how many excited carriers have appropriate momentum and energy to cross the Schottky barrier and the last term P is a scattering term which takes into account the probability that hot carriers can still cross the barrier after scattering with cold carriers and metal boundary surfaces. The quantum efficiency and responsivity of the Schottky PD can thus be optimized by maximizing the absorption ratio in or near the silicide. This ratio can easily and accurately be simulated in a finite element simulator such as Comsol or Lumerical. A computationally more efficient way to simulate this ratio is the transfer matrix method (TMM) [20]. Using the layers' complex refractive index and thickness, global reflection, transmission and absorption coefficients can be calculated for any given angle and polarization. In the case of Schottky photodiodes, only vertical illumination is of interest. The PDK provides information on dielectric layer thickness and dielectric constant, which is critical for RF designs in CMOS. However, as no material dispersion information is disclosed, the validity of these constants at optical frequencies remains uncertain. No information on the silicide material or thickness is disclosed. For the TMM simulations, NiSi was assumed with a thickness of 10 nm, as TiSi_2 and CoSi_2 are no longer used in deeply scaled CMOS technologies below 50 nm [21]. The refractive indices of NiSi were obtained from [22], while those of Si, Cu and Au were found in [23].

Fig. 5: Transfer-matrix setup for (a) BSI of flip-chipped CMOS chip on PCB (b) FSI of wire-bonded CMOS chip on PCB

1) *Backside illumination:* Backside illumination can be practically achieved by having the chip containing Schottky PDs flip-chip bonded. The TMM setup for this situation can be seen in Fig. 5(a). The resulting absorption ratio of these

situations for the dielectric stack of a 28 and 40 nm CMOS process can be seen in Fig. 6. As can be seen, all internal reflections lead to a rather chaotic profile. The relatively thick 300 μm substrate leads to beats with a small period of less than a nanometer, while the relatively thin dielectric stack results in beats with a period of tens of nanometer. The dielectric stacks of the different technologies also result in absorption notches at different wavelengths.

Fig. 6: Simulated absorption ratio for the above BSI setup for a (a) 28 nm CMOS dielectric stack (b) 40 nm CMOS dielectric stack

By placing a copper plate in the metal layer closest to the silicide (M1), the effect of the dielectric stack can be greatly circumvented as seen in Fig. 7. Furthermore, wafer thinning reduces the beat period significantly, as demonstrated by the simulations in Fig. 8, where the substrate thickness is reduced to 50 μm . The reduced thickness leads to a beat period of around 5 nm.

2) *Frontside illumination*: Frontside illumination is well suited for wire-bonded chips, the TMM setup is displayed in Fig. 5(b). Fig. 9 shows the TMM simulation results for FSI with the dielectric stack of a 28 and 40 nm CMOS process both without the M1 plate. In this case, the chaotic double beat pattern can again be observed.

Placing a M1 plate is counterproductive as most light gets reflected, which can be seen in Fig. 10. Furthermore, the little amount of light that is not reflected gets absorbed in the M1 plate. The probability of these hot electrons crossing the Schottky barrier is low. This explains why the measured FSI responsivity of the Schottky photodiodes with M1 plate in [11] is so low compared to BSI.

In these simulations, the silicide thickness was estimated 10 nm by mapping the silicide sheet resistance in the PDK to the resistivity of Si_3N_4 . However, as there remains uncertainty on the actual thickness, TMM simulations were also performed for other thicknesses. The upper and lower envelopes of the

Fig. 7: Simulated absorption ratio for BSI with M1 plate for (a) 28 nm CMOS dielectric stack (b) 40 nm CMOS dielectric stack

Fig. 8: Simulated absorption ratio for BSI with M1 plate and 50 μm substrate for 28 nm CMOS dielectric stack

Fig. 9: Simulated absorption ratio for FSI without M1 plate for (a) 28 nm CMOS dielectric stack (b) 40 nm CMOS dielectric stack

Fig. 10: Simulated absorption ratio for FSI with M1 plate for 28 nm CMOS dielectric stack

BSI absorption spectrum of a Schottky PD with M1 plate for various thicknesses can be seen in Fig. 11.

Fig. 11: Simulated absorption envelopes for BSI with M1 plate with various silicide thicknesses for (a) 28 nm CMOS dielectric stack (b) 40 nm CMOS dielectric stack

When comparing BSI and FSI, it should be noted that BSI for Schottky PDs with a M1 plate is most robust. The metal plate minimizes the impact of the unpredictable process dependent dielectric stack, which is inevitable for FSI. Furthermore, glue and other imperfections during wire-bonding can scatter the light, resulting in reflected light not reaching the silicide again. It should also be noted that the TMM assumes plane waves, whereas actual light has a divergence angle, meaning photons drift away from the photodiode silicide after some reflection cycles. However, as demonstrated by the measurement results in Fig. 12, which were performed on a Schottky PD with M1 plate in 28 nm CMOS and an O-band tunable laser, the TMM is at the very least indicative. Of course, this responsivity measurement is not directly proportional to the absorption ratio as it also contains the other two terms of the IPE quantum efficiency expression in (16).

Fig. 12: Measured spectral response of Schottky PD with M1 plate in 28 nm CMOS technology for BSI

III. SCHOTTKY PD DISTRIBUTED CIRCUIT MODEL

The lumped circuit model, as in Fig. 2, is popular because of its simplicity and because it can readily be implemented in circuit simulators. However, as will be shown in this section, it can result in inaccuracies. This is due to the series resistance, which in the lumped model only takes into account the outer circular surface of the Schottky PD underneath the STI and not the silicide and N-well resistances in the PD itself.

Fig. 13: (a) Infinitesimal slab of circular surface (b) Distributed circuit model of circular photodiode

Consider the thin infinitesimal slab of a circular surface as in Fig. 13(a). In a polar coordinate system, it has a width $rd\theta$, length dr and thus area $rd\theta dr$. Assuming the slab has a certain electrical resistivity ρ and thickness t , Pouillet's law yields the slab's resistance dR from inside to outside as (17), where $R_{\square}$ is the sheet resistance of the material layer.

$$dR = \frac{\rho}{t} \frac{dr}{rd\theta} = R_{\square} \frac{dr}{rd\theta} \quad (17)$$

In the case of a full circular strip, all slabs for each $d\theta$ are connected together in parallel. The equivalent circular strip resistance per unit length can be found by integrating over θ as in (18).

$$dR_{eq} = \frac{1}{\int_0^{2\pi} \frac{1}{dR}} = R_{\square} \frac{dr}{2\pi r} \quad (18)$$

With this information, a distributed electrical model of the circular PD in Fig. 1 can now be found in function of the radial axis r . It is shown in Fig 13(b). In this figure, $R_{\square 1}$ and $R_{\square 2}$ correspond to the silicide and N-well sheet resistances, while g_A is the small-signal linearized diode conductivity-per-area ratio. From this figure, a system of ordinary differential equations can be found, as in (19).

$$\begin{cases} \frac{dV(r)}{dr} = \frac{R_{\square 1}}{2\pi r} I_1(r) + \frac{R_{\square 2}}{2\pi r} I_2(r) \\ \frac{dI_1(r)}{dr} = 2\pi r C_A s V(r) + 2\pi r g_A V(r) + 2\pi r i_{pd}(r) \\ \frac{dI_2(r)}{dr} = 2\pi r C_A s V(r) + 2\pi r g_A V(r) + 2\pi r i_{pd}(r) \end{cases} \quad (19)$$

The Schottky PD in Fig. 1 corresponds to the initial conditions in (20), which dictate that in the center, current can only flow outwards or through the diode and that the voltage over the PD is only fixed at the outer circular edge. The system yields the solutions in (21), where γ is defined as $\sqrt{-(R_{\square 1} + R_{\square 2})(g_A + sC_A)}$.

$$\begin{cases} V(D/2) = V_{diode} \\ I_1(0) = 0 \\ I_2(0) = 0 \end{cases} \quad (20)$$

$$\begin{cases} I_1(r) = I_2(r) \\ = r\pi^2 Y_1(\gamma r) \int_0^r x J_1(\gamma x) \frac{di_{pd}(x)}{dx} dx \\ - r\pi^2 J_1(\gamma r) \int_0^r x Y_1(\gamma x) \frac{di_{pd}(x)}{dx} dx \\ + Kr J_1(\gamma r) \\ V(r) = \frac{\pi\gamma Y_0(\gamma r) \int_0^r x J_1(\gamma x) \frac{di_{pd}(x)}{dx} dx}{2(g_A + sC_A)} \\ - \frac{\pi\gamma J_0(\gamma r) \int_0^r x Y_1(\gamma x) \frac{di_{pd}(x)}{dx} dx}{2(g_A + sC_A)} \\ + K\gamma \frac{J_0(\gamma r)}{2\pi(g_A + sC_A)} - \frac{i_{pd}(r)}{g_A + sC_A} \\ K = \pi^2 \int_0^{D/2} x Y_1(\gamma x) \frac{di_{pd}(x)}{dx} dx \\ - \pi^2 \int_0^{D/2} x J_1(\gamma x) \frac{di_{pd}(x)}{dx} dx \frac{Y_0(\gamma D/2)}{J_0(\gamma D/2)} \\ + \frac{2\pi i_{pd}(D/2) + 2\pi(g_A + sC_A)V_{diode}}{\gamma J_0(\gamma D/2)} \end{cases} \quad (21)$$

These solutions reveal the current and voltage in function of the radial axis. In practice, of main interest is the current flowing in and out the PD at the outer edge terminals $I_{diode} = I_1(D/2) = I_2(D/2)$ as shown in (22).

$$\begin{aligned} I_{diode} &= \frac{\pi D J_1(\gamma D/2) (i_{pd}(D/2) + (g_A + sC_A)V_{diode})}{\gamma J_0(\gamma D/2)} \\ &+ \frac{\pi^2 D \gamma \int_0^{D/2} x J_1(\gamma x) \frac{di_{pd}(x)}{dx} dx}{2\gamma J_0(\gamma D/2)} \\ &* (Y_1(\gamma D/2) J_0(\gamma D/2) - J_1(\gamma D/2) Y_0(\gamma D/2)) \end{aligned} \quad (22)$$

The distributed model is only valid for the area directly above and under the photodiode. However, in reality there is an additional purely resistive circular path in the N-well through STI to reach the cathode terminal. Using a similar approach, one can find that this ring has an equivalent resistance of $R_{\square 3} \log(r_2/r_1)/2\pi$, where r_1 and r_2 are the inner and outer radii of the surface respectively and $R_{\square 3}$ is the sheet resistance of N-well with STI. When measuring the I-V characteristics of a Schottky photodiode, this resistance determines the slope in the forward biasing region and is thus perceived as the series resistance R_s . This explains why the measured series resistance is smaller for a larger photodiode [11], [13]. The solution (22) can now be used in circuits, both for signal and noise simulations. For example, the Schottky photodiode connected to a TI resistor now yields the output voltage expression in (23), where $\delta \equiv \sqrt{-(R_s + R_{ti})(g_A + sC_A)}$.

$$\begin{aligned} v_{out, TI} &= \frac{2\pi D R_{ti} i_{pd}(D/2) J_1(\gamma D/2)}{2\gamma J_0(\gamma D/2) - 2\pi D \delta^2 J_1(\gamma D/2)} \\ &+ \frac{\pi^2 D R_{ti} \gamma \int_0^{D/2} x J_1(\gamma x) \frac{di_{pd}(x)}{dx} dx}{2\gamma J_0(\gamma D/2) - 2\pi D \delta^2 J_1(\gamma D/2)} \\ &* (Y_1(\gamma D/2) J_0(\gamma D/2) - J_1(\gamma D/2) Y_0(\gamma D/2)) \end{aligned} \quad (23)$$

Similarly, connecting the PD to a shunt-shunt TIA consisting of a semi-ideal voltage amplifier - zero output resistance and infinite bandwidth, but limited voltage gain A_0 - and feedback resistor R_f , results in the output voltage expression in (24), where $\zeta \equiv \sqrt{-(R_s + R_f/A_0)(g_A + sC_A)}$.

$$\begin{aligned} v_{out, TIA} &= \frac{2\pi D R_f i_{pd}(D/2) J_1(\gamma D/2)}{2\gamma J_0(\gamma D/2) - 2\pi D \zeta^2 J_1(\gamma D/2)} \\ &+ \frac{\pi^2 D R_f \gamma \int_0^{D/2} x J_1(\gamma x) \frac{di_{pd}(x)}{dx} dx}{2\gamma J_0(\gamma D/2) - 2\pi D \zeta^2 J_1(\gamma D/2)} \\ &* (Y_1(\gamma D/2) J_0(\gamma D/2) - J_1(\gamma D/2) Y_0(\gamma D/2)) \end{aligned} \quad (24)$$

For $x < 1$, one can make the simplifications $J_0(x) \approx 1$ and $J_1(x) \approx x/2$. Furthermore, $Y_1(x)J_0(x) - J_1(x)Y_0(x) \approx -2/\pi x$. With these approximations, the transfer functions (23) and (24) can be rewritten as in (25) and (26).

$$v_{out, TI} \approx \frac{8\pi R_{ti} \int_0^{D/2} r i_{pd}(r) dr}{4 + \pi D^2 (R_s + R_{ti})(g_A + sC_A)} \quad (25)$$

$$v_{out, TIA} \approx \frac{8\pi R_f \int_0^{D/2} r i_{pd}(r) dr}{4 + \pi D^2 (R_s + R_f/A_0)(g_A + sC_A)} \quad (26)$$

This approximated transfer function of the TI resistor has a pole expressed in (27), which is identical as the one of the lumped model in (2), considering $r_d = 1/g_d = 4g_A/\pi D^2$ and $C_d = C_A \pi D^2/4$.

$$BW_{TI} = \frac{4 + \pi D^2 (R_s + R_{ti})g_A}{2\pi^2 D^2 (R_s + R_{ti})C_A} \quad (27)$$

However, when $\gamma D/2 > 1$, which is the case at high frequencies for a large sheet resistance or diode diameter, these approximated transfer functions are no longer valid. In Fig. 14, the transfer function (23) is plotted for a 26 μm Schottky photodiode in 28 nm technology, reverse biased at 3 V and attached to a 100 Ω resistor, both for high and low sheet resistance and for uniform and Gaussian illumination. As can be seen, when the sheet resistance is low (full lines - simulated with actual technology sheet resistances), the lumped circuit model is valid, although there is some discrepancy for the Gaussian profile at frequencies above the bandwidth. However, when the sheet resistance is high (dashed lines - simulated with 100x larger sheet resistances), the distributed RC-circuits prevent the photocurrent generated in the middle of the diode from reaching the diode terminals at high frequencies. As the Gaussian profile inherently generates more current in the center, the degradation at high frequencies is more severe for this profile.

From the previous discussion, it should be clear that the sheet resistances of the Schottky photodiode are of great significance. While PD layout design (M1 plate in parallel with silicide) can reduce the sheet resistance at the top side of the diode, the N-well/P-well/P-substrate sheet resistance is typically the bottleneck. For instance, sheet resistances of the N-well are typically in the range of a few hundreds $\Omega/\square$, while that of silicide can be some orders of magnitude lower, depending on its thickness. Therefore placing a metal plate does not have an impact on the photocurrent bandwidth.

Fig. 14: Circuit simulation of the distributed diode model with transimpedance resistor in parallel. When the diode sheet resistance is high, this model diverges from the classical equivalent circuit.

When designing for a certain receiver bandwidth, it should be verified that the PD size does not lead to degradation of the output voltage response for the technology sheet resistances. A first simple check is whether $\sqrt{2\pi R_{\square} C_A BW D} < 2$. If that is not the case, it is advisable to simulate with the distributed model. If these simulations reveal bandwidth degradation, additional connections in the N-well/P-well/P-substrate should be included in the PD layout at the cost of a reduced fill-factor. Two possible implementations are shown in Fig. 15.

Fig. 15: Possible Schottky PD layouts to increase the bandwidth for large diameters. Red color denotes Schottky region, green color Ohmic region.

Now the noise due to the resistances of the diode will be analyzed. The lumped component circuit of Fig. 2 contains three noise sources: the transimpedance resistor R_{ti} , the series resistance R_s and the diode shot noise current i_n^2 . Assuming

an infinite diode resistance r_d , the spectral density of the output noise power can be found in (28). The series resistance introduces a zero in the transfer functions, which would lead to an infinite integrated noise. However, in reality parasitic capacitances and additional circuit stages introduce extra poles in the circuit, which limit the integrated noise.

$$\begin{aligned} \overline{dv_{n,out}^2} = & \left| \frac{1 + sR_s C_d}{1 + s(R_s + R_{ti})C_d} \right|^2 4kTR_{ti} \\ & + \left| \frac{sR_{ti} C_d}{1 + s(R_s + R_{ti})C_d} \right|^2 4kTR_s \\ & + \left| \frac{R_{ti}}{1 + s(R_s + R_{ti})C_d} \right|^2 2q(I_{dark} + I_{pd}) \end{aligned} \quad (28)$$

The lumped model does not take into account the noise created by the resistive components in the diode itself. When the distributed diode model is adopted, a 4th component contributes to the output noise. The noise spectrum is then given by (29), where the four components stem from the transimpedance resistor, Nwell under STI series resistor, diode shot noise and PD distributed series resistance respectively.

$$\begin{aligned} \overline{dv_{n,out}^2} = & \left| \frac{\pi D R_s (g_A + sC_A) J_1(\gamma D/2) + \gamma J_0(\gamma D/2)}{\gamma J_0(\gamma D/2) - \pi D \delta^2 J_1(\gamma D/2)} \right|^2 4kTR_{ti} \\ & + \left| \frac{\pi D R_{ti} (g_A + sC_A) J_1(\gamma D/2)}{\gamma J_0(\gamma D/2) - \pi D \delta^2 J_1(\gamma D/2)} \right|^2 4kTR_s \\ & + \left| \frac{R_{ti} \gamma}{\gamma J_0(\gamma D/2) - \pi D \delta^2 J_1(\gamma D/2)} \right|^2 \\ & * 4\pi q \int_0^{D/2} |x J_0(\gamma x)|^2 (I_A + i_{pd}(x)) dx \\ & + \left| \frac{R_{ti} (g_A + sC_A)}{\gamma J_0(\gamma D/2) - \pi D \delta^2 J_1(\gamma D/2)} \right|^2 \\ & * 8\pi kT (R_{\square 1} + R_{\square 2}) \int_0^{D/2} |x J_1(\gamma x)|^2 dx \end{aligned} \quad (29)$$

Fig. 16 shows the output noise distribution for a 26 μm Schottky photodiode in 28 nm technology, reverse biased at 3 V with a circular resistive strip of 2 Ω , generating a total photocurrent of 10 μA and connected to a TI resistor of 100 Ω . The noise spectra in dashed lines are calculated for the lumped component model, while the full lines are valid for the distributed diode model. Assuming a non-dominant pole at 3 times the bandwidth, the noise powers are summarized in Table I. Near the bandwidth, the lumped spectra are marginally larger than those of the distributed model, which explains why the integrated noise contributions of the lumped model are slightly larger. However, the distributed resistance noise source, which does not exist in the lumped model, contributes significantly to the total noise power and results in a increase of more than 10% for the input-referred noise current.

	R_{ti}	R_s	I_d	$R_{s,dist}$	$V_{n,out}^2$	$I_{n,in}$
Lumped	6.05 nV ²	349 pV ²	118 pV ²	N/A	6.52 nV ²	0.8 μA
Distributed	5.94 nV ²	278 pV ²	105 pV ²	1.9 nV ²	8.23 nV ²	0.9 μA

TABLE I: Simulated integrated noise powers for lumped and distributed model at the output node for different noise sources

The example above illustrates that while the noise expressions of the lumped model renders rather accurate results,

Fig. 16: Simulated output noise spectrum for 26 μm with 100 Ω R_{ti} and 2 Ω R_s . Dashed lines are calculated for lumped model, full lines are calculated for distributed model.

the noise contribution of the distributed resistances in the diode should be considered in delicate designs. Again, for large diodes or N-well sheet resistances, having more Ohmic connections in the diode area can provide a solution to reduce this noise contribution.

IV. CONCLUSION

Various techniques and insights have been presented for the optimized design of Schottky photodiodes in bulk CMOS for fully integrated high speed optical receivers. The methodology to find an optimum photodiode size can be used for any given profile. The transfer-matrix method revealed that placing a metal plate as close to the active area as possible and wafer thinning the silicon substrate results in the most robust Schottky photodiode implementations. Finally, an advanced distributed circuit model has been introduced for co-design with electrical building blocks. While the lumped model suffices in most cases, the distributed model is absolutely necessary for large photodiode sizes or sheet resistances.

V. ACKNOWLEDGMENTS

The authors would like to thank Prof. J. Bauwelinck from Intec-UGent for support with measurements and the Research Foundation Flanders (FWO) for the research grant (G0D7519N) that supports this work.

REFERENCES

- [1] D. Lee *et al.*, "An 8.5-gb/s fully integrated cmos optoelectronic receiver using slope-detection adaptive equalizer," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2861–2873, Dec 2010.
- [2] A. C. Carusone *et al.*, "Cmos technology scaling considerations for multi-gbps optical receivers with integrated photodetectors," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 8, pp. 1832–1842, Aug 2011.
- [3] S. H. Huang *et al.*, "A 10-gb/s oec with meshed spatially-modulated photo detector in 0.18- μm cmos technology," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 1158–1169, May 2011.
- [4] J. S. Youn *et al.*, "10-gb/s 850-nm cmos oec receiver with a silicon avalanche photodetector," *IEEE Journal of Quantum Electronics*, vol. 48, no. 2, pp. 229–236, Feb 2012.
- [5] S. Huang and W. Chen, "A 20-gb/s optical receiver with integrated photo detector in 40-nm cmos," in *A-SSCC 2013*, Nov 2013, pp. 225–228.
- [6] H. Y. Jung *et al.*, "A high-speed cmos integrated optical receiver with an under-damped tia," in *IPC 2015*, Oct 2015, pp. 347–350.
- [7] C. Sun *et al.*, "A 45 nm cmos-soi monolithic photonics platform with bit-statistics-based resonant microring thermal tuning," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 4, pp. 893–907, April 2016.

- [8] N. Mehta *et al.*, "A 12gb/s, 8.6app input sensitivity, monolithic-integrated fully differential optical receiver in cmos 45nm soi process," in *ESSCIRC 2016*, Sep. 2016, pp. 491–494.
- [9] V. Stojanović *et al.*, "Monolithic silicon-photonics platforms in state-of-the-art cmos soi processes," *Opt. Express*, vol. 26, no. 10, pp. 13 106–13 121, May 2018.
- [10] A. H. Atabaki *et al.*, "High-speed polysilicon cmos photodetector for telecom and datacom," *APL*, vol. 109, no. 11, p. 111106, 2016.
- [11] W. Diels *et al.*, "Modelling, design and characterization of schottky diodes in 28nm bulk cmos for 850/1310/1550nm fully integrated optical receivers," in *ESSDERC 2017*, Sep. 2017, pp. 224–227.
- [12] W. Diels *et al.*, "A 1310/1550 nm fully-integrated optical receiver with schottky photodiode and low-noise transimpedance amplifier in 40 nm bulk cmos," in *ESSCIRC 2018*, Sep. 2018, pp. 242–245.
- [13] W. Diels *et al.*, "Schottky photodiodes in bulk cmos for high-speed 1310/1550 nm optical receivers," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 24, no. 6, pp. 1–8, Nov 2018.
- [14] H. Elabd, T. Villani, and W. Kosonocky, "Palladium-silicide schottky-barrier ir-cdd for swir applications at intermediate temperatures," *IEEE Electron Device Letters*, vol. 3, no. 4, pp. 89–90, April 1982.
- [15] C. K. Chen *et al.*, "Ultraviolet, visible, and infrared response of pti schottky-barrier detectors operated in the front-illuminated mode," *IEEE TED*, vol. 38, no. 5, pp. 1094–1103, May 1991.
- [16] E. H. Rhoderick, "Metal-semiconductor contacts," *IEE Proceedings 1 - Solid-State and Electron Devices*, vol. 129, no. 1, pp. 1–, February 1982.
- [17] B. Smith and E. Rhoderick, "Schottky barriers on p-type silicon," *Solid-State Electronics*, vol. 14, no. 1, pp. 71 – 75, 1971.
- [18] C. Yeh and F. I. Shimabukuro, *The essence of dielectric waveguides*. Springer, 2010.
- [19] M. Casalino, "Internal photoemission theory: Comments and theoretical limitations on the performance of near-infrared silicon schottky photodetectors," *IEEE JQE*, vol. 52, no. 4, pp. 1–10, April 2016.
- [20] C. Katsidis and D. Siapkias, "General transfer-matrix method for optical multilayer systems with coherent, partially coherent, and incoherent interference," *Appl. Opt.*, vol. 41, no. 19, pp. 3978–3987, Jul 2002.
- [21] B. Wong, *Nano CMOS Circuit and Physical Design*. Wiley, 01 2005.
- [22] S. Zollner, "Nmsu ellipsometry data," <https://ellipsometry.nmsu.edu/>.
- [23] M. Polyanskiy, "Refractive index database," <https://refractiveindex.info>.

Wouter Diels (S'14) obtained his Master of Electrical Engineering from the KU Leuven, Belgium in 2014. He is currently working towards a Ph.D. in electrical engineering in the ESAT-MICAS research division. His main interests lie in the monolithic integration of opto-electronic systems.

Michiel Steyaert (F03) received the M.S. degree in electrical and mechanical engineering and Ph.D. degree in electronics from KU Leuven, Leuven, Belgium, in 1983 and 1987, respectively. In 1988, he was a Visiting Assistant Professor with the University of California at Los Angeles, Los Angeles, CA, USA. In 1989, he was appointed by the National Fund of Scientific Research (Belgium) as a Research Associate, in 1992 as a Senior Research Associate and in 1996 as a Research Director with the Laboratory ESAT, KU Leuven. From 1989 to 1996, he was also a part-time Associate Professor. He is currently a Full Professor with KU Leuven. He is also the Dean of the Faculty of Engineering. His current research interests include high-performance and high-frequency analog integrated circuits for telecommunication systems and analog signal processing.

Filip Tavernier (M05) received the masters degree in electrical engineering and the Ph.D. degree in engineering science from KU Leuven, Leuven, Belgium, in 2005 and 2011, respectively. From 2011 to 2014, he was a Senior Fellow with the Microelectronics Group, European Organization for Nuclear Research, Geneva, Switzerland. From 2014 to 2015, he was a Post-Doctoral Researcher with the Department of Electrical Engineering, ESAT-MICAS, KU Leuven, where he has been an Assistant Professor since 2015. His main research interests include circuits for optical communication, data converters, power converters, and chips for radiation environments.