Calculation of the Current Response of the Spatially Modulated Light CMOS Detector

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Abstract—We present an analytical model that allows to calculate the current response of a spatially modulated light CMOS detector (SML-detector) and compare this response with the response of a traditional CMOS photodetector. It is shown that the SML detector already yields a three orders of magnitude faster response time than a traditional CMOS detector in a $0.25\ \mu\text{m}$ CMOS technology. This response time will further decrease as CMOS technology evolves. This analytical expression is compared with a numerical solution of the diffusion equation and with experimental results. Both show an excellent correspondence. Therefore we can conclude that the SML-detector is the solution of choice for cheap, CMOS-compatible receivers in integrated opto-electronic systems.

Index Terms—CMOS analog integrated circuits, optical receivers, photodetectors.

I. INTRODUCTION

ELECTRICAL interconnections between integrated circuits suffer nowadays from lack of aggregate bandwidth, electromagnetic interference (EMI), electromagnetic compatibility (EMC), ESD problems and too high power consumption. Connecting integrated circuits with optical channels may possibly alleviate most of these problems. Optical solutions are investigated and developed for parallel optical interconnects between chips and for several other communication systems, such as Gigabit Ethernet, ... [1]–[5]. However, almost all current high speed optical sources and receivers require a hybrid technology, which lead to increased cost, increased power consumption, and overall system degradation. The spatially modulated light CMOS detector (SML-detector) offers a high-speed optical receiver in conventional CMOS VLSI technology. As such it allows a perfectly matched receiver-amplifier circuit without the cost of hybrid technology. Several demonstrators with excellent performance have already been built, e.g., a matrix with 100 receiver channels on an area of $1\ \text{mm}^2$ where each receiver acquires a $25.1\ \mu\text{W}$ light channel at 200 Mb/s with a bit error rate below 10^{-11} [5]. The development of an analytical model for the calculation of the intrinsic SML-detector response is the object of this paper.

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Therefore, we first describe the concept of the SML detector and the origin of its high-speed response. Next we calculate the minority-carrier profile below the PN-junction as a function of time. This spatially modulated electron profile is shown to dominate the detector response, as long as the detector finger spacing is wider than the n-well implantation depth. In order to prove this statement, the hole response in the n-well is also calculated in a later section and both responses are subsequently combined. Finally, this response is compared with the experimental results and some conclusions are drawn.

II. SML DEVICE STRUCTURE

A cross section of the SML detector is shown in Fig. 1. In this section, we explain how a (spatial) differential design of a CMOS detector leads to drastic speed improvements. The differential approach is implemented as follows. Several equal minimal width n-well stripes are placed at the minimal allowed distance with respect to each other. Alternate ones are covered with floating metal and connected with the deferred output. The others are connected with the immediate output. The substrate consists of lowly doped p-type silicon. As a light pulse is incident on the detector, photogenerated carriers are only present below the latter wells, as is shown in Fig. 1. The minority carriers will diffuse toward the PN-junctions formed between the n-well and the p-substrate. The detector response is mainly determined by the time the carriers arrive at the junction. On a very small time scale, photocurrent is only obtained on the immediate output, from minority carriers generated close to the junction. However, as time evolves the minority carriers will also diffuse laterally, yielding a finally equal response on the immediate and the deferred output, from carriers generated deep in the substrate. These carriers arrive with a substantial delay with respect to the incident light and limit as a consequence the maximum frequency of a conventional CMOS detector. However, if the difference between the immediate and the deferred current is taken, the effect of the carriers generated deep in the substrate is canceled out, yielding a fast detector response. The smaller the n-well stripes can be taken, the faster will be the overall detector response. As a consequence, the maximum detector speed will increase further as technology evolves.

Not only the current response as a function of time determines the performance of a detector. Also the detector capacitance is an extremely important speed-limiting factor. Actually, the best detector sensitivity can be obtained when the detector capacitance matches the input capacitance of the subsequent amplifier. And the lower both capacitances can be taken, the higher

Fig. 1. SML-Detector cross section (top) and mask layout (bottom). The dots symbolize the photogenerated carriers at illumination moment $t = t_0$.

will be the overall system speeds. Fig. 2 shows a photograph of such a SML detector and subsequent differential amplifier and digital output logic integrated using conventional CMOS technology. Currently, all SML-detectors are using the PN-junction between the n-well and the p-substrate, due to the fact that this junction has the lowest capacitance and due to the fact that a higher amount of light is captured related to the fact that this junction is deeper in the substrate. However, it is possible that future SML-detector systems will use the PN-junction between the n+ active implantation and the p-substrate, when the demand for a high maximum detector frequency starts to dominate on the demand for a low detector capacitance and a high current response.

Basically, the SML detector eliminates the current response of photogenerated minority carriers deep in the substrate by making the difference between the immediate and the deferred current. Only minority carriers generated close to the junction are taken as such into account. Other concepts (e.g., the Lateral interdigitated PIN photodetectors on very low-doped substrates or on insulators) have been developed to compensate for the very long absorption length in silicon [2], but these concepts all require nonstandard CMOS processing and are as such more expensive.

III. CARRIER PROFILE BELOW THE JUNCTION

The current response of the CMOS detector described above is mainly determined by the transport of minority carriers (i.e.,

Fig. 2. Photograph of an n-well SML detector and integrated receiver amplifier.

electrons) in the p-type doped layer within the first few diffusion lengths (L_n) below the space charge region of the pn-junction. n_p is the minority carrier concentration in the region below the space charge region, relative to the equilibrium concentration n_{p0} that would be obtained in an infinite bulk layer. The transport of these carriers is described by the equation [6]:

$$\begin{aligned} \frac{\partial n_p}{\partial t} = & D_n \frac{\partial^2 n_p}{\partial x^2} + D_n \frac{\partial^2 n_p}{\partial y^2} + \mu_n \frac{\partial(\xi_x n_p)}{\partial x} \\ & + \mu_n \frac{\partial(\xi_y n_p)}{\partial y} - \frac{n_p}{\tau_n} + g(t, x, y). \end{aligned} \quad (1)$$

With $g(t, x, y)$ the electron generation rate, D_n being the diffusion coefficient of the electrons in the p-doped layer, ξ_x is the electrical field along the x -axis (i.e., the direction perpendicular to the surface), ξ_y is the electrical field along the y -axis (i.e., the direction parallel to the surface perpendicular to detector fingers), μ_n is the mobility of the electrons in the p-doped region, and τ_n being the minority-carrier lifetime. The light intensity in the substrate decays exponentially due to the absorption and the light generated carriers can be expressed as a consequence as

$$g(t, x, y) = g(t, y)e^{-\alpha x}. \quad (2)$$

$g(t, y)$ is then the electron generation rate at the lower border of the space charge region ($x = 0$). This lower border of the space charge region is also the origin of the x -axis of the calculation.

Due to the fact that the electric field (ξ) in the region below the space charge region is negligible, (1) can be approached by

$$\frac{\partial n_p}{\partial t} = D_n \frac{\partial^2 n_p}{\partial x^2} + D_n \frac{\partial^2 n_p}{\partial y^2} - \frac{n_p}{\tau_n} + g(t, y)e^{-\alpha x}. \quad (3)$$

In the simulations discussed below, all parameters are taken as follows: α is about $7 \times 10^2 \text{ cm}^{-1}$ at the GaAs bandgap ($\lambda = 825 \text{ nm}$), the mobility of electrons (μ_n) in p -doped Si is $1500 \text{ cm}^2/\text{V}\cdot\text{s}$, $D_n = 38.8 \text{ cm}^2/\text{s}$, $\tau_n = 2.5 \times 10^{-3} \text{ s}$, and L_n equals 3.11 mm [6]. When a light source at $\lambda = 600 \text{ nm}$ can be used, α increases to $4 \times 10^3 \text{ cm}^{-1}$.

We used diffusion equation (3) to calculate numerically the minority carrier profile below the space charge region of the PN junctions of an SML detector. For a periodicity of the detector fingers of $2 \mu\text{m}$, we will compare the analytical and numerical results. A reverse bias voltage of 3.3 V was applied over the detector and the equilibrium minority carrier profile (compared to bulk material) was used as the starting point of the simulation (i.e., the profile at the moment t_o). This implied that before the simulation started all minority carrier densities were negative numbers. The immediate region was first illuminated during 5 ps after t_o and the total structure was monitored further up to $t_o + 400 \text{ ps}$. Some obtained minority-carrier profiles are shown in Fig. 3. It should be noted that the vertical scale of these figures is 10 times smaller than the horizontal scale. The first profile shows the minority carrier density at the end of the illumination ($t_o + 5 \text{ ps}$). The nonilluminated region still has negative minority-carrier densities, while the illuminated region has positive minority-carrier densities. The borderline between both (marked 0) is still almost vertical but not sharp. It is clear that the first effects of diffusion are already visible. As time evolves this borderline rapidly moves to an almost horizontal line and the difference between the carrier density profile under the immediate and the deferred contacts progressively vanishes. Above $t_o + 70 \text{ ps}$ it is hard to distinguish between both profiles. As a consequence, no big difference between the immediate and the deferred current is further expected. However, both profiles are still positive, even at $t_o + 400 \text{ ps}$. So the photogenerated current at both contacts will persist, even long after the incident light pulse.

We can obtain the immediate (I) and the deferred (D) current from the above calculated carrier densities. The result for the same example is shown in Fig. 4. We observe that both immediate (I) and deferred (D) current have a sharp onset but slow decay. The immediate current (I) has not decreased more than one order of magnitude after 400 ps , but the difference $I - D$ has almost gone down by three orders of magnitude after only 120 ps .

These numerical simulations point out the superior performance of the SML detector, but are difficult to handle to describe the scaling rules of the detector and its performance. Therefore we solve these equations theoretically.

A. Theoretical Solution of the 1-D Problem

The above discussed diffusion equation (3) will be first solved theoretically in one dimension, i.e., the direction perpendicular to the surface. This one-dimensional (1-D) problem is similar to the classical diode switching time problem, where the former

minority-carrier profile is taken as initial condition for solving the diffusion equation [7]. This paragraph uses the same method but adds the photogenerated minority-carrier profile. The diffusion equation in one dimension is

$$\frac{\partial n_p}{\partial t} = D_n \frac{\partial^2 n_p}{\partial x^2} - \frac{n_p}{\tau_n} + g(t)e^{-\alpha x} \quad (4)$$

with $g(t)$ the electron generation rate at the lower border of the space charge region. It can be expressed as a function of the incident light flux $\Phi_o(t)$ as

$$g(t) = \alpha \Phi_o(t) e^{-\alpha l_x} \quad (5)$$

with l_x the distance between the surface and the lower of the space charge region. We took the Laplace transform of the time variable t in (4) and applied the appropriate boundary conditions, assuming an infinite depth of the substrate. This allows to solve the carrier profile analytical. This solution assuming an infinite depth corresponds to the worst-case solution. Equation (4) can also be solved for a finite depth and yields a faster response [8]. From the carrier profile we obtain the current density profile at the lower border of the space charge region of the conventional detector as a function of the frequency, being

$$\frac{J_c(j\omega)}{\Phi_o(j\omega)} = q\alpha L_n e^{-\alpha l_x} \frac{1}{\sqrt{1 + j\omega\tau_n + \alpha L_n}}. \quad (6)$$

A Bode plot of this response is shown as the dashed line in Fig. 5. Equation (6) shows that, from the 3 dB frequency

$$f^* = (4 - \sqrt{7}) \frac{(\alpha L_n + 1)^2}{2\pi\tau_n} \approx 1.3542 \frac{(\alpha L_n + 1)^2}{2\pi\tau_n} \quad (7)$$

the current response of the detector decays with 5 dB/decade. The output power decays as a consequence with 10 dB/decade. f^* is typical 4.1 MHz at $\lambda = 825 \text{ nm}$ and 133 MHz at $\lambda = 600 \text{ nm}$ (Our experimental CMOS reference detector shows a 3 dB frequency of 3 MHz at $\lambda = 825 \text{ nm}$). This implies that a conventional CMOS detector yields signal deformation at higher frequencies. It can be proven that Inter-Symbol Interference (ISI) cannot be removed for binary baseband data transmission at data rates above $2 f^*$ [9]. However, if a certain amount of ISI is tolerated, a higher data rate can be obtained. This will be discussed further in Section VI.

The Bode plot of Fig. 5 shows the current response of the detector. If the voltage response is considered, this current is integrated on a capacitor, i.e., an additional low-pass filter is added. But this effect is limited due to the low capacitance of the SML-detectors.

B. Theoretical Solution of the Two-Dimensional Problem

In this section, we analytically calculate the minority carrier profile below the pn-junction for the SML detector. Equation (1) is now applied to a structure described in two dimensions. A similar approach is followed and the response of the SML detector is compared with the conventional CMOS detector.

When the metal finger pattern with periodicity l is applied, the photo generated carrier profile $g(t, y)$ is a periodic function of l , i.e., the condition $g(t, y) = g(t, y + l)$ applies (see Fig. 1). In order to obtain a realistic estimate of the immediate and deferred

Fig. 3. Calculated excess carrier profile below the pn junction after a 5 ps light pulse incident on a $2 \mu\text{m}$ period SML detector. This profile is recorded for several moments of time (5 ps, 10 ps, 22 ps, 54 ps, 70 ps, and 400 ps).

current, the diffusion equation (3) needs to be solved in two dimensions.

Due to the periodic nature of the structure of (3) in the y direction, we can expand both n_p and $g(t, y)$ as a Fourier se-

Fig. 4. The immediate (I) and deferred (D) current densities extracted from the numerical simulations given in Fig. 3 as a function of time. The difference between both currents is given as $I-D$. The inset shows the theoretical calculation using the inverse Laplace transforms of (6) and (9) for the same structure.

ries with the periodicity of the finger pattern. Equation (3) can only be fulfilled for every value of y if every harmonic component of the Fourier series obeys the equation. So (3) is solved for every harmonic component of the Fourier series of both n_p and $g(t, y)$. First the carrier profile is calculated by taking the Laplace transform of the time variable t . From this carrier profile a current density profile is calculated at the border of the space charge region. This current density profile is integrated over both the junction length of the immediate and the deferred detector yielding J_I and J_D for each component of the Fourier series. From these currents we calculate J_{I-D} and J_{I+D} . The zero order solution equation corresponds to (4), apart from the factor 2, which is due to the coverage with metal of half the surface, and a similar current response is obtained as in (6), and matches, as expected, the sum of the immediate and the deferred signal of the SML CMOS detector

$$J_{I+D}(j\omega) = \frac{J_C(j\omega)}{2}. \quad (8)$$

The zero order solution has an equal current on both the immediate and the deferred detector and does not, as a consequence, contribute to J_{I-D} . The higher order solutions are all uneven in nature and do not contribute to J_{I+D} but do all contribute to J_{I-D} . The sum of all these contributions yields

$$\frac{J_{I-D}(j\omega)}{\Phi_o(j\omega)} = q\alpha L_n e^{-\alpha l_x} \sum_{n=1}^{\infty} \frac{4}{\pi^2 (2n-1)^2} \frac{1}{\sqrt{\left(\frac{(2n-1)2\pi L_n}{l}\right)^2 + 1 + j\omega\tau_n + \alpha L_n}}. \quad (9)$$

Equation (9) has been used to calculate the frequency and phase response of the electron current of three typical SML detectors, i.e., a detector with a grid periodicity of 20 μm , 10 μm and 4 μm .

The results are shown in Fig. 5. The phase response is shown to reach 45° and not 90° at high frequencies. It emerges that a SML CMOS detector implements a build-in equalizer (i.e., no input signal shape deformation) up to the 3 dB frequency, assuming $1/l$ is much larger than α (otherwise, there is no advantage in using an SML detector):

$$f^{**} \approx \sqrt{3} \frac{2\pi}{\tau_n} \left(\left(\frac{L_n}{l} \right)^2 + 1 \right) = 2\pi D_n \sqrt{3} \left(\left(\frac{1}{l} \right)^2 + \left(\frac{1}{L_n} \right)^2 \right). \quad (10)$$

A grid periodicity (l) of 20 μm results in a maximal frequency of about 105 MHz without a pulse deformation. A grid periodicity of 10 μm results in a maximal frequency of about 422 MHz, and a grid periodicity of 5 μm results in a maximal frequency of about 1.6 GHz, which allows the use of nonreturn-to-zero data communication up to 3.2 Gb/s. This implies that a square wave of light coming in results a square detector current waveform. A similar result becomes clear from the experimental $I-D$ current profile discussed in the experimental results section.

The inverse Laplace transforms of (6) and (9) have been used to calculate the electron current impulse response as a function of time for both the Sum ($I+D$) and the differential ($I-D$) response of the detector. The result is shown in the inset of Fig. 4 and compares very well with the full numerical solution of the differential equation (3) shown in the rest of Fig. 4. The major difference is caused by the fact that for the impulse response an infinite Dirac impulse is applied and the numerical simulation uses a pulse of finite height and 5 ps width. The theoretical model gives a superior insight in the performance of a detector, but the numerical simulations are still a valid tool to study the detector under special circumstances, e.g., to study the influence

Fig. 5. Bode diagram of the SML-detector electron current response compared to the conventional CMOS detector (dashed line). Several detector finger periods (L) are given. When both amplitude and phase are flat, no distortion is observed in the detector signal.

of not perpendicular incident light. But this study goes beyond the scope of this paper.

IV. CARRIER PROFILE ABOVE THE JUNCTIONS SPACE CHARGE REGION

In this section, we calculate the minority carrier profile above the junction, which is in this case a hole profile. Holes are as such slower than electrons and at first glance, one would expect a slower response current from the photogenerated holes. However, current state of the art integrated circuit technology implements extremely shallow n^+ diffusion layers and n -wells. This reduces the maximal diffusion length for the holes and results, as a consequence, in a fast hole response current.

Due to the fact that there is no diffusion from the immediate n -doped top layer to the deferred n -doped top layer, the photogenerated holes will not contribute to D current.

In the first approach, we can consider an almost constant hole generation in the area above the PN junction. The equilibrium excess hole concentration is zero at all border surfaces: At the top surface due to surface recombination and at the other surfaces due to the presence of the electrical field. However, the photogenerated hole concentration is only zero at the three junction borders and not at the surface, because the surface recombination process is far slower than the frequencies considered in this paper. The minority carrier current through the top surface is however zero, because there is no top contact above an illuminated part of the well.

In order to calculate the hole response current, we solved the transport equation for the holes being

$$\frac{\partial p_n}{\partial t} = D_p \frac{\partial^2 p_n}{\partial x^2} + D_p \frac{\partial^2 p_n}{\partial y^2} - \frac{p_n}{\tau_p} + g(t). \quad (11)$$

With $g(t)$ being $\Phi_o(t)/l_x(1 - e^{-\alpha l_x})$, L_p is the diffusion length of the holes in the N -type layer (1.5 mm) and τ_p is the hole live time in the N -type layer (2.5 ms) [6]. The carrier distribution function $p(n)$ and the carrier generation function $g(t)$ are rewritten as the product of two Fourier series, one of a square wave in the x -direction (having index n) and the other of a square wave in the y -direction (having index m). Each of these decomposed terms of $g(t)$ drives one of the terms of decomposed of p_n . For each set of indexes n and m , a carrier profile can be calculated and the current profiles can be determined from these carrier profiles.

The total contributed current is the integral of the current through the two sidewalls and the bottom layers. It can be expressed as the sum of the contributions for each of the indices m and n as (12), shown at the bottom of the page. The slowest and also dominant contribution to the current corresponds to the case $n = m = 1$. It can be seen from (12) that the amplitude of the other contributions decreases quadratic with n and m . Therefore, if the hole diffusion is the frequency limit of the detector, the maximum detector frequency is determined by

$$f^{**} \approx \frac{\pi}{2\tau_p} \left(\left(\frac{L_p}{2l_x} \right)^2 + \left(\frac{L_p}{l_y} \right)^2 + 1 \right) \\ = \frac{\pi D_p}{2} \left(\left(\frac{1}{2l_x} \right)^2 + \left(\frac{1}{l_y} \right)^2 + \left(\frac{1}{L_p} \right)^2 \right). \quad (13)$$

The diffusion constant of the holes in the n -doped region (D_p) does depend on the doping level. For the structures under consideration, it can be estimated as $\approx 9 \text{ cm}^2/\text{s}$ [6]. The diffusion length for holes in the n -doped region (L_p) is substantially higher than l_x and l_y , and its influence in (13) can almost be neglected. Comparing (13) with (10) one observes that the pre-factor is about 28 times smaller, but l_y is usually about $l/4$, and if the well depth is about the half of the well width, both equations are equivalent. However, the shallower the well depth, the higher the maximum hole frequency, but the lower its contribution to the overall current response. Fig. 10 shows maximal frequencies of the hole-diffusion current for some commercially available technologies (circles). Not all CMOS fabs reveal their n -well junction depths, so some circles are missing in this figure. In the current state-of-the-art silicon technology, this frequency is somewhat above the corresponding limiting frequency of electron diffusion current.

V. OVERALL DETECTOR CURRENT RESPONSE FUNCTION

The overall detector current response function obviously is the sum of three contributing current responses

$$J_{I-D} = J_{I-D}|_n + J_{I-D}|_{\text{SCR}} + J_{I-D}|_p. \quad (14)$$

The minority-carrier current response of both electrons $J_{I-D}|_n$ and holes $J_{I-D}|_p$ have been discussed in the previous sections. The current density response of the space charge region (SCR) will always be much faster than the readout amplifier response and can be considered just proportional to the light absorption up to frequencies equal to the inverse of the SCR-transit time. Because these frequencies are far beyond the maximum frequencies we consider, the response of the space charge region equals

$$\frac{J_{I-D}|_{\text{SCR}}(j\omega)}{\Phi_o(j\omega)} = q\alpha L_{\text{SCR}} \frac{A_I}{A_T} \quad (15)$$

with L_{SCR} being the length of the SCR, A_I the area below the immediate contact (well or diffusion) and A_T the total detector area. The scaling factor A_I/A_T is needed in order to be able to compare the response current density with the conventional CMOS detector response and the response of both the n -type and the p -type doped layers.

VI. INTER SYMBOL INTERFERENCE

Traditional theories on inter symbol interference are not valid for the SML detector because of the slow frequency response decay after the 3 dB point and because the response is actually the sum of three response functions. Therefore we elaborated the ISI for the conventional and the SML CMOS detector in this section. We consider baseband binary data being transmitted through the optical system where a fixed threshold intensity is used to discriminate between both logic levels. Fig. 6 shows the bode diagram of the combined I -D SML detector response for a detector with a well width being $2 \mu\text{m}$, a well spacing being $3 \mu\text{m}$ and a well depth being $1.5 \mu\text{m}$. The separate electron and hole contributions to the current and the current of the space charge region are also shown. The dominant current is the electron current, which has its 3 dB frequency around 450 MHz. The hole response has its 3 dB frequency around 5 GHz. Finally, also a flat response is obtained, corresponding to carriers generated in the space charge region. In the discussion on inter symbol interference (next section) we will point out which maximum signal frequency that can be obtained starting from these response functions.

With a sampling period t_o , the signal amplitude (S) equals

$$S = \int_0^{t_o} J(t) dt \quad (16)$$

$J(t)$ is the current response function in the time domain. It can be obtained from the inverse Laplace transformations of (9), (12) and (15). The inter symbol interference can be expressed

$$\frac{J(j\omega)}{\Phi_o(j\omega)} = q \frac{L_p^2}{l} \frac{32}{\pi^2} \frac{(1 - e^{-\alpha l_x})}{l_x} \sum_{n=1}^{\infty} \sum_{m=1}^{\infty} \frac{\frac{2l_x}{l_y} \left(\frac{1}{2n-1} \right)^2 + \frac{l_y}{2l_x} \left(\frac{1}{2m-1} \right)^2}{\left(\frac{(2n-1)\pi L_p}{2l_x} \right)^2 + \left(\frac{(2m-1)\pi L_p}{l_y} \right)^2 + 1 + j\omega\tau_p}. \quad (12)$$

Fig. 6. Bode diagram of the combined I - D SML detector response for a detector with a well width being $2 \mu\text{m}$, a well spacing being $3 \mu\text{m}$ and a well depth being $1.5 \mu\text{m}$. The response of the electron current and hole current is also given (dotted).

as a fixed offset (ISI_f) and a statistical variation (ISI_v). Both are strongly dependent on the signal statistics

$$\text{ISI}_f = \sum_{n=1}^{\infty} P_1(n) \int_{nt_o}^{(n+1)t_o} J(t) dt$$

$$\text{ISI}_v = \sqrt{\sum_{n=1}^{\infty} P_1(n) \left(\int_{nt_o}^{(n+1)t_o} J(t) dt \right)^2}. \quad (17)$$

With $P_1(n)$ the probability of having a digital one n b before the actual symbol. The most appropriate threshold level (T_i) equals

$$T_i(t_0) = \text{ISI}_f + \frac{S}{2}. \quad (18)$$

The bit error rate (BER) with this threshold level can then be determined as

$$\text{BER} = \frac{1}{2} \text{erfc} \left(\frac{S}{\sqrt{\text{ISI}_v^2 + N^2}} \right)$$

$$= \frac{1}{2} \text{erfc} \left(\left(\left(\frac{S}{\text{ISI}_v} \right)^{-2} + \left(\frac{S}{N} \right)^{-2} \right)^{\frac{1}{2}} \right) \quad (19)$$

For random bitstreams $P_1(n) = 1/2$. Fig. 7 shows the random-bitstream BER of both the conventional CMOS detector and a SML CMOS detector with a $10 \mu\text{m}$ periodicity, and this for

several signal to noise levels. It is observed that a conventional CMOS detector ($\lambda = 825 \text{ nm}$, $\tau_n = 2.5 \text{ ms}$) cannot obtain a BER below 10^{-11} at 20 Mb/s , with a fixed threshold level and a random bitstream. Appropriate bit sequences ($P_1(n) \neq 1/2$) and error corrections schemes allow the application in the 100 Mb/s range, but the Gb/s range forms a fundamental limit. The $10 \mu\text{m}$ periodicity SML CMOS detector allows 3 Gb/s operation with a BER below 10^{-11} ($\text{S/N} = 10$). This 3 Gb/s is substantially above the in (10) calculated f^{**} (422 MHz). This conclusion can be generalized as “the f^{**} of the SML detector is indicative for the maximum bitrate, but the maximum frequency depends on the randomness of the bitstream, the S/N ratio, and the maximum allowable BER. The maximum bitrate is in any case substantially beyond the frequency f^{**} .”

VII. EXPERIMENTAL RESULTS

Fig. 8 shows the measured I - D SML-detector response for a detector with a $15.6\text{-}\mu\text{m}$ grid periodicity fabricated in a $0.6 \mu\text{m}$ CMOS process. The structure corresponds to what is calculated in Fig. 6. The experimental responsivity is almost flat up to 500 Mb/s . Theoretically, we expect 350 Mb/s for this detector.

Fig. 9 shows the experimentally measured I , D , $I + D$, and $I-D$ waveforms on the above described SML CMOS detector after an incident baseband binary data stream of 300 Mb/s . It is obvious that the $I-D$ signal is the only signal obtained without shape deformation.

Fig. 7. Bit error rate versus data rate for a conventional CMOS detector and an $10\text{ }\mu\text{m}$ periodicity SML detector, for several signal to noise ratios (S/N).

Fig. 8. Measured responsivity as a function of frequency for a $15.6\text{-}\mu\text{m}$ grid periodicity SML detector. A flat $I\text{-}D$ curve is obtained up to 500 Mb/s .

VIII. EVOLUTION OF THE FREQUENCY RESPONSE VERSUS TECHNOLOGY

Fig. 10 plots the maximal SML CMOS detector frequency (n-well implementation) as a function of the minimal gate length of the technology. The central line in both graphs of Fig. 10 indicates a lattice periodicity obtained from the λ scaling rules [10]. However, from a small study of the well width and well spacing parameters used in semiconductor industry [11] (crosses in Fig. 10), it is observed that required lattice period is between 14 and 25 times the minimal gate length of the technology for the n-well implementation. The corresponding obtained frequency is indicated in the two outer lines of Fig. 10. The annotations mark the year this CMOS detector raster could be obtained using ASIC technology according to the SIA roadmap 1999 [12]. The tendency in VLSI technology to replace the n-well diffusion by n-well implantation will definitely lead to a smaller well-to-well spacing and as a consequence higher frequencies.

Fig. 9. Measured signals of a $15.6\text{-}\mu\text{m}$ grid spacing SML detector. The original pulse shape is clearly maintained in the $I\text{-}D$ signal, whereas the slow decay is visible in all other signals.

IX. CONCLUSION

The major advantage of the SML detector is that an undistorted signal is obtained up to the frequency f^{**} . Other systems that try to recover the original binary data from the distorted data cannot use simple threshold logic and require edge detection circuitry or variable threshold logic. This makes them definitely much more sensible to noise, and these systems need as a consequence an elaborated encoding and error correction system. An SML detector system can be operated without or with a simple error detection and correction scheme up the very high frequencies. These frequencies will further rise with technology. The outlook described above indicates that the SML-CMOS has indeed all major capabilities to become the solution of choice for

Fig. 10. Maximal n-well SML CMOS detector frequency f^{**} as a function of the gate length of the used technology for light at 825 nm. The years used in the annotations indicate in which year this technology can be used for the production of ASICs [12]. The gray area indicates the diffraction limit for the used light.

cheap, CMOS compatible receivers in integrated optoelectronic systems.

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