Bias stress in pentacene transistors measured by four probe transistor structures

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Abstract

This paper deals with operational lifetime measurements of organic field-effect transistors. The organic semiconductor under study is pentacene, the gate dielectric is thermal SiO_2, treated with an OTS self-assembled monolayer, and the source and drain electrodes are gold, treated with thiols. The source and drain are defined by photolithography, and the channel length is 100 microns. We apply DC stress conditions on these structures, and monitor the output characteristics of the TFTs during stress as well as during recovery after stress. The transistor structures have been modified to incorporate two voltage-measurement probes in the channel in addition to the source and drain contacts. This results in a 4-probe configuration, that allows to measure the voltage drop in the intrinsic transistor channel separately from the voltage drop over the source and the drain contact regions. When applying a constant (DC) gate-source bias (V_{GS}) corresponding to a field in the gate insulator of 1 MV/cm, we observe two degradation mechanisms: one part of the degradation is permanent, the other part recovers. The permanent degradation could be traced back to the drain side. It typically results in the current halving after 2 hours of stress at a vertical (gate insulator) field of 1 MV/cm. The degradation measured during stress includes both this permanent degradation and the recoverable part. It is significantly larger in magnitude than the permanent degradation, resulting in typically a factor of 10 or more in drain current. The magnitude of the recoverable degradation not only depends on the gate voltage, but also on the drain voltage. It is therefore a consequence of the lateral field at the drain side of the channel. This phenomenological study is a first step towards a comprehensive model for degradation of bias stress in organic field-effect transistors.

1. Introduction

Transistors in organic materials have obtained growing interest since the last decade of the former century as they have potential to realize low-cost electronic circuits. Evaporated pentacene is one of the organic materials that has proven good mobilities (larger than $2 \ cm^2/Vs$) and good on-off ratio's [1, 2]. However, organic materials are much more sensible to degradation. Also the interfaces between the metal and the organic material are often source of degrading contacts [3]. Bias-stress measurements have recently been done to study degradation effects for p-type polymers [Poly(9-9-dioctyl-fluorene-co-bi-thiophene) and regioregular polythiophene [4]] and for pentacene [5]. Regioregular poly-(3-alkylthiophene) has proven that organic transistors can have a substantial shelf life and operation lifetime [6]. Bias-stress experiments on pentacene transistors have been explained by a V_T shift [5], fitted by the empirical equation

$$\Delta V_T \propto |V_G|^{\beta} t^{\gamma} \exp(\frac{E_A}{kT}), \qquad (1)$$

where V_G and t correspond to the gate voltage and the stress time. Fitting Eq. (1) with the experimental data yielded stretching factors $\beta = 0.35$ and $\gamma = 0.22$ for positive gate stress-voltages and $\beta = 0.75$ and $\gamma = 0.06$ for negative gate stress-voltages. In the results mentioned above, Knipp *et al.* [5] do not make a difference between permanent and non-permanent degradation and do not indicate an influence of the drain voltage in the empirical Eq. (1). In this paper, we show the results of bias-stress degradation measurements on pentacene based organic transistors, indicating the above mentioned effects are relevant.
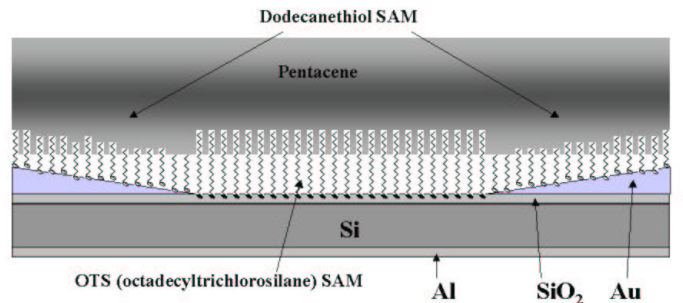

Figure 1. cross-section of the measured device
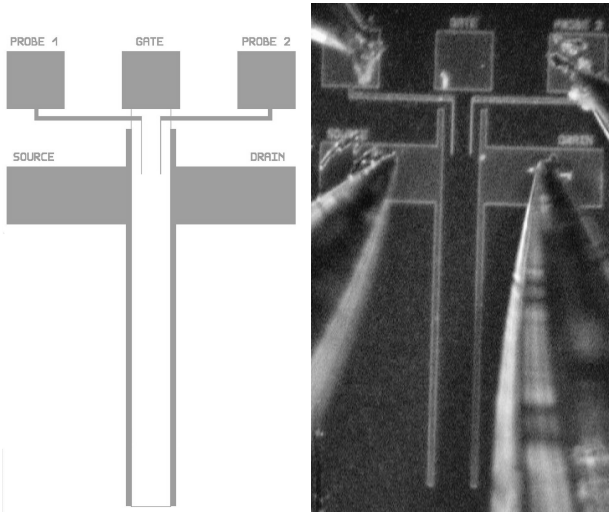
2. Sample preparation

Figure 2. Mask (left) and photograph (right) of the measured device

Fig. 1 sketches the cross-section of the sample used in our experiments. It has been prepared on a silicon substrate with an aluminum back contact. 100 nm thermal SiO_2 has been grown on top of this wafer as a gate dielectric. 20 nm gold source and drain contact layers have been deposited using the mask of Fig. 2. Next the gate dielectric has been covered with an octadecyltrichlorosilane (OTS) self-assembled monolayer and the source and drain electrodes are treated with dodecanethiol. Finally, a 50 nm pentacene layer is deposited under vacuum (flux rate = 0.25 Å/s and substrate temperature 55^oC). The transistor under consideration has a gate length of 100 μm and a gate width of 1000 μm. Probe pads are added at 25 μm and 75 μm in the channel to monitor whether the degradation takes place in the channel or at the contacts (see Fig. 2). After deposition, the sample is introduced in a vacuum probe station for measurements.

3. Source-drain voltage characteristics

Fig. 3 shows the initial source-drain characteristics of the device under investigation. The gate voltage is stepped to -10 V, which corresponds to a vertical (gate insulator) field of 1 MV/cm, which does not seem to introduce much degradation yet. The lower part of this figure shows the same current with respect to the voltage difference between (a) source and source-channel probe (25 μm separated), (b) the voltage difference between the two probes in the channel (50 μm separated) and (c) the voltage difference between drain-channel probe and the drain (25 μm separated). As expected, the largest voltage drop is observed at the drain side when the transistor is in saturation.
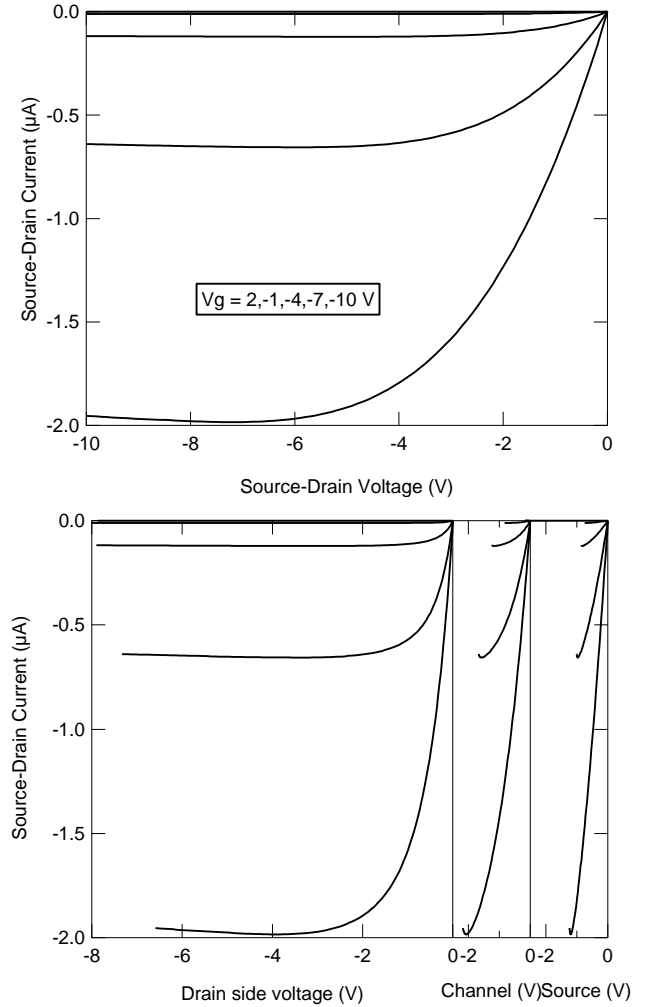

Figure 3. Initial Source-drain current versus source-drain voltage (top) and this current versus the voltage drop over three probed domains (bottom)

These devices subsequently have been stressed using vertical (gate insulator) field beyond 1 MV/cm. After each bias-stress period, a long time has been waited in order to allow a full recovery of the non-permanent degradation. Fig. 4 indicated how the initial curves evolved after a period of bias stress. A short period of bias stress a gate voltage of -15 V (a vertical gate-insulator field of 1.5 MV/cm) showed the evolution from the solid to the dotted curves. Almost no slope change is observed in the characteristics at the source side of the contact and along the channel, and some current drop is observed at the drain side. After a longer stress period, with gate voltages going to -20 V, the dashed transistor characteristics are measured. The saturation current decrease is more pronounced and the slope in the linear regime at the drain side and along the channel degrades substantial. (The slope at the source side does not change). Further bias-stress measurements, at both -15 V and -20 V gate voltage, resulted in the dashed-dotted curves in Fig. 4. No further slope degradation is observed

along the channel and at the source, but the slope in the linear regime at the drain side degrades, combined with a lower saturation current. It is clear that permanent degradation must be located mostly at the drain side. Further experiments are required for the full understanding of this degradation. Two possible causes can be suggested:
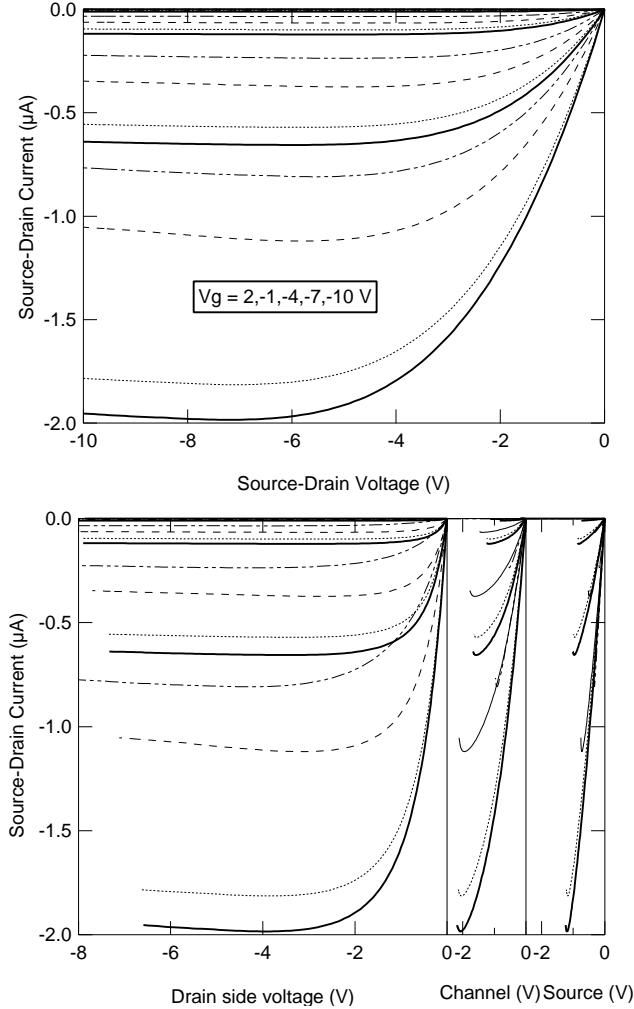

Figure 4. Subsequent Source-drain current versus source-drain voltage (top) and this current versus the voltage drop over three probed domains (bottom)

- A V_T shift, which is, at low gate bias stress, only present at the drain side. At higher bias stress, this V_T shift becomes also observable in the middle of the channel. The consequence of a non-uniform V_T along the channel would lead to a modification in the gradual channel approximation.

- A degradation of the drain contact resistance depending on the applied bias over the drain contact. This degradation is depending on the field at the drain contact.
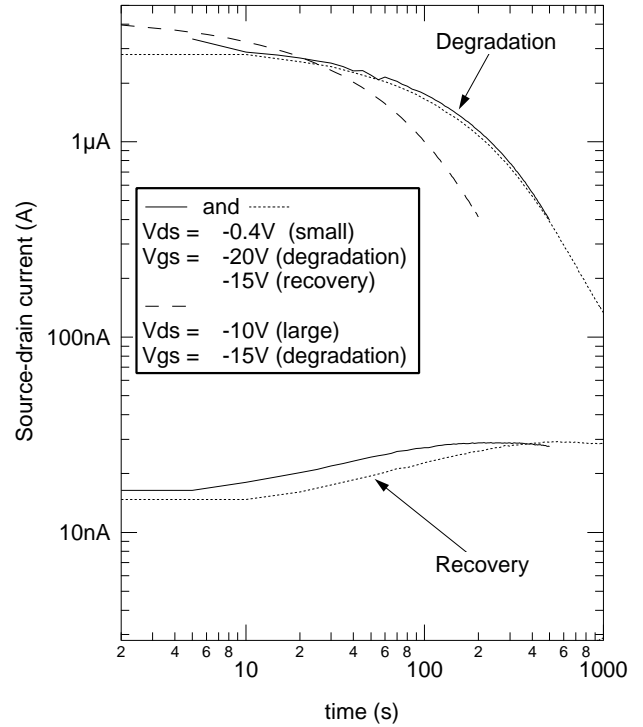
4. Time-dependent measurements

Figure 5. Time-dependent measurement of the current degradation and subsequent recovery. For a small source-drain voltage the full line and the doted line show the degradation at a gate voltage of -20 V followed by a recovery at -15 V. The dashed line shows the degradation present at -15 V for a large source-drain voltage.

Fig. 5 shows the source-drain current as a function of time during the bias-stress measurements. The first set of measurements (solid and the dotted line on Fig. 5) are stress measurements under a high gate voltage and at a small source-drain voltage (-0.4 V). First -20 V is applied at the gate and subsequent -15 V is applied for the same time. It is observed that at -20 V a degradation in the current takes place, which recovers at -15 V gate voltage. The first experiment (2 times 500 seconds) is shown by the full line. The dotted line shows the subsequent experiment (2 times 1000 seconds). Both experiments coincidence, apart from a clear delay in the recovery when the stress has been applied during 1000 seconds. The above mentioned stress experiments took place between the measurements of the dotted and the dashed curves on Fig. 4, i.e. the curves between which the most significant permanent degradation took place. Similar degradation and recovery occurs when space-charge-limited current (SCLC) pentacene devices are measured [7].

We also executed stress measurement at a lower gate voltage (-15 V) and a higher source-drain voltage (dashed curve on Fig. 5). It is observed that the characteristics degrade much faster under a high source-drain voltage, even

though a lower gate voltage was present. This measurement took place between the measurement of the dashed and the dashed-dotted curve on Fig. 4. It appears that after bias-stress with high source-drain voltage, the permanent degradation mostly occurs at the drain site only, in contrast with some permanent degradation along the channel after low source-drain voltage stress.

5.   Conclusion

Bias-stress measurements have been done on pentacene based bottom-contact bottom-gate transistors. Both the permanent and the recoverable degradation have been studied. Both depend on gate voltage and source-drain voltage. At high source-drain voltage, most of the permanent degradation is present at the drain side, whereas a low source-drain voltage and a high gate voltage yields in permanent degradation along the channel and at the drain side. The cause for both the permanent and recoverable degradation is still unclear. Possible causes are high-field degradation of the thiols at the drain side and current or high field related degradation in the octadecyltrichlorosilane (OTS) self-assembled monolayer or in the pentacene layer. Current empirical models (e.g. Eq. (1)) are in any case not elaborate enough to consider drain-field effects, effects of the variation of the V_T along the channel and contact degradation effects. Further experiments will allow to investigate the physical origin of the bias-stress effects in more detail and might suggest further modifications for device improvement.

6.   Acknowledgments

7.   References

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