Low voltage complementary organic inverters

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(Received 2 December 2005; accepted 26 February 2006; published online 20 April 2006)

We have developed a method for integrating *n*- and *p*-type organic thin-film transistors (OTFTs) on the same substrate. An integrated shadow mask was used for the *n*- and *p*-type semiconductor patterning. The integrated shadow mask can be aligned with submicron accuracy relative to the OTFT substrate. This allows for the integration at transistor level of *n*- and *p*-type OTFTs on the same substrate. A complementary inverter was fabricated, showing excellent performance while operating at a supply voltage of 2 V. © *2006 American Institute of Physics*.
[DOI: 10.1063/1.2197604]

For the last few years, organic electronics have become a promising technology for applications requiring low-cost, large area coverage, mechanical flexibility, and low temperature processing. The performance of organic thin-film transistors (OTFTs) based on the organic semiconductor pentacene is now at a level comparable to that of amorphous silicon (*a*-Si:H) TFTs. Several groups have published results on electronic circuits based on OTFTs. Examples of such circuits range from inverters and ring oscillators[1] to shift registers, switching backplanes for flat-panel displays[2] and radio-frequency identification (RF-ID) tag circuitry.[3,4]

Most of the OTFT-based circuits reported to date use *p*-type transistors only. This can be attributed to several reasons. A first reason is the fact that the field-effect mobility μ of *n*-type organic semiconductors is generally lower than that of most *p*-type semiconductors.[5] A major reason for the lack of *n*-type transistors in circuits is the intrinsic instability of the *n*-type semiconductors themselves, and their rapid degradation upon exposure to air and moisture.[5] However, copper hexadecafluorophthalocyanine (F_{16}CuPc) is known to be a relatively stable *n*-type semiconductor, with field-effect mobilities greater than 10^{-2} cm^2/V s.[6] Furthermore, it is generally desired to use low work function materials (Mg, Ca) for the source and drain electrodes in order to create a low electron injection barrier between the source electrode and the *n*-type semiconductor. These metals oxidize almost instantly in ambient air, which limits their practical use. In this respect, F_{16}CuPc has the obvious advantage in that its lowest unoccupied molecular orbital (LUMO) (4.8 eV) is close to the work function of Au (5.0 eV), allowing to use Au as the source and drain electrode material.[7] Finally, it is not straightforward to selectively define *n*-type and *p*-type areas on the same substrate. In this letter, we propose a solution for this last problem.

In spite of these drawbacks of organic *n*-type semiconductors, it stands beyond doubt that the use of both *n*-type and *p*-type transistors in electronic circuits is very advantageous, as is well known in conventional Si complementary metal-oxide-semiconductor (CMOS) technology. Using a complementary technology leads to a lower power dissipation, higher noise margin, better robustness, and easier design of the circuit.

The very first results on complementary OTFT-based circuits have been published by the Bell Labs group, demonstrating the feasibility of fabricating large-scale organic integrated circuits.[8] The *n*- and *p*-type transistor active areas had to be spatially separated by depositing the semiconductors through two shadow masks. With this approach, however, the density of the layout is limited.

Recently, Klauk *et al.* reported on a truly complementary organic technology.[9] In their approach, the *p*-type semiconductor is deposited and patterned using a water-based photoresist and an oxygen plasma etch.[10] Next, the *n*-type material is deposited, which is not patterned afterwards. This approach offers a relatively easy way to create truly complementary organic TFTs and circuits. However, it requires an additional processing step in between the two semiconductor depositions. A third way to complementary organic logic circuits has been proposed, using organic semiconductors with ambipolar transport properties.[11]

We have developed a method that allows to pattern the *n*-type and the *p*-type semiconductor separately on the same substrate. In our approach, the patterning step is done prior to the deposition of the two organic small molecule materials. Devices were processed on a highly doped *n*++ Si wafer, acting as the substrate and the gate electrode. On top of this substrate, 100 nm of SiO_2 was thermally grown, acting as the gate dielectric. The source and drain electrodes consist of a layer of 20 nm Au, patterned by photolithography and lift-off. Subsequently, a layer of the negative photoresist SU-8 25 (purchased from MicroChem Corp.) was spin coated. Processing of the SU-8 25 leads to a patterned layer of about 20 μm thickness, which we call the integrated shadow mask.[12] The highest temperature used in the processing of SU-8 25 is only 95 °C, which makes it thermally compatible with processing technologies on flexible substrates. Subsequent to the SU-8 processing, the substrate was thoroughly cleaned and treated with octadecyl trichlorosilane (OTS) and dodecanethiol self-assembled monolayers. A schematic cross section of the sample is shown in Fig. 1(a).

The sample was mounted on a triangular sample holder. A layer of 30 nm of F_{16}CuPc was evaporated in ultra-high vacuum ($p=10^{-8}$ torr) at a rate of 2 Å/s. During this deposition, the flux is in a 45° angle with respect to the substrate. The SU-8 25 profile thus creates a shadowed region with a width equal to the thickness of the SU-8 25, such that the

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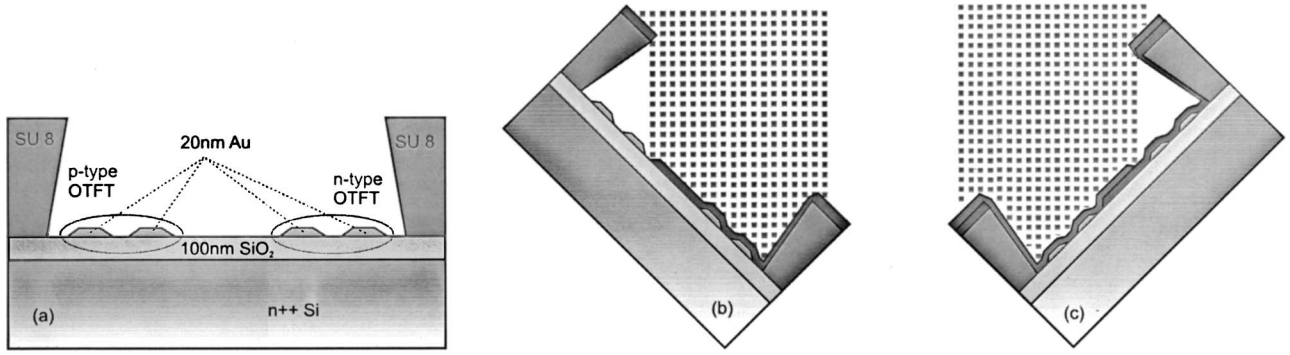

FIG. 1. Schematic cross sections (a) prior to the depositions, (b) during the deposition of *n*-type F_{16}CuPc, and (c) during the deposition of *p*-type pentacene.

substrate is only partially covered with F_{16}CuPc. Figure 1(b) schematically represents the F_{16}CuPc deposition step. The *p*-type transistors are designed in such a way that they fit completely in the regions where the shadow of the SU-8 25 prohibits the growth of F_{16}CuPc.

After the deposition of the *n*-type material, the sample was taken out of the evaporation chamber. In an inert N_2 atmosphere, the substrate was turned 180° on the triangular sample holder. A layer of 30 nm of pentacene was evaporated in ultra-high vacuum ($p=10^{-8}$ torr) at a rate of 0.25 Å/s. During this deposition, the flux is in a −45° angle with respect to the substrate. The SU-8 25 profile thus creates a shadowed region with a width equal to the thickness of the SU-8 25, but different from the one used during the F_{16}CuPc deposition. Again, the substrate is only partially covered with pentacene: applying this method leads to a configuration in which part of each of the semiconductors does not overlap with the other semiconductor. The *n*-type transistors are designed in such a way that they fit completely in the regions where the shadow of the SU-8 25 prohibits the growth of pentacene. Figure 1(c) shows a schematic representation of the pentacene deposition.

As a result of this patterning method, *n*-type and *p*-type transistors have been clearly defined on the same substrate. The devices are not exposed to ambient air or moisture. As can be verified from the optical microscope image in Fig. 2, the *n*- and *p*-type semiconductor patterning principle of this method clearly works.

We have measured *n*-type and *p*-type OTFTs that were fabricated following the described method. After the deposition of F_{16}CuPc and pentacene, the samples were transported through air and measured in a N_2 atmosphere using an Agilent 4156C parameter analyzer. The transistor parameters were extracted from the transfer curve in the saturation regime. Figures 3(a) and 3(b) show typical transfer curves of *n*-type and *p*-type OTFTs.

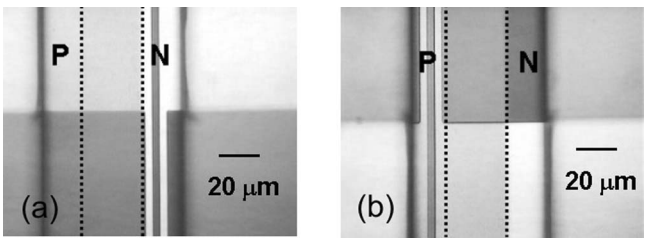

FIG. 2. Microphotographs of the (a) *n*-type and (b) *p*-type OTFTs. The patterned active areas are clearly visible.

In order to prove the usefulness of this organic complementary technology, we have fabricated inverters. A microphotograph of the complementary inverter is shown in Fig. 4. To account for the lower field-effect mobility μ of the *n*-type semiconductor, the W/L of the *n*-type OTFT was designed to

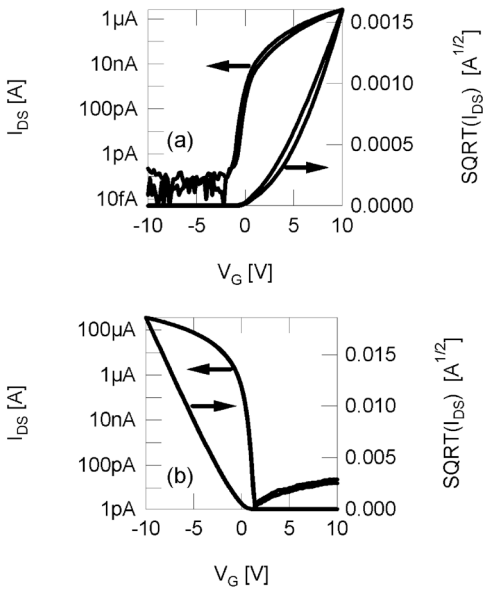

FIG. 3. Measurements of (a) an *n*-type OTFT ($W/L=2500/5$; $V_{DS}=10$ V, and $\mu=5\times10^{-3}$ cm^2/V s, $V_T=2.5$ V); (b) a *p*-type OTFT ($W/L=2500/5$; $V_{DS}=-10$ V, and $\mu=0.5$ cm^2/V s; $V_T=-0.7$ V), and (c) a complementary inverter operating at $V_{DD}=2$ V [inverter transfer curve (solid line) and corresponding gain (dashed line)]. The inset shows the schematic of the complementary inverter.

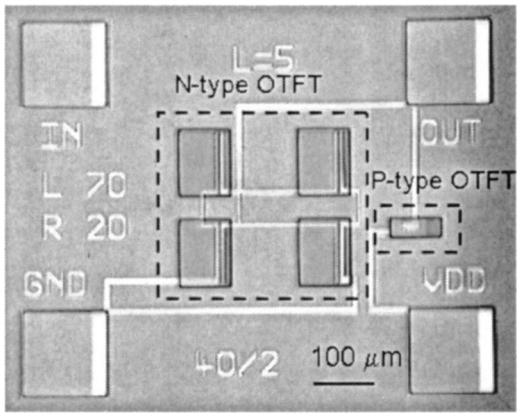

FIG. 4. Microphotograph of the complementary organic inverter.

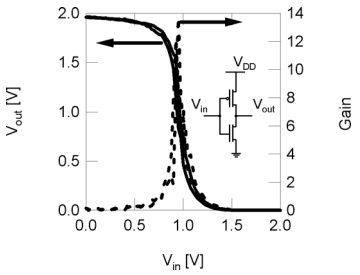

FIG. 5. Measured transfer curve of a complementary inverter operating at Vdd=2 V (solid line) and corresponding gain (dashed line). The inset shows the schematic of the complementary inverter.

be 20 times larger than the W/L of the p-type OTFT. As can be verified in Fig. 5, the complementary inverter shows an almost ideal transfer curve, at a supply voltage V_{DD} of only 2 V. Judging from the extracted threshold voltages of the OTFT measurements on the same substrate, it is assumed that the n-type transistor is operating in the subthreshold region. This explains why the inverter can be successfully operated at a supply voltage that is lower than the expected n-type OTFT threshold voltage. The gain of the inverter was substantially larger than 10, even at these extremely low supply voltages. The output voltage swing is 1.96 V. The hysteresis is negligibly small. The noise margin of this inverter is more than 0.65 V, almost a third of V_{DD}, as calculated by the maximum equal criteria.[12] This clearly demonstrates the enhanced performance and robustness of the complementary inverter with respect to p-type-only inverters.[13] These complementary organic devices are the first to feature excellent gain and noise margin at low operating voltages.[14]

In summary, we have developed an elegant method for fabricating complementary organic TFTs and circuits. We have demonstrated the feasibility and the superiority of this technology by fabricating n- and p-type transistors on the same substrate, using $F_{16}CuPc$ and pentacene, respectively. In addition, low voltage complementary inverters with almost ideal transfer characteristics were realized. The gain was typically between 10 and 15, even at a supply voltage of 2 V. The noise margin is vastly increased with respect to p-type-only inverters. This is the first demonstration of the excellent and stable operation of organic complementary inverters at a supply voltage V_{DD} of 2 V.

This work is partially supported by the EU-funded Integrated Project PolyApply (IST No. 507143) (http://www.polyapply.org).

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