Operation of the Full-Bridge Three-Level DC-DC Converter in Unbalanced Bipolar DC Microgrids

Giel Van den Broeck[1]*, Jef Beerten[1], Mauricio Dalla Vecchia[1], Simon Ravyts[1], Johan Driesen[1]

[1] *KU Leuven, Dept. Electrical Engineering, EnergyVille, Thor Park 8310, 3600 Genk, Belgium*
* E-mail: giel.vandenbroeck@energyville.be

Abstract: As compared to two-wire, unipolar DC microgrids, bipolar DC microgrids apply a positive, neutral and negative conductor to increase the power transfer capability while retaining two voltage levels for supplying low- and high-power devices at an appropriate voltage. However, connecting devices between the positive or negative pole and the neutral conductor, will result in unbalanced currents causing voltage unbalance. Therefore, power electronic converters with voltage balancing capability are essential. Instead of installing dedicated voltage balancing converters, this paper proposes to apply three-level DC-DC converters. These converters are able to interface battery storage with bipolar DC microgrids and balance the pole-to-neutral voltages at the same time. However, high levels of unbalanced currents drive three-level DC-DC converters towards their theoretical unbalanced operating limits. To derive these, a method is presented which decomposes the governing equations in balanced and unbalanced components. Although the method is generally applicable to the three-level converters, the full-bridge three-level converter serves as a comprehensive example. The method enables to derive the unbalanced operating area of three-level DC-DC converters and to appropriately size the filter inductor. Furthermore, a novel modulation strategy is introduced in order to lower the inductor current ripple in unbalanced conditions, supported by experimental results.

1 Introduction

Low-voltage DC microgrids (DCμG) have regained significant interest throughout the past 15 years for enabling a more cost-efficient interconnection of renewable energy sources, energy storage systems, and loads with higher energy efficiency [1, 2]. The key driver for DCμG are power electronics converters which are becoming omnipresent in the power system and frequently contain at least one intermediate DC stage [3]. DCμG harness the increased compatibility between the overlay DCμG and the aforementioned DC devices, to simplify the power conversion steps, to achieve higher power density and higher conversion efficiency [4]. Furthermore, more power can be transferred across the same cable infrastructure [5, 6]. Finally, the presence of controllable converters enables managing the power in-feed and off-take, as opposed to passive diode rectifiers. These advantages drive the adoption of DCμGin a number of applications: datacenters [7], public distribution grids [8], commercial buildings [4], electric vehicle charging stations [9], industrial manufacturing facilities [3].

Two wiring configurations exist for DCμG, namely the unipolar (two-wire) and the bipolar (three-wire) configuration [10–12]. This paper specifically addresses the bipolar configuration, which applies a positive, neutral and negative conductor as depicted in Fig. 1. Bipolar DCμG (b-DCμG) therefore provide two voltage levels: the pole-to-neutral and the pole-to-pole voltage. International initiatives are moving towards ± 350 V and ± 380 V [13]. The availability of the pole-to-pole voltage and the pole-to-neutral voltage enables to connect equipment at an appropriate voltage level. Furthermore, as compared to the unipolar configuration, the power transfer capability significantly increases while the conduction losses diminish up to a factor of four [10]. In the end, also the availability will increase as a bipolar system can potentially continue in single-pole operation when one of both poles would fail [10].

The price to pay to benefit from aforementioned advantages, is the need for power electronic blocks named *voltage balancers* that can equalize the pole-to-neutral voltages [14–18]. The most straightforward solution is a resistive voltage divider, which is not preferred
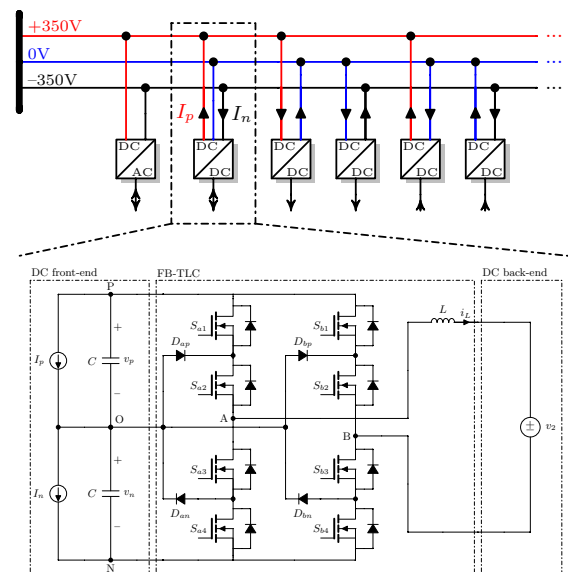

Fig. 1: Full-bridge three-level DC-DC converter in a bipolar DC system with unbalanced loads and generation

as it presents a trade-off between high quiescent losses and tolerable voltage unbalance [19]. Alternatively, a two-level half-bridge can be used for ensuring balanced voltages through bidirectional power transfer between the positive and the negative pole [20].

A different approach to voltage balancing is the introduction of three-level DC-DC converters (TLCs) [9, 21–26]. TLCs are primarily serving as DC-DC converter in applications such as photovoltaic systems and battery storage systems. They were initially proposed to reduce the passive filter size and halve the voltage stress for power semiconductor devices [27–30]. But, as shown in Fig. 1, the availability of a midpoint in between two stacked capacitors

at the converter front-end, enables a three-terminal connection to a b-DCμG.

This paper proposes a comprehensive method to analyze the operation of TLCs in unbalanced conditions. It therefore decomposes the governing equations into balanced and unbalanced components, to separate the voltage balancing function from the main power conversion function. The method is applied to the full-bridge three-level DC-DC converter (FB-TLC) as an example [27, 31], but it is generally applicable to the remaining topologies of the family. The method furthermore enables to establish the unbalanced operating area, defined in section 3, yielding the theoretical limitations for the unbalance conditions that TLCs can accommodate. Although control strategies for balancing pole-to-neutral voltages exist in the literature [32, 33], the typical level of unbalanced current due to non-idealities such as leakage currents, dead-time and differences in capacitances is several orders of magnitude lower than in b-DCμG. At these low levels, the converter will not encounter its theoretical limitations. On the contrary, the high levels of unbalanced currents in b-DCμG drive the FB-TLC towards its theoretical unbalance compensation limits, to be derived.

Before introducing the method and the unbalanced operating area in the third section, this paper covers the steady-state operation of the FB-TLC in unbalanced conditions in section two. In section four, the method is applied to derive the inductor current ripple as a function of the degree of unbalance, which allows to appropriately size the inductance. Furthermore, section four proposes a new modulation strategy for the FB-TLC to minimize the current ripple in unbalanced conditions. Finally, the theoretical results are validated experimentally in section five and the last section concludes this paper.

2 Steady-state operation in unbalanced conditions

2.1 Topology description

The FB-TLC, as depicted in Fig. 1, consists of two neutral-point clamped converter legs, named A and B in the figure. Both legs contain four stacked power semiconductor devices (S_{a1} to S_{a4} and S_{b1} to S_{b4}) with anti-parallel diodes and two clamping diodes (D_{ap}, D_{an}, D_{bp} and D_{bn}). The voltage stress of the power semiconductor devices is by construction equal to the pole-to-neutral voltage (v_p and v_n for the devices on the positive and negative side respectively). Each leg enables to connect the output terminal (labeled A and B respectively) to either the positive (P), neutral (O) or negative (N) terminal of the DC front-end. The complementary switch pairs (for $x = A$ or B) are (S_{x1},S_{x3}) and (S_{x4},S_{x2}). S_{x1} and S_{x4} should never be simultaneously on as the output terminal voltage at A or B would otherwise be undefined. Between terminals A and B the DC back-end (represented by the voltage source v_2) is connected with a series inductor L. v_2 may represent a battery energy storage system, electric vehicle or a photovoltaic system. At the DC front-end, the converter interfaces with a bipolar DC system, represented by the DC current sources I_p and I_n. The task of the FB-TLC is to maintain the output voltages across the front-end capacitors (C) balanced (i.e. $v_p = v_n$) even in the presence of unbalance currents ($I_p \neq I_n$).

2.2 Conversion stages

To start the comprehensive description of the converter operation, consider the following example. The seven possible circuit configurations are depicted in Fig. 2. For example, consider that the FB-TLC is withdrawing power from v_2 and injects it into the bipolar DC system to charge v_p and v_n at the front-end. In the first stage (a), the inductor is charged during a freewheeling interval. Thereafter, in stage (b) and subsequently (d), current will be injected in the positive and negative pole alternately and the cycle repeats. If the DC front-end would withdraw current equally ($I_p = I_n$), an equal amount of charge should be supplied to v_p and v_n to maintain the voltages balanced. However, in unbalance conditions ($I_p \neq I_n$), more charge should be supplied to one pole with respect to the other. That amount

of charge can be altered by changing the duty cycle of configuration (b) and (d) in one switching period. By increasing the duty cycle of (b) and decreasing the duty cycle of (d), more charge will be added to v_p with respect to v_n and vice versa. This example illustrates that the FB-TLC can actively maintain the DC front-end voltages balanced and a similar analysis can be made in case the inductor current i_L is positive as in Fig. 2.

Note that to reduce the inductor current ripple in practice, the freewheeling interval will be distributed between discharging to the positive (b) and negative (d) pole, so the sequence becomes (b)-(a)-(d)-(a). The FB-TLC is also able to apply the entire P-N DC voltage across AB in configurations (f) and (g), in case the back-end voltage v_2 exceeds the pole-to-neutral voltage level. Still, configurations (b) and (d) are applied to inject current asymmetrically into the front-end capacitors. The sequence then becomes (b)-(f)-(d)-(f).

The FB-TLC can also transfer power between the positive and negative pole as it can connect v_p and v_n in both polarities. It is for instance possible to charge the DC back-end from the positive pole in configuration (b) and discharge towards the negative pole by applying configuration (e). This is a distinguishing feature of the FB-TLC that will result in a larger operating area (derived in the next section), as compared to the B-TLC and the HB-TLC. Within that respect, the FB-TLC is considered a topology from which the B-TLC and HB-TLC can be derived.

3 Unbalanced operating area

Although the FB-TLC can maintain a balanced DC front-end, the extent to which is limited as the duty cycle values are bounded. This section will theoretically derive the unbalanced operating area of the FB-TLC, starting from the governing equations. In the subsequent paragraphs, upper-case letters refer to steady-state quantities and lower-case letters refer to dynamic quantities.

Provided the complimentary switch pairs (S_{a1},S_{a3}), (S_{a4},S_{a2}), (S_{b1},S_{b3}), (S_{b4},S_{b2}), four PWM signals need to drive the converter and hence four corresponding duty cycles (d_{a1},d_{a4},d_{b1},d_{b4}) need to be set during each switching period. As the duty cycles d_{x1} and d_{x4} connect the output terminal ($x = A$ or B) to the positive and negative pole respectively, following steady-state equation holds:

$$\underbrace{(D_{a1} - D_{b1})}_{D_p} V_p + \underbrace{(D_{b4} - D_{a4})}_{D_n} V_n - V_2 = 0 \qquad (1)$$

wherein D_{a1} is the steady-state value of the duty cycle driving S_{a1}, D_{a4} is the steady-state value of the duty cycle driving S_{a4}, D_{b1} is the steady-state value of the duty cycle driving S_{b1} and D_{b4} is the steady-state value of the duty cycle driving S_{b4}.

Note that the analysis defines two control signals: $D_p \equiv D_{a1} - D_{b1}$ is the positive duty cycle and $D_n \equiv D_{b4} - D_{a4}$ is the negative duty cycle, related to the positive and the negative pole respectively. In the modulation strategy, pulse-width modulation (PWM) signals d_{a1} and d_{b1} are never on simultaneously, but either one of both is continuously zero throughout the switching period. I.e. $D_p > 0$, $D_{a1} = D_p$ and $D_{b1} = 0$ and $D_p < 0$, $D_{b1} = -D_p$ and $D_{a1} = 0$. Similarly, only one of the PWM signals d_{a4} and d_{b4} is active in each switching period, while the other remains off. This implies that D_p and D_n can vary in the range between $[-1; 1]$.

Considering the steady-state of the front-end currents, (2) and (3) hold for the positive and negative pole respectively. Hereby, the previously defined positive and negative duty cycles are directly substituted.

$$-D_p I_L - I_p = 0 \qquad (2)$$

$$-D_n I_L - I_n = 0 \qquad (3)$$

Equations (1)-(3) determine the steady-state of the FB-TLC. The positive duty cycle D_p (negative duty cycle D_n) determines the part of the inductor current injected in the positive (negative) pole as in (2) and (3) respectively. Furthermore, the duty cycles are interrelated

Fig. 2: Conversion stages of the FB-TLC (red: $i_L < 0$, blue: $i_L > 0$)

and depend on the pole-to-neutral voltage levels V_p and V_n and the DC back-end voltage level V_2.

To facilitate the subsequent analysis of the FB-TLC in unbalanced conditions, the steady-state equations will be expressed in balanced and unbalanced components [18, 34]. The balanced components (voltages, currents and duty cycles) are denoted by the subscript 'b' and the unbalanced components are denoted by the subscript 'u'. The balanced components are one-on-one related to the positive and the negative components used before as in (4)-(5).

$$x_b = \frac{x_p + x_n}{2} \tag{4}$$

$$x_u = \frac{x_p - x_n}{2} \tag{5}$$

Hence, the balanced voltage is simply the average of the pole-to-neutral voltages and the unbalanced voltage is simply half the difference of the pole-to-neutral voltages. A similar reasoning holds for the balanced and the unbalanced current. Introducing these quantities in the steady-state equations (1)-(3), results in (6)-(8).

$$2D_b V_b + 2D_u V_u - V_2 = 0 \tag{6}$$

$$-D_b I_L = I_b \tag{7}$$

$$-D_u I_L = I_u \tag{8}$$

Note that in the transformation, the positive D_p and the negative D_n duty cycle have been substituted by their balanced D_b and unbalanced D_u counterparts. These novel duty cycles, that were introduced, are referred to as the balanced D_b and the unbalanced duty cycle D_u.

The steady-state equations (6)-(8) in balanced and unbalanced components lead to following conclusions in case the pole-to-neutral voltages are balanced (meaning: $V_p = V_n \Leftrightarrow V_u = 0\,\text{V}$):

- The balanced duty cycle is solely determined by the input-output voltage ratio V_2/V_b.
- The balanced duty cycle is independent of the amount of unbalanced current.
- The inductor current is determined by the balanced duty cycle and the balanced current.

From these conclusions it becomes apparent that the decomposition into balanced and unbalanced components enables to study the operation in unbalanced conditions of the converter from its main power conversion function in balanced loading conditions. At zero unbalanced current ($I_u = 0\,\text{A}$), the positive and the negative pole of the DC front-end are equally loaded, meaning $I_p = I_n$. In that case, the unbalanced duty cycle equals zero ($D_u = 0$). Beside, the balanced duty cycle is not determined by the unbalanced current, but by the input-output voltage ratio V_2/V_b. That balanced duty cycle, and the demanded balanced current, in turn determine the inductor current I_L. Whenever $V_u = 0$, (6) and (7) remain unaffected by the unbalanced current I_u. The only quantity that changes in unbalanced operating conditions with non-zero I_u is D_u.

Just like the original duty cycles $D_p \in [-1; 1]$ and $D_n \in [-1; 1]$, D_b and D_u have strict operating limits, which are depicted in Fig. 3a. In the range $|D_b| \leq 0.5$, the figure shows that the unbalanced duty cycle should remain within $[-0.5; 0.5]$, which appears from (9) and (10). These equations reflect the rule that the PWM signals d_{x1} and d_{x4} (x refers in this case to either leg A or leg B of the FB-TLC) should never be simultaneously on, as previously noted in the topology description. For (9), if both d_{a1} and d_{a4} are non-zero in a single switching period, their sum should not exceed 1. As either d_{a1} or d_{b1} is non-zero in a single switching period, $D_p = D_{a1}$ in this particular case, following (1). Similarly In that particular case, $D_n = -D_{a4}$. An analogous reasoning is applied for (10).
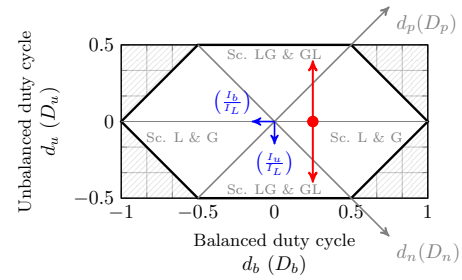
(a) Balanced and unbalanced duty cycle operating area
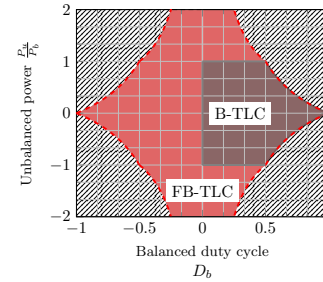
(b) Unbalanced power operating area

Fig. 3: Unbalanced operating area of the B-TLC and FB-TLC. The white regions represent the operating area. The operating area is valid during transients and in steady-state (steady-state quantities are capitalised and within brackets).

$$\underbrace{D_{a1}}_{D_p} \leq 1 - \underbrace{D_{a4}}_{-D_n} \Rightarrow D_p \leq 1 + D_n \Rightarrow D_U \leq \frac{1}{2} \tag{9}$$

$$\underbrace{D_{b1}}_{-D_p} \leq 1 - \underbrace{D_{b4}}_{D_n} \Rightarrow -D_p \leq 1 - D_n \Rightarrow D_U \geq -\frac{1}{2} \tag{10}$$

As the balanced and unbalanced duty cycle are related to the balanced and unbalanced currents by (7) and (8), axes referring to I_b and I_u are added to the figure. Furthermore, Fig. 3a includes two arrows to illustrate how the unbalanced duty cycle changes according to the demanded unbalanced current I_u. In balanced conditions $I_u = 0$ and the corresponding unbalanced duty cycle will equal zero ($D_u = 0$) corresponding to the dot. The location of the dot on the horizontal axis is determined by the balanced duty cycle and hence solely by the ratio V_2/V_b, which does not vary with the unbalanced current. If the unbalanced current differs from zero, D_u will deviate up or downward according to the direction of I_u. If more current is withdrawn from the positive pole, I_p exceeds I_n and I_u is positive, so D_u progresses downward if $I_L > 0$ and vice versa.

Furthermore, Fig. 3a includes four scenario's (abbreviated by 'Sc.'), according to the direction of I_p and I_n:

- Scenario L (unbalanced load): $I_p > 0$ and $I_n > 0$, meaning that power is withdrawn from both poles.
- Scenario G (unbalanced generation): $I_p < 0$ and $I_n < 0$, meaning that power is injected from both poles.
- Scenario LG: $I_p > 0$ and $I_n < 0$, meaning that power is withdrawn from the positive pole and injected in the negative pole. This scenario may occur if there is net generation in the negative pole and net load in the positive pole.
- Scenario GL: $I_p < 0$ and $I_n > 0$, meaning that power is withdrawn from the negative pole and injected in the positive pole.

The FB-TLC operating area also encompasses operating points where $D_b = 0$ and hence $D_p = D_u$ and $D_n = -D_u$. D_u thereby

can vary between -0.5 and 0.5. In that operating condition, the FB-TLC will transfer power from the positive pole to negative pole or vice versa, but not exchange net power over a switching cycle. In that region, the FB-TLC operates as the HB-TLC [35]. The unbalanced duty cycle can be freely selected in the range $[-0.5; 0.5]$ and the inductor current magnitude is entirely determined by the unbalanced current. Selecting $D_u = \pm 0.5$ results in the highest inductor current ripple, but the lowest average inductor current according to (8). Alternatively, lower D_u values result in lower inductor current ripple ΔI_L according to (11).

$$\Delta I_L = \frac{V_b D_u}{L f_s} \quad [D_b = 0] \tag{11}$$

The operating limits can also be studied using power quantities, as depicted in Fig. 3b. The area covered by the FB-TLC is bounded by the dashed red line. Defining the power in the positive pole $P_p = V_b \cdot I_p$ and in the negative pole $P_n = V_b \cdot I_n$ in balanced conditions ($V_u = 0$), enables to relate the *unbalanced power* $P_u = (P_p - P_n)/2$ and *balanced power* $P_b = (P_p + P_n)/2$ to the balanced and unbalanced duty cycle in (12).

$$\frac{P_u}{P_b} = \frac{P_p - P_n}{P_p + P_n} = \frac{I_p - I_n}{I_p + I_n} = \frac{I_u}{I_b} = \frac{D_u}{D_b} \tag{12}$$

For completeness, Fig. 3b also includes the unbalanced operating area of the buck three-level converter (B-TLC), analyzed in [23]. Note that the preceding analysis can also be applied to the B-TLC and the half-bridge three-level converter HB-TLC. The figure clearly indicates that the FB-TLC can cover a larger unbalanced operating area than the B-TLC. A feature worth highlighting is the fact that the FB-TLC can cope with scenario LG and GL, while the B-TLC cannot. This however comes at the expense of additional power semiconductor devices.

4   Modulation and control strategy

After considering the steady-state operation of the FB-TLC, this section will zoom in to a single switching period. As the preceding analysis has shown, in balanced conditions ($I_u = 0$) D_p and D_n will be both equal to the balanced duty cycle D_b. But in unbalanced conditions ($I_u \neq 0$) the duty cycles will deviate with an amount expressed by the unbalanced duty cycle D_u. A non-zero unbalanced duty cycle causes a difference between D_p and D_n and consequently affects the inductor current ripple as this section will show.

4.1   Modulation strategy

To drive the FB-TLC, two modulation schemes are proposed. The first modulation scheme in Fig. 4a applies the positive and negative duty cycle at the start and at half of the switching period respectively. This modulation scheme corresponds to the conventional modulation scheme for three-level converters in balanced conditions and minimizes the inductor current ripple [28]. However, the conditions introduced in the previous section require that PWM signals d_{a1} and d_{a4} do not overlap, as well as d_{b1} and d_{b4}. It is evident from Fig. 4a that these conditions are not respected by modulation 1 in case $D_p > 0.5$ and $D_n < 0$ and in case $D_n > 0.5$ and $D_p < 0$. In that part of the operating area, as indicated by the hatched yellow area in Fig. 6, another modulation scheme is required. Therefore, this paper introduces modulation scheme 2 as shown in Fig. 4b. Modulation scheme 2 applies the positive and negative duty cycle at the start and at the end of the switching period respectively. In that case, the aforementioned conditions are respected.

Additionally, Fig. 6 proposes to apply modulation 2 as well in case $0.5 < D_p < 1$ and $0 < D_n < 0.5$ and in case $0.5 < D_n < 1$ and $0 < D_p < 0.5$. This results in lower inductor current ripple as compared to modulation 1. The normalized inductor current ripple and the real inductor current ripple ΔI_L are defined by (13).
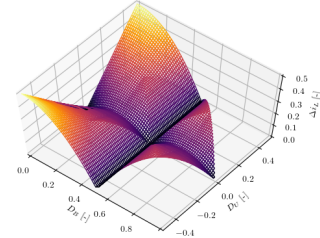
$$\Delta I_L = V_b (L f_s)^{-1} \Delta i_L \tag{13}$$
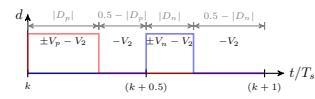
(a) Modulation 1
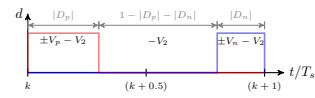
(b) Modulation 2

(c) Normalized inductor current ripple
($\Delta I_L = V_b (L f_s)^{-1} \Delta i_L$)
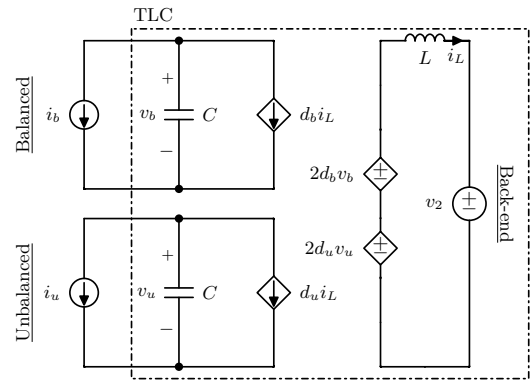
Fig. 4: Modulation scheme

Fig. 5: Equivalent circuit of three-level converters

Where L denotes the inductance, f_s the switching frequency and V_b the balanced voltage.

For modulation scheme 1, the normalized inductor current is given by (14) and for modulation scheme 2, the normalized inductor current is given by (15). These equations show that the normalized inductor current ripple is solely a function of the balanced and the unbalanced duty cycle. The influence of the unbalanced duty cycle is however apparent, showing that operating the FB-TLC in unbalanced conditions will require overdimensioning the filter inductance.

$$\Delta i_L =$$

$$\begin{cases} (|D_b| + |D_u|)(1 - 2|D_b|) & |D_b| \in [0; 0.25] \\ (0.5 - |D_b| + |D_u|)(-2|D_b|) & |D_b| \in [0.25; 0.5] \wedge |D_u| \leq 0.25 \\ (1 - |D_b| - |D_u|)(-2|D_b|) & |D_b| \in [0.25; 0.5] \wedge |D_u| > 0.25 \\ (|D_b| + |D_u| - 0.5)(2 - 2|D_b|) & |D_b| \in [0.5; 0.75] \wedge |D_u| \leq 0.25 \\ (|D_b| - |D_u|)(2 - 2|D_b|) & |D_b| \in [0.5; 0.75] \wedge |D_u| > 0.25 \\ (1 - |D_b| + |D_u|)(1 - 2|D_b|) & |D_b| \in [0.75; 1] \end{cases}$$

$$\tag{14}$$
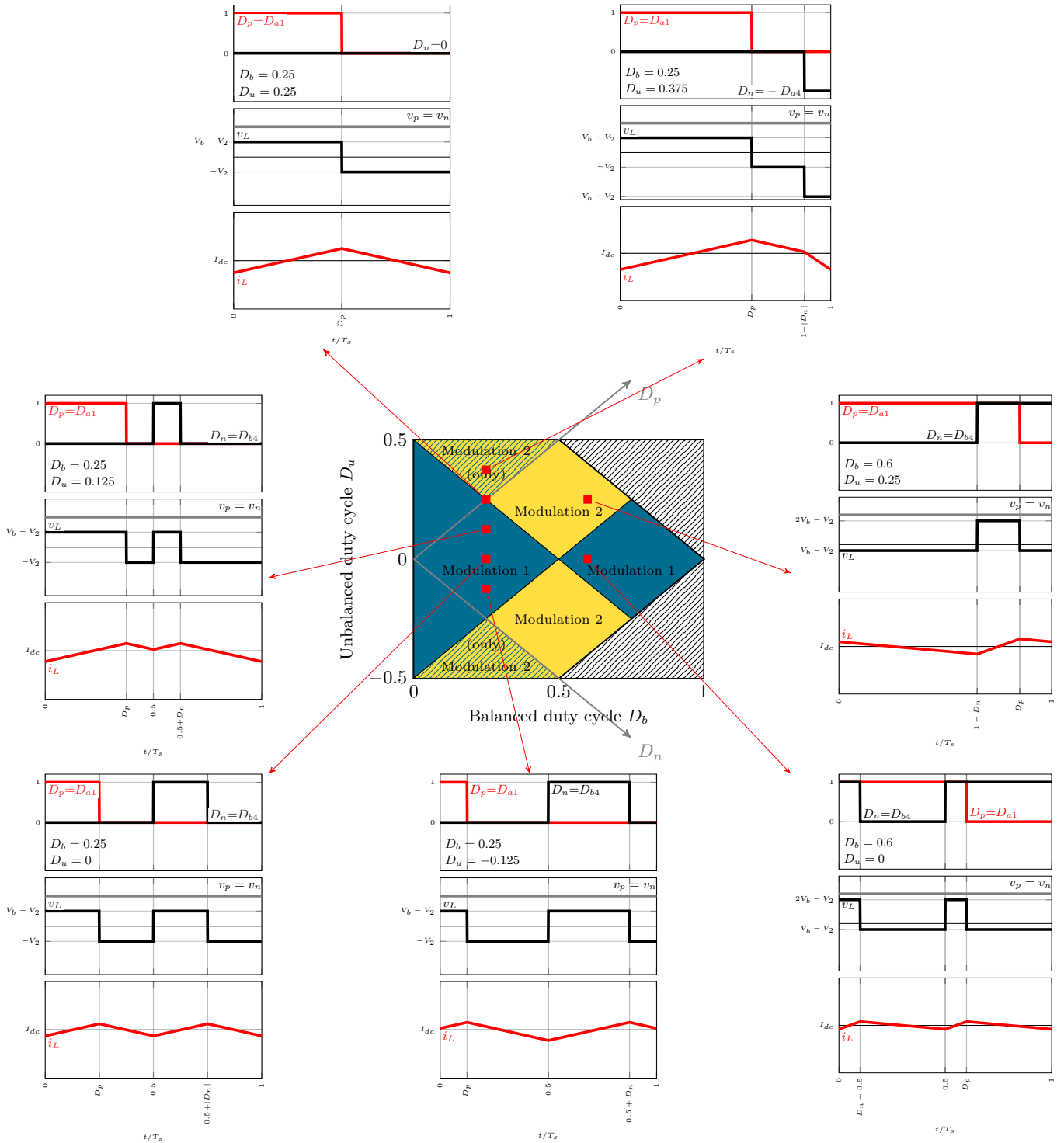
Fig. 6: Waveforms of the FB-TLC for different unbalanced operating points
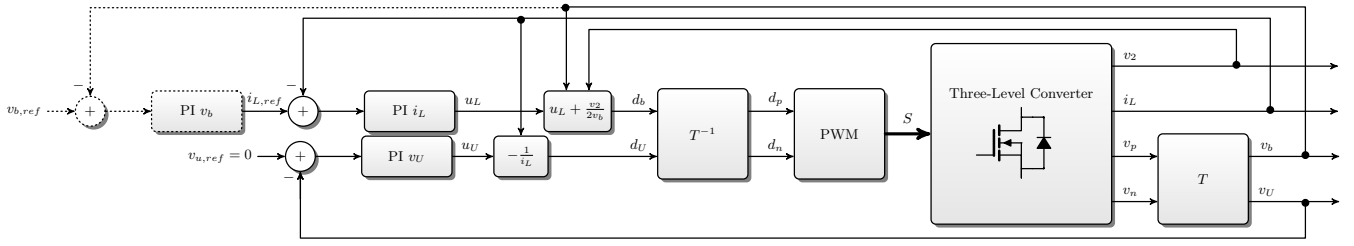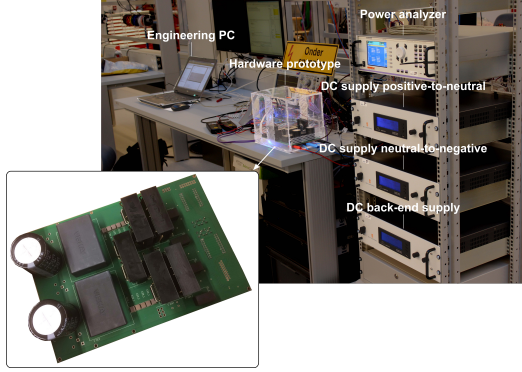
Fig. 7: Control strategy
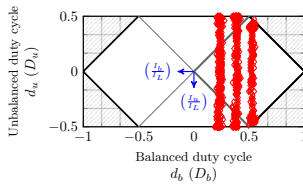

Fig. 8: Hardware prototype in the lab

Fig. 9: Experimental verification of the unbalanced operating area

$$\Delta i_L = \begin{cases} (|D_b| + |D_u|)(1 - 2|D_b|) & |D_b| \leq 0.5 \land |D_b| - |D_u| \leq 0 \\ (1 - 2|D_b|)(2|D_b|) & |D_b| \leq 0.5 \land |D_b| - |D_u| > 0 \\ (2|D_b| - 1)(2 - 2|D_b|) & |D_b| > 0.5 \end{cases}$$

(15)

The normalized inductor current ripple Δi_L is depicted in Fig. 4c for varying balanced and unbalanced duty cycles. As indicated in Fig. 6, this paper advises to change the modulation scheme depending on the operating point in order to minimize the inductor current ripple. The worst-case inductor current ripple occurs at $D_b = 0$ and $D_u = \pm 0.5$, so a higher inductance is required to respect the current ripple requirements. Also note that the inductor current ripple for $D_u = 0$ corresponds to the well-known curves in balanced conditions [28].

The resulting PWM signals, inductor voltage v_L and current i_L waveforms are depicted in Fig. 6 for different operating points in the previously derived operating area. It is advisable to start reading the figure from the lower-left corner, in balanced conditions where the positive and negative duty cycles are equal. When progressing in the clockwise direction, the unbalanced current magnitude I_u and duty cycle D_u increase, while the input-output voltage ratio V_2/V_b and hence D_b remains constant. The remaining waveforms on the right side are for different input-output voltage ratios and modulation schemes.

4.2 Converter dynamics

The three state-variables describing the converter dynamics are the capacitor voltages v_p and v_n and the inductor current i_L, which are governed by (16)-(18). In this section, lower-case symbols are used for time-varying signals, while capitals were used previously to indicate steady-state variables.

$$L\frac{di_L}{dt} = d_p v_p + d_n v_n - v_2$$

(16)

$$C\frac{dv_p}{dt} = -i_p - d_p i_L$$

(17)

$$C\frac{dv_n}{dt} = -i_n - d_n i_L$$

(18)

As in the steady-state analysis, the equations (16)-(18) expressed in positive and negative components are decomposed in balanced and unbalanced components in (19)-(21). These equations can also be represented alternatively by the equivalent circuit in Fig. 5.

$$L\frac{di_L}{dt} = 2d_b v_b + 2d_u v_u - v_2$$

(19)

$$C\frac{dv_b}{dt} = -i_b - d_b i_L$$

(20)

$$C\frac{dv_u}{dt} = -i_u - d_u i_L$$

(21)

4.3 Control strategy

The control strategy is depicted in Fig. 7, which contains additional feedback linearization and feed-forward terms as compared to the control strategy which is generally applied to render controller gains independent of the operating point [23, 32]. T represents the conversion from positive and negative components into balanced and unbalanced components according to (4)-(5). Within the PWM block, the duty cycle values are converted into switching signals as described in the previous section.

The inductor current is controlled through the control signal u_L, which is directly related to the balanced duty cycle d_b, including a feed-forward term. Optionally, as indicated by dashed lines in Fig. 7, the balanced voltage controller can adjust the inductor current reference signal i_{ref} in order to maintain the balanced voltage setpoint (e.g. 350 V). Even in case the balanced voltage controller is disabled, the converter can actively regulate the unbalanced voltage $v_u \to 0$ V by adjusting the unbalanced duty cycle d_u, as shown in the control scheme. A division by i_L is included in the v_u controller in order to make the speed-of-operation independent of the operating point.

4.4 Soft-switching conditions

Under the proposed modulation schemes, the FB-TLC does not operate in zero voltage soft-switching (ZVS) conditions, which implies that all switching transients are hard-switching, having a negative impact on the conversion efficiency. Zero voltage switching occurs if the voltage across a power semiconductor device equals zero, prior to device turn-on. However, considering the conversion stages of the
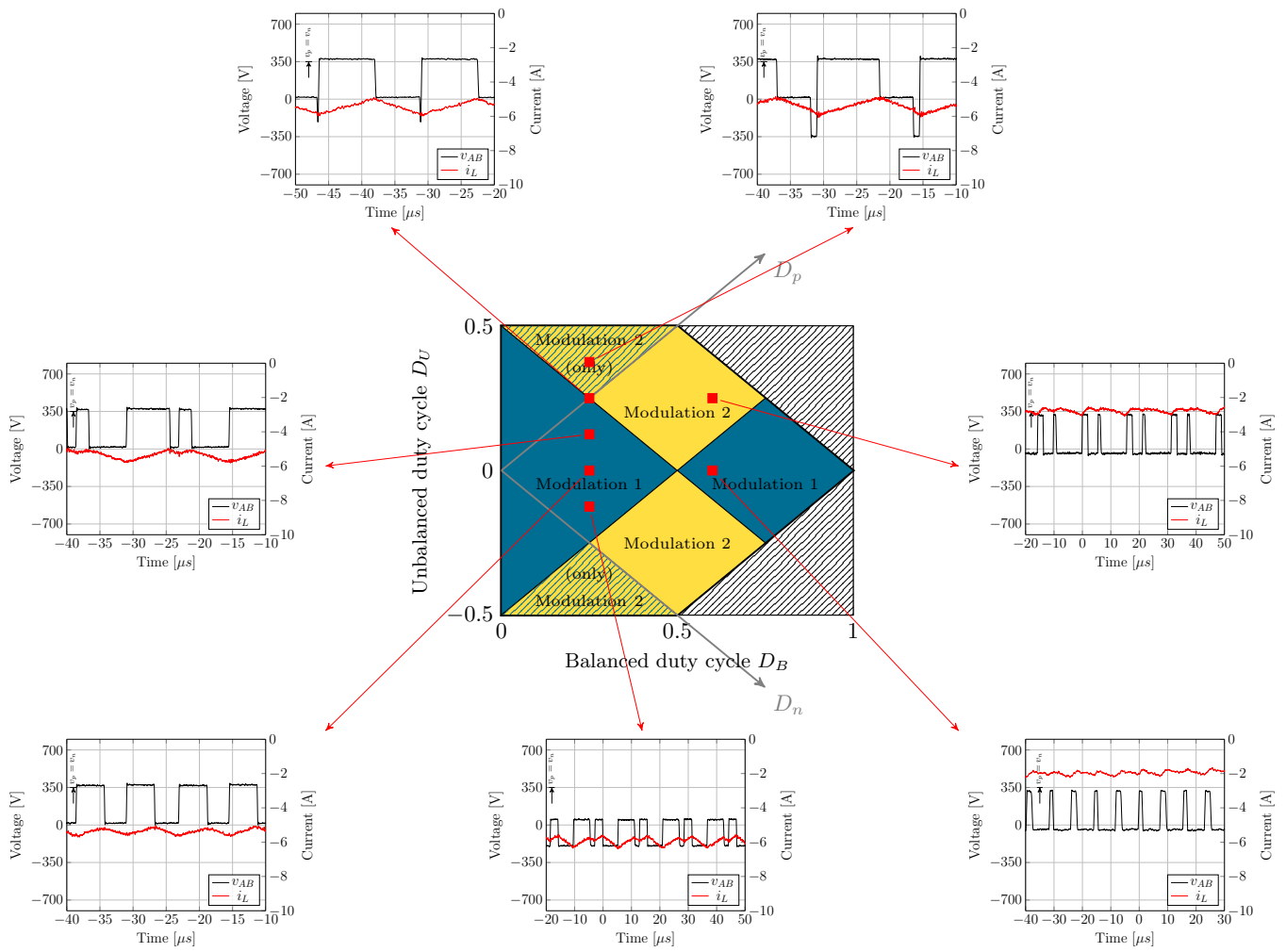
Fig. 10: Experimental waveforms of the FB-TLC for different unbalanced operating points
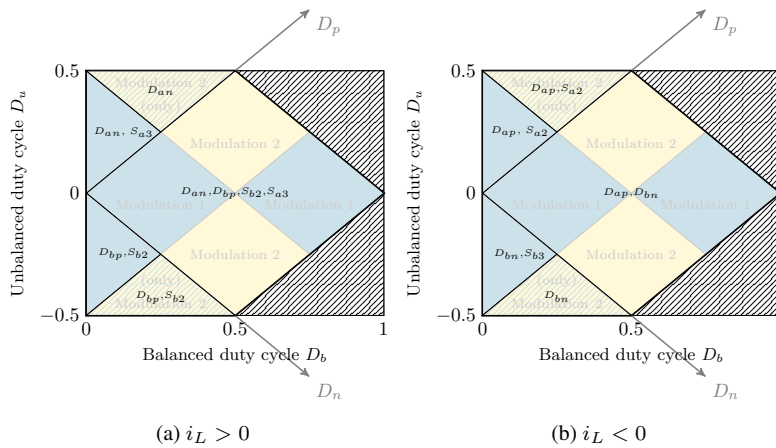

(a) $i_L > 0$

(b) $i_L < 0$

Fig. 11: Power semiconductor devices in zero-current switching conditions

FB-TLC in Fig. 2, reveals that the inductor current does not change sign during a switching period. As a consequence, no anti-parallel diodes accompanying the power semiconductor devices S_{a1}, S_{a2}, S_{a3}, S_{a4}, S_{b1}, S_{b2}, S_{b3} or S_{b4} will conduct prior to device turn-on and zero voltage switching does not occur. This conclusion is valid in all points of the operating area (Fig. 3a). This behavior fundamentally differs from isolated full-bridge three-level DC-DC converters, in which case the magnetizing current enables zero-voltage and zero-current switching conditions [36–38]. Recognize that the voltage across any power semiconductor device in its off-state equals the positive pole-to-neutral voltage v_p or the negative pole-to-neutral voltage v_n. That voltage should hence drop when transitioning from the off-state to the on-state, implying that the devices are non zero-voltage switching.

Zero-current soft-switching (ZCS) occurs if the current through a power semiconductor device equals zero, prior to device turn-off. As shown in Fig. 2, the direction of the inductor current determines which neutral-point clamping diodes and power semiconductor devices conduct in conversion stages (a)-(e). It implies that part of the power semiconductor devices will not conduct in case the inductor current is positive and vice versa. These power semiconductor devices will hence turn-off at zero current and feature ZCS. The part of the unbalanced operating area in which the FB-TLC is operating determines the sequence of the conversion stages and hence which devices feature ZCS. This has been indicated in Fig. 11a for positive inductor current and in Fig. 11b for negative inductor current.

5 Experimental results

The previous sections analyzed the FB-TLC in unbalance conditions and specifically have shown that the FB-TLC can both interface DC devices while providing voltage balancing capability. The aim of this section is to demonstrate the voltage balancing capability of the FB-TLC experimentally.

Therefore, a 2 kW hardware prototype has been developed as depicted in Fig. 8. The converter switching frequency equals $f_s = 65$ kHz, the DC bus capacitors $C = 220\,\mu$F and the inductor $L = 1.4$ mH. The lab set-up in Fig. 8 consists of three programmable bidirectional power supplies. The first two power supplies are connected at the DC front-end (I_p and I_n) and operate in constant current mode, while the third power supply powers the DC back-end in constant voltage mode (V_2).

A TI C2000 F28379D digital signal processor obtains measurements of the positive and negative pole-to-neutral voltages, the inductor current, and outputs the four complimentary PWM signals to the FB-TLC gate drivers. The controller depicted in Fig. 7 has been programmed in the digital signal processor. The control objective is to maintain the balanced voltage constant at $V_b = 350$ V and maintain the pole-to-neutral voltages balanced ($V_u = 0$ V).

The DC back-end power supply is set at $V_2 = 200$ V. The current i_L that is supplied by the back-end power supply, is controlled by the converter prototype in order to maintain the balanced voltage setpoint $V_b = 350$ V. Furthermore, the converter prototype is controlled by the unbalanced duty cycle to maintain the pole-to-neutral voltages balanced at $V_p = V_n = 350$ V, even in unbalance conditions caused by the front-end power supplies.

5.1 Operating area

To explore the boundaries of the theoretical operating area, the FB-TLC is operated in different unbalance conditions in Fig. 9. Three red lines are depicted in the figure, representing the operating conditions at three different back-end voltage levels $V_2 = 200$ V, 300 V and 400 V respectively from left to right. The unbalance conditions and D_u were varied up to the converter limits.

5.2 Waveforms

The hardware prototype is operated in different unbalance conditions at $V_2 = 175$ V, $V_b = 350$ V and $P_2 = -1$ kW. The waveforms for

increasing $D_u = 0$ (balanced), $D_u = 0.125$, 0.25 and 0.375 are depicted in Fig. 10. The figure depicts the output voltage v_{AB}, measured between the terminals of the three-level half-bridges, and the inductor current waveform i_L. These waveforms correspond to the theoretical outcomes in Fig. 6. Corresponding to Fig. 4c, the current ripple increases in unbalanced conditions.

5.3 Converter dynamics

Fig. 12a depicts the FBTLC dynamics for a step-change applied in the balanced current I_b, demonstrating that the FBTLC is able to maintain the positive pole-to-neutral voltage v_p and the negative pole-to-neutral voltage v_n equal and controlled at the setpoint value 350 V after a load increase. This corresponds to a load increase of 50 % or 1 kW.

Fig. 12b depicts the FBTLC dynamics for a step-change increase in the unbalanced current I_u, in case the DC back-end voltage equals 175 V, corresponding to a balanced duty cycle value of $D_b = 0.25$. This step-change corresponds to moving from the operating point at zero unbalance ($D_u = 0$) in Fig. 10 to the operating point at $D_u = 0.375$. The results show that the unbalanced current has a minor influence on the inductor current, which remains constant throughout the transient. Furthermore, the results show that the FBTLC is able to smoothly change from modulation scheme 1 to 2 during the transient.

Fig. 12c depicts the FBTLC dynamics for a step-change increase in the unbalanced current I_u, in case the DC back-end voltage equals 420 V, corresponding to a balanced duty cycle value of $D_b = 0.60$. This step-change corresponds to moving from the operating point at zero unbalance ($D_u = 0$) in Fig. 10 to the operating point at $D_u = 0.25$. The results again show that the unbalanced current has a minor influence on the inductor current, which remains constant throughout the transient. Again, the results show that the FBTLC is able to smoothly change from modulation scheme 1 to 2 during the transient.

6 Conclusion

In order to balance the pole-to-neutral voltages in bipolar DC microgrids, this paper introduced a comprehensive analysis method to compare the voltage balancing capability of three-level DC-DC converters and applied it in-depth to the full-bridge three-level DC-DC converter. The method decomposed the governing equations into balanced and unbalanced components and is generally applicable to the three-level DC-DC converter family. The method resulted in the definition of the unbalanced operating area, which has been derived for the full-bridge and buck three-level DC-DC converter topologies, featuring a bipolar DC front-end. It showed that the unbalanced operating area of the full-bridge three-level DC-DC converter extends beyond the one of the buck three-level DC-DC converter. While the buck three-level DC-DC converter can operate in scenario L and G with unbalanced load and generation respectively, the unbalanced operating area of the full-bridge three-level DC-DC converter additionally covers scenario LG with load in one pole and generation in the other pole. Furthermore, expressing the inductor current ripple as a function of the balanced and the unbalanced duty cycle, revealed that the filter inductance should be over-dimensioned to meet the current ripple constraints in unbalanced conditions. To compensate for the increase, the paper proposed to smoothly shift to a different modulation scheme depending on the degree of unbalance. This shift is even indispensable in part of the unbalanced operating area, as the conventional three-level DC-DC converter modulation scheme would violate fundamental operation rules. To validate the theoretical contributions, an experimental prototype has been developed and tested in unbalanced conditions.
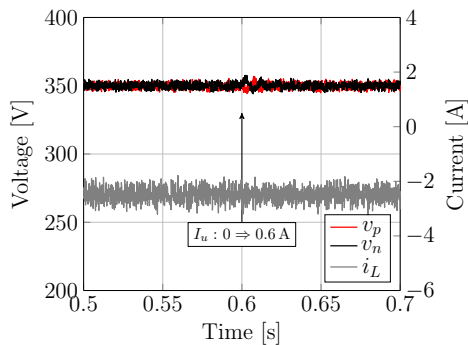
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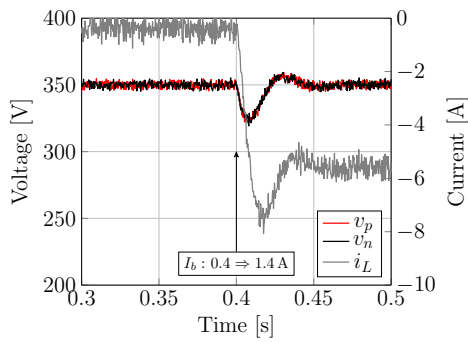
(a) $D_b = 0.25$ $I_b : 0.4 \to 1.4$A
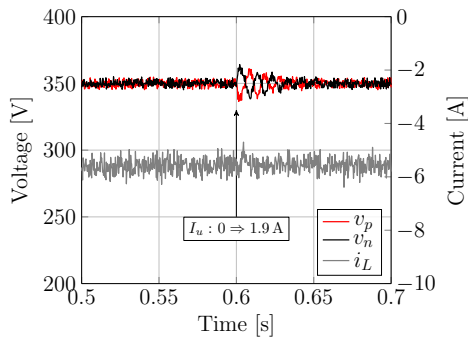
(b) $D_b = 0.25$ $I_u : 0 \to 1.9$A

(c) $D_b = 0.60$ $I_u : 0 \to 0.6$A

Fig. 12: Dynamic response of the FB-TLC converter

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