Performance Limitation Analysis of Highly-Digital Time-Based Closed-Loop Sensor-to-Digital Converter Architectures

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***Abstract*—This paper presents the theoretical and comparative analysis of two major time-based architectures for sensor interfaces. Both use a voltage-controlled oscillator (VCO) to achieve a highly-digital scalable implementation. The first architecture is based on a phase-locked loop, while the second one is count-based. Both systems are closed loop to efficiently mitigate the VCO nonlinearity. They show inherent first-order quantization noise shaping thanks to the use of an oscillator and phase detection. The two systems having a different working principle leads to different VCO requirements in terms of gain linearity (V-to-f or V-to-T linearity). Formulas are derived to predict the maximum SQNR for both architectures. Equations for the achievable maximum SNR taking into account the VCO phase noise are also derived, since this is the limit to the SNR in practical implementations. State-variable-based simulation results are presented, confirming the theoretical analysis and emphasizing the different design trade-offs and practical considerations.**

I. Introduction

Distributed integrated sensors are increasingly important in the emerging era of the Internet of Things (IoT), as they are the gate between the physical world and the electronics. Lately, time-based sensor interfaces representing the signal by time information have become more and more popular: their highly-digital implementation allows a small area, a high energy efficiency and a good scalability exploiting all the benefits of advanced CMOS technology nodes [1].

Time-based implementations have been proposed both in open and closed loop. In [2] and [3], the oscillators are used as a frequency modulator, resulting in a $\Sigma\Delta$ modulator with no need for DACs due to the open-loop architecture. Two different analyses of such open-loop VCO-based ADC are presented in [4] and [5], emphasizing its similarity with pulse frequency modulators and $\Sigma\Delta$ modulators, respectively. However, in such open-loop systems the poor VCO linearity limits the overall system SNDR.

In [6]–[10] the VCO nonlinearity is tackled by placing the VCO in a closed loop after the passive/active analog integrator. Here, multiphase VCO outputs or VCOs in combination with counters are used as quantizers following power-hungry loop filters. PLL-based sensor-to-digital interface architectures have been described in [11]–[13]. In [14], a theoretical study shows that the PLL-based sensor interface also resembles a first-order $\Sigma\Delta$ modulator due to the oscillator frequency-to-phase conversion. In these closed-loop systems the performance is rather limited by the VCO phase noise than the VCO nonlinearity.

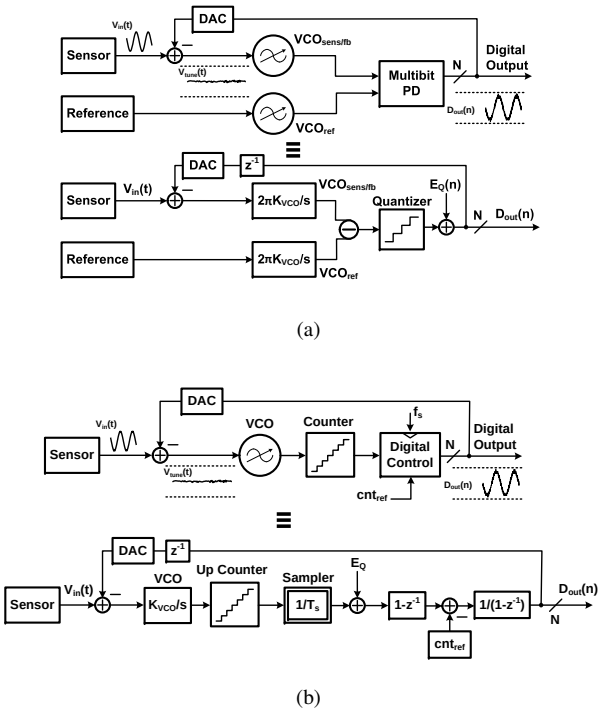

Fig. 1: Block diagram and corresponding simulation model of (a) the PLL-based and (b) the count-based closed-loop sensor interface architectures.

This paper presents the theoretical analysis and simulation results of two major closed-loop highly-digital-oriented architectures used for sensor interfaces: the first is based on the phase-locked loop, as shown in Fig. 1(a), while the second is based on counting, as shown in Fig. 1(b). A closed loop is preferred for sensor interface applications due to the low-bandwidth and high-linearity requirements.

The paper is organized as follows. Section II highlights the working principles of the two architectures, leading to different VCO requirements. Section III derives the maximum SQNR and discusses the performance including phase noise. Simulation results employing a state-variable Matlab model confirm the theoretical analysis. Section IV draws conclusions.

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II. System-level sensor interface architectures

A. PLL-based Architecture

Fig. 1(a) shows the basic building blocks of a PLL-based system used as a sensor interface [12]–[14]. The architecture consists of two matched VCOs and a multi-bit phase detector (PD). A time-domain chopping technique introduced in [13] is employed to cancel both the DC offset from the VCOs' mismatch and the VCOs' $1/f$ noise. Note that the multi-bit PD can be substituted by a single-bit PD and a digital PI filter to create an N-bit output, resulting in an almost equivalent system [14], avoiding the multi-bit PD nonlinearity.

1) Working principle: The conversion is based on the locking of the two identical VCOs: one controlled by a reference voltage (VCO_{ref}) and one by a voltage determined by both the sensor and the feedback signal ($\text{VCO}_{\text{sens/fb}}$).

2) Locking condition: In every sampling period T_{ref}, the oscillator $\text{VCO}_{\text{sens/fb}}$ can lag or lead with respect to VCO_{ref}. The PD outputs an N-bit code (D_{out}), which is the result of time-domain quantization, and thus is the digitization of the sensor signal ($V_{in}(t)$). The locking condition implies that the $\text{VCO}_{\text{sens/fb}}$ period is on average equal to the VCO_{ref} period:

$$\overline{T}_{sens/fb} = T_{ref}. \tag{1}$$

Hence, to ensure correct operation, the edge detection principle requires a voltage-to-period (V-to-T) linear VCO, modeled as follows:

$$T_{VCO} = T_0 - K_{T_1} \cdot V_{tune} \tag{2}$$

where T_0 is the free-running period, K_{T_1} is the linear V-to-T gain factor, and V_{tune} is the VCO input voltage.

B. Count-based Architecture

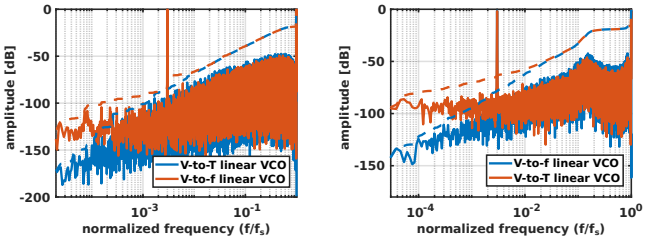
Fig. 1(b) shows the basic building blocks of the count-based sensor-to-digital converter. The system consists of a VCO, a counter[1], a sampling clock, digital blocks and a feedback circuit. Differently from [9], the integrator has been removed, leading to first-order noise shaping. Compared to [3], the loop has been closed, requiring further digital processing to ensure the correct signal and noise transfer functions.

1) Working principle: The basic operation is to count the number of VCO edges that occur within each sampling clock period (T_s). The count values are then scaled according to a reference count value (cnt_{ref}), which can be recomputed to tackle PVT variations. Finally, a digital circuit computes the digital output (D_{out}), which is fed back to the input.

2) Equilibrium condition: Due to the closed loop, the count values ($cnt_{sens/fb}$) are on average equal to cnt_{ref}, meaning that the oscillator frequency ($f_{sens/fb}$) is kept on average proportional to the sampling frequency (f_s):

$$\frac{\overline{f}_{sens/fb}}{f_s} = \overline{cnt}_{sens/fb} = cnt_{ref}. \tag{3}$$

[1]The counter may be replaced by a multi-phase VCO output allowing higher sampling frequencies. However, the phase noise performance of the two systems differs: the phase noise of the single-phase VCO employed in the count-based architecture is degraded by $10log_2N$ when used as N-phase VCO [5]. In this brief, in order to make a fair comparison between the two architectures, the same VCO is used: the count-based architecture is thus preferred. This leads to different sampling frequencies for the two systems.



(a) (b)

Fig. 2: Simulated output spectrum as a function of the input bandwidth with a V-to-f linear and a V-to-T linear VCO for (a) the PLL-based architecture (T_0 = 100ns, K_{T_1} = 4ns/V, N = 4, $f_s = 1/T_0$ = 10MHz) and (b) the count-based architecture (f_0 = 10MHz, K_{f_1} = 8MHz/V, N = 4, f_s = 1MHz). The dashed lines indicate the simulated integrated noise corresponding to the spectra with the same color.

V-to-T linear VCO	**Equivalent V-to-f linear VCO**
T_0	$f_0' = 1/T_0 = f_0$
K_{T_1}	$K'_{f_1} = -K_{T_1}/{T_0}^2 = -K_{T_1} \cdot {f_0}^2$
V-to-f linear VCO	**Equivalent V-to-T linear VCO**
f_0	$T_0' = 1/f_0 = T_0$
K_{f_1}	$K'_{T_1} = -K_{f_1}/{f_0}^2 = -K_{f_1} \cdot {T_0}^2$

TABLE I: V-to-T and V-to-f linear VCO parameters.

Since the count value is directly proportional to the frequency, a voltage-to-frequency (V-to-f) linear VCO is required to ensure proper functionality. The VCO frequency is thus expressed as:

$$f_{VCO} = f_0 + K_{f_1} \cdot V_{tune} \tag{4}$$

where f_0 is the free-running frequency, K_{f_1} is the linear V-to-f gain factor, and V_{tune} is the VCO input voltage. The ratio f_0/f_s determines the reference count value cnt_{ref} (3).

C. Analysis and comparison

To verify the validity of these linearity conclusions and to analyze the performance of the two time-based architectures, a time-domain state-variable-based Matlab model has been developed for the two systems. At first, the phase noise is not included to focus on the impact of the VCO linearity relationship (V-to-T or V-to-f) on the maximum SQNR. The impact of phase noise will be discussed in Section III-B.

Fig. 2(a) and Fig. 2(b) plot the simulated output spectra of the PLL-based and the count-based architecture, respectively, employing a V-to-T (2) and a V-to-f (4) linear VCOs. The equations to compute the equivalent V-to-f linear VCO starting from a V-to-T linear VCO, and vice versa, are shown in Table I. By employing a V-to-f linear VCO in the PLL-based architecture (Fig. 2(a)) and a V-to-T linear VCO in a count-based architecture (Fig. 2(b)), a noise floor appears in the spectrum limiting the ideal behavior. This confirms that in a PLL-based architecture a V-to-T linear VCO is needed to reach the maximum SQNR, while a count-based architecture requires a V-to-f linear VCO. To increase the legibility of the spectrum, the integrated noise is also plotted (dashed) [15].

In practical implementations, although the effect of the VCO nonlinearity is mitigated by the closed-loop architecture,

	PLL-based architecture	Count-based architecture
$S_{in,p-p}$	$2AK'_{f_1}$	$\frac{2\pi 2AK_{f_1}}{f_s}$
Δ	$\frac{2AK'_{f_1}}{2^N}$	2π

TABLE II: Peak-to-peak signal power $S_{in,p-p}$ and quantization step Δ definitions for both architectures where A is the maximum signal amplitude, N the quantizer resolution, K'_{f_1} the equivalent VCO V-to-f gain (as the PLL-based architecture requires a V-to-T linear VCO), K_{f_1} the VCO frequency gain for the count-based architecture, and f_s the sampling frequency.

the use of a VCO with the non-optimal linearity relationship results in a performance loss[2], as shown in Fig. 2.

III. Performance Evaluation

In the bottom parts of Fig. 1(a) and Fig. 1(b), the simulation block diagrams of both architectures are depicted. In the first subsection the ideal behavior of the two systems will be derived, showing the analogy with a first-order noise-shaped $\Sigma\Delta$ modulator operating in the phase/frequency domain instead of the voltage domain. In the second subsection the effect of the oscillator phase noise will be analyzed.

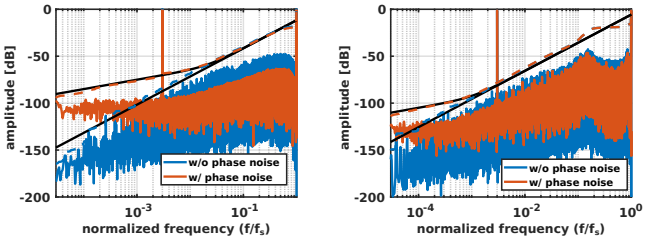
A. SQNR and Oversampling

The input signal power P_S is equal to $(S_{in,p-p}/(2\sqrt{2}))^2$ where $S_{in,p-p}$ is the peak-to-peak amplitude of the input signal. Assuming the quantization error has equal probability over the range of the quantization step Δ, the quantization noise power can be written as $P_Q = \frac{\Delta^2}{12}\frac{\pi^2}{3}\left(\frac{1}{\text{OSR}}\right)^3$. By definition, the SQNR is calculated as P_S/P_Q.

Table II reports the values of $S_{in,p-p}$ and Δ for both architectures. By replacing these values in the aforementioned formulas for P_S and P_Q, it is possible to derive the maximum SQNR equal to $6.02N' - 3.41 + 30\log(\text{OSR})$. This is the well-known result for a $\Sigma\Delta$ modulator with first-order noise shaping. For the PLL-based architecture, N' corresponds to N, the number of bits in the PD, while for the count-based architecture, N' is defined as $N_q = \log_2(2K_{f_1}A/f_s)$, and it also represents the quantizer resolution.

In the PLL-based architecture, the maximum SQNR depends only on N, the number of bits in the multi-bit quantizer. The system performance is not influenced by the VCO properties, except for the free-running frequency, which determines the system sampling rate. A change in the VCO gain, K'_{f_1}, does not have any impact on the ideal behavior. Moreover, the VCO gain and the number of bits in the feedback DAC can be chosen independently. On the other hand, in the count-based topology, the maximum SQNR strongly depends on the VCO gain, K_{f_1}, since the quantizer resolution, N_q, is function of K_{f_1}. Moreover, the number of bits in the feedback DAC, N, needs to be proportional to N_q in order to ensure correct behavior. In both architectures, the quantizer resolution and the number of bits in the feedback DAC can be decoupled using a digital $\Sigma\Delta$ [9].

[2]The performance loss caused by the use of a VCO with the non-optimal linearity relationship depends on the number of bits in the quantizer. Increasing the number of bits allows to reduce the excited VCO frequency/period span, which appears more linear, hence decreasing the error.



(a) (b)

Fig. 3: Simulated power spectrum without and with phase noise (-100 dBc/Hz@100 kHz offset) for (a) the PLL-based architecture (T_0 = 100ns, K_{T_1} = 40ns/V, N = 4, f_s = $1/T_0$ = 10MHz) and (b) the count-based architecture (f_0 = 10MHz, K_{f_1} = 8MHz/V, N = 4, f_s = 1MHz). The dashed lines indicate the simulated integrated noise of the spectra with the same color. The black lines indicate the calculated theoretical results.

B. SNR and Phase Noise

The practically achievable SNR is limited by other sources of noise, such as the oscillator phase noise, beyond the quantization noise. The phase noise $L(\Delta f_x)$, expressed in dBc/Hz, represents the noise power density at an offset frequency Δf_x from the carrier frequency f_0. The $1/f^2$ phase noise power of the oscillator is:

$$P_{pn,f,PLL} = \pi L(\Delta f_x)\Delta f_x^2 \cdot \frac{f_0}{\text{OSR}} \tag{5}$$

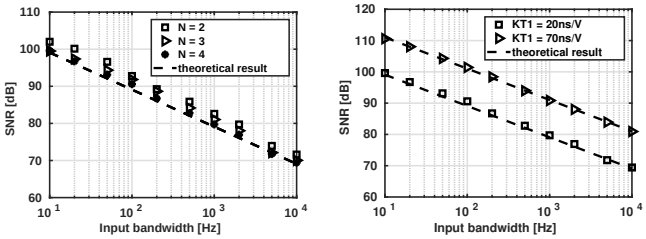
$$P_{pn,\phi,COUNT} = 16\pi L(\Delta f_x)\Delta f_x^2 \cdot \frac{1}{f_s}\frac{1}{\text{OSR}} \tag{6}$$

for the PLL-based [14] and the count-based architectures [5], respectively. The free-running frequency of the VCOs, f_0, in the PLL-based architecture, and the clock frequency, f_s, in the count-based architecture represent the sampling rate of the two systems, respectively. The total noise power is then determined by the sum of the quantization noise power P_Q, derivable from Table II, and the phase noise power P_{pn} (5) and (6). [3]

Fig. 3(a) and Fig. 3(b) plot the simulated power spectrum with and without phase noise for the PLL-based and the count-based architectures, respectively. Two regions can be distinguished: the first one where the phase noise dominates the quantization noise (flat spectrum), and the second one where the quantization noise dominates the phase noise (20dB/decade spectrum). In order to increase the legibility of the spectra and to compare the simulation results with the theoretical analysis, the integrated noises of the spectra are plotted in Fig. 3 as dashed line with the corresponding spectrum color. In both architectures, the simulated integrated noise is in agreement with the theoretical analysis, shown as black line, for both settings (with and without phase noise). In the simulations, the rms cycle-to-cycle jitter of the oscillator is calculated from the $1/f^2$ phase noise using ${\sigma_c}^2 = L(\Delta f_x)\Delta f_x^2/{f_0}^3$ [16].

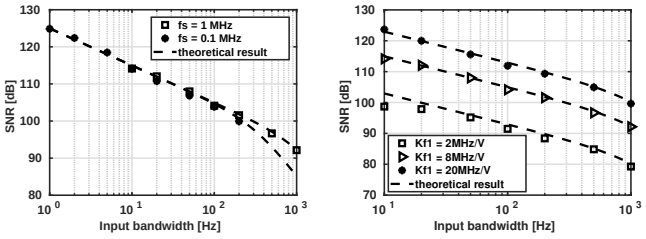
Considering the PLL-based architecture, when the phase noise dominates, which is the typical operating region, P_{pn}

[3]Note that the formulas that express the signal power P_S and the quantization noise power P_Q, both derivable from Table II, and the formulas for the phase noise power P_{pn} (5) and (6) have the unit [Hz^2] for the PLL-based architecture, while being dimensionless for the count-based architecture.



(a) (b)

Fig. 4: SNR as a function of the input bandwidth for the PLL-based architecture with -100 dBc/Hz@100 kHz offset phase noise for (a) different numbers of bits in the multi-bit PD (T_0 = 100ns, K_{T_1} = 20ns/V) and (b) different VCO period gains (T_0 = 100ns, N = 4).



(a) (b)

Fig. 5: SNR as a function of the input bandwidth for the count-based architecture with -100 dBc/Hz@100 kHz offset phase noise for (a) different sampling clock frequencies (f_0 = 10MHz, K_{f_1} = 8MHz/V) and (b) for different VCO frequency gains (f_0 = 10MHz).

is (much) larger than P_Q, the SNR can be equated as follows:

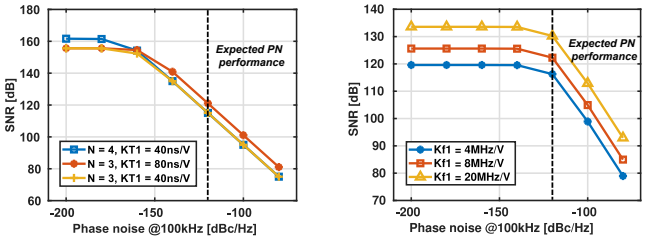
$$\begin{aligned}\text{SNR}_{pn,PLL} &= 20\log(K'_{f_1}A/\sqrt{2}) \\ &\quad - 10\log(\pi L(\Delta f_x)\Delta f_x^2 f_0) + 10\log(\text{OSR}) \\ &= 10\log\left(\frac{(K'_{f_1}A)^2}{\pi 4L(\Delta f_x)\Delta f_x^2 f_{in}}\right), \quad (7)\end{aligned}$$

meaning that in the phase-noise-limited region of operation, increasing the number of bits N does not increase the SNR by 6.02dB for each bit. Fig. 4(a) indeed shows that simulation results for all number of bits N are within few dB of the theoretical value (7). However, in contrast to the ideal case, the oscillator gain K_{T_1} starts to influence the SNR performance when the phase noise is included, as shown in Fig. 4(b), confirming (7). The $+10\log(\text{OSR})$ behavior instead of $+30\log(\text{OSR})$ is also visible in the plots.

For the count-based topology, the VCO frequency gain K_{f_1} plays an important role in determining the SNR in both the ideal and the non-ideal case. The phase-noise-limited SNR (when $P_{pn} \gg P_Q$) can be expressed as:

$$\begin{aligned}\text{SNR}_{pn,COUNT} &= 20\log(K_{f_1}A/\sqrt{2}) \\ &\quad - 10\log(4/\pi L(\Delta f_x)\Delta f_x^2 f_s) + 10\log(\text{OSR}) \\ &= 10\log\left(\frac{\pi(K_{f_1}A)^2}{16L(\Delta f_x)\Delta f_x^2 f_{in}}\right). \quad (8)\end{aligned}$$

As shown in Fig. 5(a), the SNR does not depend anymore on the sampling frequency f_s for a given bandwidth. Increasing the VCO gain improves the SNR, as shown in Fig. 5(b).



(a) (b)

Fig. 6: SNR as a function of the oscillator phase noise for (a) the PLL-based architecture (T_0 = 100ns) and (b) the count-based architecture (f_0 = 10MHz, f_s = 1MHz, N = 4) for an input bandwidth of 100 Hz for different system parameter values (e.g. N, K_{T_1}, K_{f_1}).

However, the VCO gain strictly influences the achievable phase noise. A high-gain VCO usually shows a larger phase noise than a low-gain VCO at the same free-running frequency.

It is interesting to notice that in the PLL-based architecture operating in the phase-noise-limited region, the SNR (7) has lost its dependency on the number of bits N (see Fig. 4(a)) compared to the maximum SQNR. Similarly, in the count-based architecture operating in the phase-noise-limited region, the SNR (8) has lost its dependency on the sampling frequency f_s (see Fig. 5(a)) compared to the maximum SQNR. Moreover, both architectures show the same dependency on the VCO gain (see also Fig. 4(b) and Fig. 5(b)).

Fig. 6 summarizes the SNR results for both systems. In Fig. 6(a), for the PLL-based topology, it is visible how the number of bits, N, in the multi-bit PD influences the SNR when the phase noise is negligible (left part), while the VCO gain K_{T_1} has no influence. On the other hand, when the phase noise starts dominating (right part), the VCO gain influences the SNR, while N has no effect on the performance. Fig. 6(b) plots the SNR as a function of the phase noise for the count-based architecture, showing the effect of the oscillator gain K_{f_1} in both regions (quantization noise dominant (left part) and phase noise dominant (right part)). The vertical dashed line limits the design space region, since practical $1/f^2$ phase noise values for $\Delta f = 100$kHz and $f_0 = 10$MHz are typically around or above -120dBc/Hz.

In practical implementations, at very low bandwidths, which is the case for sensor interface applications, the system performance is limited by the oscillator phase noise[4]. It is, therefore, interesting to compare the performance of these two time-based architectures under this condition. Fig. 7 plots the SNR as a function of the input bandwidth for both the PLL-based and the count-based architectures. In order to have a fair comparison, the same VCO and phase noise are used in the simulations. As stated in Section II, the PLL-based architecture requires a V-to-T linear VCO, while the count-based architecture requires a V-to-f linear VCO. The proper VCO has been used in the simulations (Table I). The count-based architecture shows a 4dB better SNR in the

[4]In this brief only the $1/f^2$ oscillator noise is considered. The $1/f$ noise can be canceled by means of chopping [13] in a PLL-based architecture. In a count-based architecture, the VCO flicker noise can be tackled by means of negative feedback [17].

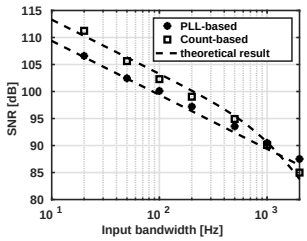
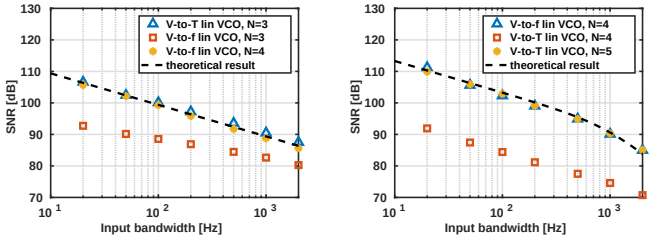


Fig. 7: SNR as a function of the input bandwidth for the PLL-based and the count-based architectures employing the same VCO (f_0 = 10MHz, K_{f_1} = 6.6MHz/V). The VCO phase noise is equal to -100 dBc/Hz@100 kHz offset.



(a) (b)

Fig. 8: SNR as a function of the input badwidth for (a) the PLL-based and (b) the count-based architectures employing the same VCO (f_0 = 10MHz, K_{f_1} = 6.6MHz/V) but with a different linearity relationship (see Table I).

phase-noise-limited region (low bandwidth), confirming the theoretical result that is obtained by comparing (7) and (8) when the same VCO, the same phase noise and the same signal amplitude are used:

$$\text{SNR}_{pn,COUNT} - \text{SNR}_{pn,PLL} = 10\log(\pi^2/4) \approx 4\text{dB}. \quad (9)$$

The transition from the phase-noise-limited to the quantization-noise-limited SNR is visible at high frequencies.

Fig. 8 shows that the use of the non-optimal VCO (see Sec. II) can further degrade the system performance (orange squares). However, by increasing the quantizer resolution, the excited range in the VCO characteristic reduces, hence appearing more linear, thus reducing the error due to using the non-optimal linearity relationship, which becomes negligible compared to phase noise. The optimization of N depends on the system architecture, and the VCO gain and phase noise.

C. Design guidelines

The two time-based closed-loop architectures studied here theoretically have similar performance. However, the PLL-based system requires matched VCOs [14]; time-domain chopping relaxes this requirement [13]. The count-based topology intrinsically avoids this demand by employing only one VCO, which also leads to a lower power consumption. However, thanks to its pseudo-differential architecture, the PLL-based system is more robust against common-mode disturbances. This architecture is therefore suitable for differential sensors read-out, while the count-based system is a good candidate for interfacing single-ended sensors.

IV. Conclusion

This paper has analyzed and compared the achievable performance of two major time-based closed-loop sensor interface architectures: PLL-based and count-based. The theoretical derivations have been validated by means of state-variable-based Matlab simulations. The different working principles of the two systems have been highlighted, leading to different VCO requirements in terms of gain linearity (V-to-T or V-to-f). Formulas describing the maximum SQNR have been derived for both architectures. Since the oscillator phase noise is the limitation in practice, equations to predict the practically achievable SNR have been derived and validated by simulations. Different trade-offs and considerations for the design of both architectures have been presented.

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