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ARTICLE

# Doping-Free Complementary Logic Gates Enabled by Two-Dimensional Polarity-Controllable Transistors

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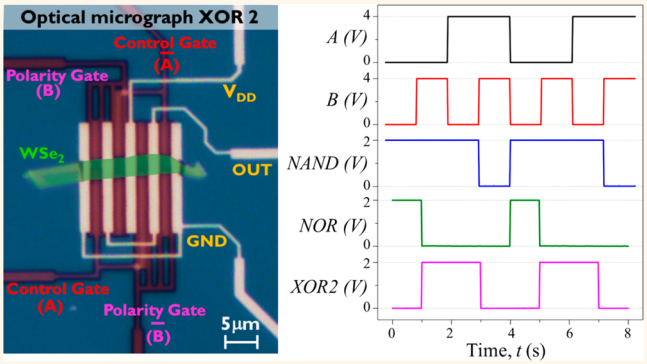
Supporting Information

**ABSTRACT:** Atomically thin two-dimensional (2D) materials belonging to transition metal dichalcogenides, due to their physical and electrical properties, are an exceptional vector for the exploration of next-generation semiconductor devices. Among them, due to the possibility of ambipolar conduction, tungsten diselenide ($WSe_2$) provides a platform for the efficient implementation of polarity-controllable transistors. These transistors use an additional gate, named polarity gate, that, due to the electrostatic doping of the Schottky junctions, provides a device-level dynamic control of their polarity, that is, n- or p-type. Here, we experimentally demonstrate a complete doping-free standard cell library realized on $WSe_2$ without the use of either chemical or physical doping. We show a functionally complete family of complementary logic gates (INV, NAND, NOR, 2-input XOR, 3-input XOR, and MAJ) and, due to the reconfigurable capabilities of the single devices, achieve the realization of highly expressive logic gates, such as exclusive-OR (XOR) and majority (MAJ), with fewer transistors than possible in conventional complementary metal-oxide-semiconductor logic. Our work shows a path to enable doping-free low-power electronics on 2D semiconductors, going beyond the concept of unipolar physically doped devices, while suggesting a road to achieve higher computational densities in two-dimensional electronics.




**KEYWORDS:** *two-dimensional semiconductor, $WSe_2$, electrostatic doping, polarity control, reconfigurable, logic gates, standard cell library*

Dimensional scaling has been the main drive of the silicon industry in recent decades. The growth of information technology has been sustained by the miniaturization of complementary metal-oxide-semiconductor (CMOS) field-effect transistors (FETs),[1] with the number of devices per unit area constantly increasing, as exemplified by Moore's law.[2] Modern digital integrated circuits (ICs) contain billions of transistors and logic gates, fabricated with CMOS technology. In CMOS, silicon is physically doped during the fabrication process with ion implantation to create unipolar devices with Ohmic contacts. The doping process irreversibly sets the polarity of the transistors (n- or p-type) according to the dopant atoms used (arsenic (As) for electron and phosphorus (P) for hole doping). With the physical gate length of modern devices approaching 10 nm, ion implantation has become increasingly more complicated to control.[3,4] Fluctuations in number of dopant atoms present in the transistor channel are responsible for an increased variability of the threshold voltage of the devices.[4] In addition, ion implantation requires high-temperature annealing to repair damages in the silicon and achieve proper dopant activation.[5,6] This high-temperature process is not compatible with the process for monolithic 3D-CMOS, which requires a low

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thermal budget. A device concept that would not rely on any physical doping and use undoped materials would be of great interest in this regard. Undoped materials are, for the most part, able to conduct both charge carriers (*i.e.*, electrons and holes), a property which is called ambipolarity, and usually create Schottky barriers (SB) at the contact interface with a metal. However, a purely ambipolar device would be difficult to switch off with a standard gate configuration, as we cannot selectively suppress the injection of one type of charge carrier.[7,8] The key to unlock the possibility of controlling the polarity of the transistor is the separate gating of different channel regions, due to a double-independent-gate structure.[8] By adding a second gate, which we refer to as polarity gate (or program gate, PG), we are able to induce electrostatic doping at the contact interfaces and block the injection either of electrons or holes. It is then possible to dynamically reconfigure the device polarity at run time, by reversing the bias applied to the polarity gate. A conventional gate, named control gate, acting in the central region of the channel modulates a potential barrier in the semiconducting material controlling the ON/OFF state of the device. The possibility to dynamically change the polarity at run time enhances the switching property of the transistors, enabling a doping-free, highly flexible design for logic circuits.[9] Polarity-controllable devices have been demonstrated using a variety of semiconducting materials;[8,10−20] however, the fabrication of complex logic gates, exploiting the polarity control of the transistors, has only been shown on silicon.[11,20] Here, we report a library of logic gates realized with two-dimensional polarity-controllable transistors.

Two-dimensional semiconductors of the transition metal dichalcogenide (TMDC) family[21] have recently attracted the attention of the scientific community in view of their structural and electronic properties.[22−24] With sub-nanometer single layers, providing optimal electrostatic control,[25−27] a significant energy band gap, and the promise of dangling-bond-free interfaces,[22−24] avoiding surface scattering, 2D-TMDC semiconducting materials, such as molybdenum disulfide ($MoS_2$) and $WSe_2$, have been extensively studied.[28−33] Rigorous quantum transport simulations have also been carried out to assess the performances of 2D semiconductor devices at ultrascaled gate lengths, in the case of both unipolar physically doped devices[43,44] and doping-free polarity-controllable transistors.[45] Continuous progress in the growth of 2D materials[34−36] in testing and understanding of their properties[37−39] and in the demonstration of device concepts[40−42] keeps the spotlight on this family of materials. Complex logic circuits have been demonstrated with 2D semiconductors[29,46] using a pseudo-n-MOS logic, with n-type $MoS_2$ transistor, which does not have the power consumption benefits of CMOS. However, physical doping of 2D materials is still an open challenge, and the realization of CMOS logic gates on 2D semiconductors has only been achieved with the use of chemical doping and different metal contacts[31,32] or using two different materials for n- and p-type devices.[33] Both methods greatly complicate the fabrication process and, in the case of chemical doping, make it nonscalable and noncompatible with conventional CMOS fabrication. When no physical or chemical doping is introduced, contact to a 2D semiconductor usually results in the creation of a Schottky barrier. Thus, the use of electrostatic doping of the contact regions to reversibly select the polarity of the transistor adapts perfectly to these emerging class of materials and provides a path for the realization of CMOS logic with the use of a single two-dimensional ambipolar semiconductor. The most known TMDC material, $MoS_2$, has proven to be a viable solution for the realization of n-MOS transistors,[28,29] and ultrascaled devices have been recently demonstrated.[25−28] Despite recent work that has shown the possibility of achieving ambipolar behavior in $MoS_2$,[47] due to hexagonal boron nitride (h-BN) tunneling contacts, the partial Fermi level pinning at the contact interface[48] remains challenging to overcome without greatly complicating the fabrication process. Moreover, the higher band gap reported for $MoS_2$, with respect to that of $WSe_2$ and other 2D materials such as zirconium selenide ($ZrSe_2$) and hafnium selenide ($HfSe_2$),[37] makes it less appealing for polarity-controllable applications, as it would produce higher Schottky barriers, thus limiting carrier injection at the contacts.[45] $WSe_2$ has shown high carrier mobility[49] and ambipolar behavior,[7,8] and CMOS-like devices have been reported experimentally with chemical doping of the material.[31,32] Recently, polarity-controllable transistors have been shown on 2D tungsten diselenide ($WSe_2$), achieving ON/OFF ratios higher than $10^6$ for both n- and p-type behavior in a single device,[8] making it arguably the best candidate for further exploration of the potential of reconfigurable devices. However, to be best of our knowledge, a complete basis for an effective standard cell library of two-dimensional logic gates, fabricated with polarity-controllable devices, has not been demonstrated yet.

In this paper, we use two-dimensional semiconducting material to fabricate highly expressive doping-free logic gates using polarity-controllable devices. We exploit the presence of Schottky barrier contacts in $WSe_2$, and due to electrostatic doping, we achieve dynamic control of the polarity of the transistor, removing the need for any physical or chemical doping during the fabrication process. We fabricate and characterize a variety of polarity-controllable logic gates such as inverters (INV), negative-AND (NAND), and negative-OR (NOR) that are the building primitives used in the logic synthesis frameworks for conventional CMOS logic. Moreover, we experimentally show 2-input XOR (XOR-2), 3-input XOR (XOR-3), and Majority (MAJ) gates that, due to the polarity-controllable devices, can be realized with fewer transistors than what is achievable in conventional CMOS. We demonstrate a complete standard cell library with the possibility of fabricating compact, highly expressive logic gates that can be exploited to gain advantages at circuit level, using XOR and MAJ functions as logic primitives.[50−53]

## RESULTS AND DISCUSSION

**Fabrication of Logic Gates and Design Regularity.** For our experiments, we use $WSe_2$ flakes prepared by mechanical exfoliation from commercially available bulk crystals. The flakes are exfoliated on a $Si/SiO_2$ substrate and then transferred (see Materials and Methods and Supporting Information S1) on a target substrate with prepatterned back-gates (2 nm Ti/10 nm Pt) isolated with $ZrO_2$ deposited by atomic layer deposition (details on the fabrication process are presented in Materials and Methods and Supporting Information S2). The addition of the polarity gate enables us to use a single semiconducting material for the realization of both n- and p-type transistors, without the addition of physical or chemical doping. This is a great advantage because the latter greatly complicates the fabrication process, often making it nonscalable and non-CMOS compatible. Figure 1a shows a



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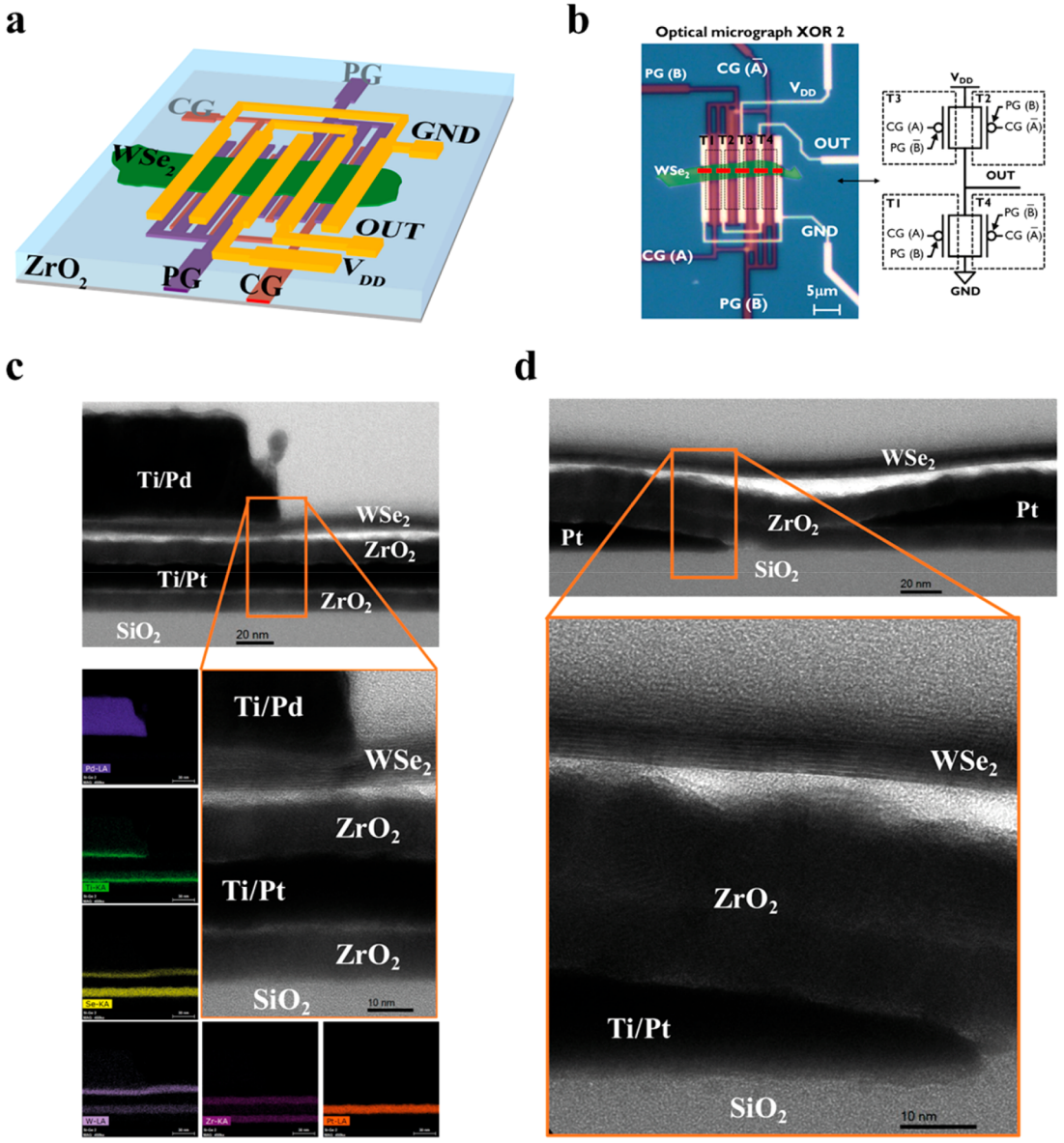


**Figure 1. 2D-$WSe_2$ polarity-controllable two-input XOR and cross-sectional TEM with EDX mapping. (a) Cartoon of the $WSe_2$ 2-input XOR logic gate with platinum buried gates (CG and PG) and titanium/palladium contacts. (b) Optical micrograph of the fabricated 2-input XOR gate, with corresponding circuit schematic highlighting the position of the four transistors and the logic inputs acting on them. The red dashed line indicates the position where the TEM cross sections are taken. (c,d) Cross-sectional TEM image of the contact region with EDX mapping (c) and of the central region of the device, showing the separation between CG and PG (d). Note that the EDX mapping for selenium (Se) and tungsten (W) also shows a false signal due to the overlap between the Se, W, and Pt peaks used during the measurements. Se and W are present only in the top 2D layer. The white region between the $ZrO_2$ and the $WSe_2$ is empty space, as confirmed by the lack of C atoms in the region (see Figure S4). It is probably caused by partial delamination of the 2D flake, occurring during the focused ion beam sample preparation.**

cartoon schematic of a 4-transistor XOR-2, with an optical micrograph of the device and the corresponding circuit schematic presented in Figure 1b. Each transistor has now two independent gates that can be biased with different logic inputs (*e.g.*, CG (A) is a control gate biased with logic input A and PG (B) is a polarity gate biased with logic value B). The design of the polarity and control gate (PG and CG, respectively) was chosen in order to allow the use of a single $WSe_2$ flake for the fabrication of each logic gate. Moreover, the PG and CG structures are identical for all the fabricated logic gates (except for the inverter design), creating a universal gating structure that enables a highly regular and flexible design of the logic gates. In fact, different logic gates can be obtained from the same gating structure by wiring differently the source and drain contacts of the transistors (see Figure S2.2). The fabricated logic gates (NAND, NOR, XOR-2, XOR-3, and MAJ) have four polarity-controllable transistors (except for the INV, which has 2) that share the same semiconducting $WSe_2$ flake but behave with opposite polarities according to the bias applied to the respective PG. The TEM cross section taken at the contact interface (see Figure 1c) shows the PG buried structure isolated by $ZrO_2$, with the 2D-$WSe_2$ flake on top and the Pd contact. Energy-dispersive X-ray (EDX) spectroscopy confirms the elemental composition of the device. Figure 1d focuses in the central region of the channel and shows the separation (~60 nm) and $ZrO_2$ isolation between the CG and



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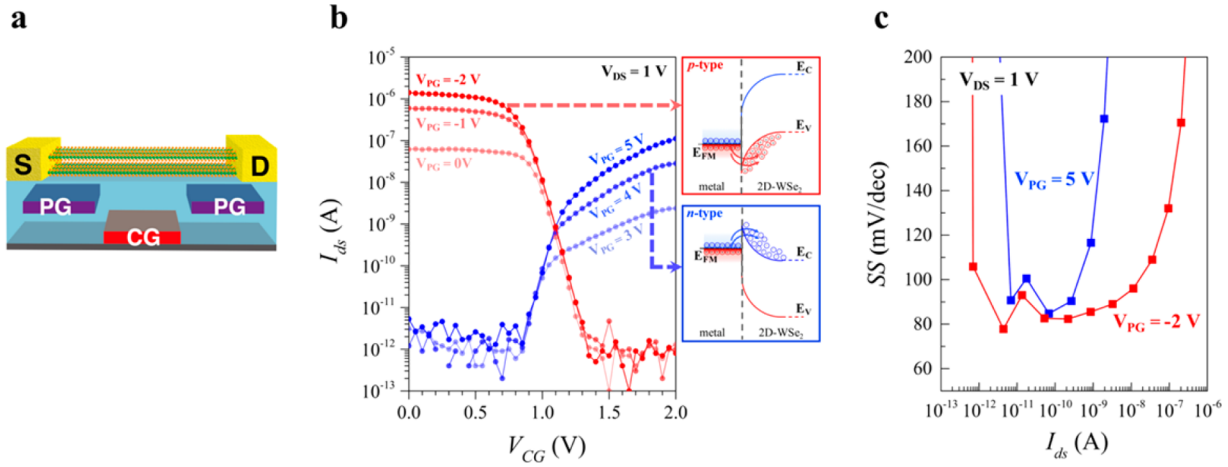


**Figure 2. Polarity-controllable device characteristics (a) Cartoon of the cross section for a single device, showing the position of the PG and CG with respect to the 2D semiconducting channel. (b) Transfer characteristics showing ambipolar conduction and demonstrating the polarity-controllable behavior. The p-type (n-type) operation is achieved for $V_{PG}$ < 0 V (>3 V). The insets show the effect of the PG on the Schottky barrier, leading to the injection of only one type of charge carriers. (c) Subthreshold slopes extracted from the transfer characteristics presented in (b) for $V_{PG}$ = 5 V and $V_{PG}$ = −2 V.**

the PG structures. The atomic layers of the 2D-$WSe_2$ are clearly visible in the zoomed-in views of Figure 1c,d, and the thickness of the transferred flake can be estimated to be around 6 nm.

**Characterization of a Single Device.** As mentioned above, the regular and flexible design for the logic gates is made possible by the switching properties of the single polarity-controllable devices that are also enabling the compact fabrication of the XOR-2 gate, which is presented in Figure 1a,b. We will now decompose the behavior of our logic gate and study in detail the switching properties of the single polarity-controllable devices fabricated with the process presented above. Figure 2a shows a 3D schematic cross section of a single device, highlighting the multilayer 2D semiconducting channel and the overlap between the PG and the source and drain contacts, which is necessary to ensure optimal modulation of the Schottky barrier. The CG gate controls the ON/OFF state of the device.

Ambipolar conduction and polarity control behavior are observed, as shown in Figure 2b. When the PG is biased at 0 V or below, holes are favorably injected in the channel and the device behaves as a p-type transistor. Conversely, the transistor is programmed to function as a n-type device when the PG is biased at 3 V and above. In both cases, the CG is able to turn the transistor ON and OFF when swept between 0 and 2 V. It appears that a higher voltage range is needed to flip the transistor polarity, using PG, with respect to the voltage needed to control the potential barrier in the channel, using the CG. We believe this difference stems from the different mechanism that the two gates are exploiting, that is, electrostatic doping of the Schottky junction and modulation of a potential barrier in the channel, with a different band movement factor probably occurring for the two gates. We achieve high ON/OFF ratios of $10^5$ and $10^6$ for n- and p-type conduction, respectively, on the same device. The asymmetry between the n- and p-type transfer characteristics, with the p-current around 10× higher than the n-current, stems from the nonperfect midgap contact alignment, creating asymmetric Schottky barriers for electrons and holes, which was achieved with Ti/Pd contacts. Current flow in a Schottky barrier FET (SB-FET) is the result of two separate conduction mechanism across the barrier: (i) thermionic emission of carriers over the top of the barrier and (ii) tunneling of charge carriers through the Schottky barrier.[54] Here, the PG acts both at the contact interface between the metal and the semiconductor and also on the region underneath the contact (as can be seen in Figure 1a), which is essential to have an efficient charge injection. It has been recently shown how the gate-induced modulation underneath the contacts (contact gating), provides additional tunneling paths that allow a better carrier injection in the 2D semiconductor.[55] Biasing the PG leads to accumulation of mobile charges underneath and at the contact interface, providing electrostatic doping of the 2D-$WSe_2$ and considerably thinning the SB. Tunneling of charge carriers through the thinned barrier thus becomes much more favorable. The control of the PG on the barriers is evident as changing the PG bias from 0 to 3 V results in a complete switch of the transistor polarity. However, because the transmission of charge carriers through the barrier depends exponentially on the barrier height (for both thermionic emission and tunneling),[54] it is essential to ensure a midgap contact to have symmetric barrier heights for electrons and holes. Future work will focus in improving the symmetry between the n and p branch, which is a desired feature for circuit operation,[20] exploring different metals or introducing graphene to finely tune the Fermi level alignment at the contacts. Moreover, in our previous studies,[8] we found the Ti/Pd contact to $WSe_2$ to provide an enhanced electron conduction, with the n-current roughly 10× higher than that of the p-current. We attribute this difference to the change in the dielectric environment ($Al_2O_3$ in our previous work, and $ZrO_2$ in this work) that could lead to a different doping of the semiconducting 2D-$WSe_2$. Further experiments would be needed to assess the influence of the dielectric environment on the conduction properties of 2D materials but are outside of the scope of this work. The extrinsic mobility, extracted from the transfer characteristics (see Supporting Information S3), is 1.5 and 0.1 $cm^2\ V^{-1}\ s^{-1}$ for hole and electron conduction, respectively. These values are smaller than those reported in the literature for $WSe_2$[31,32] and are determined by the presence of large Schottky barriers at the contacts, the lack of a top high-$\kappa$ passivation, and the presence of interface charges at the $ZrO_2/WSe_2$ interface that could increase charge scattering



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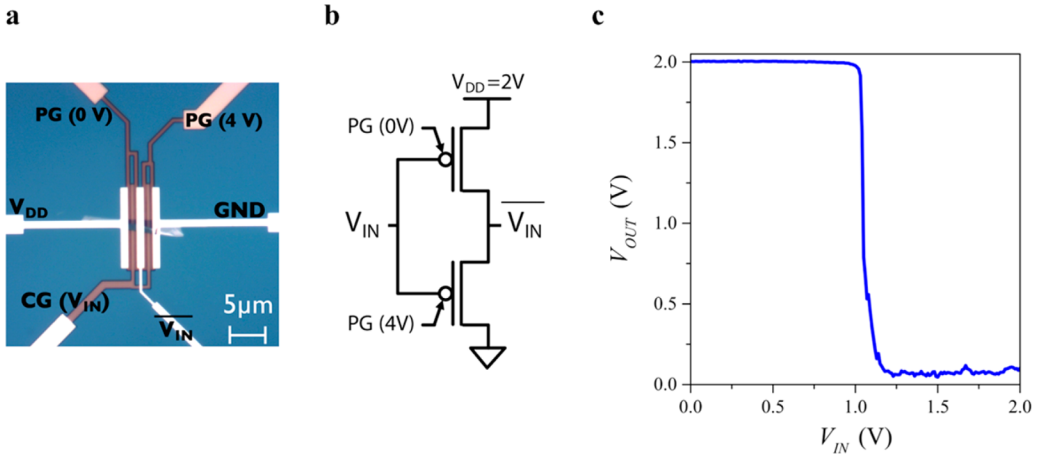


**Figure 3. Inverter behavior. (a) Optical micrograph of the fabricated inverted with the terminal names reported. (b) Corresponding circuit schematic, showing the voltage bias on the program gates. (c) Measured inverter behavior for $V_{DD}$ = 2 V, showing a sharp transition between the "1" and "0" state around $V_{DD}/2$.**

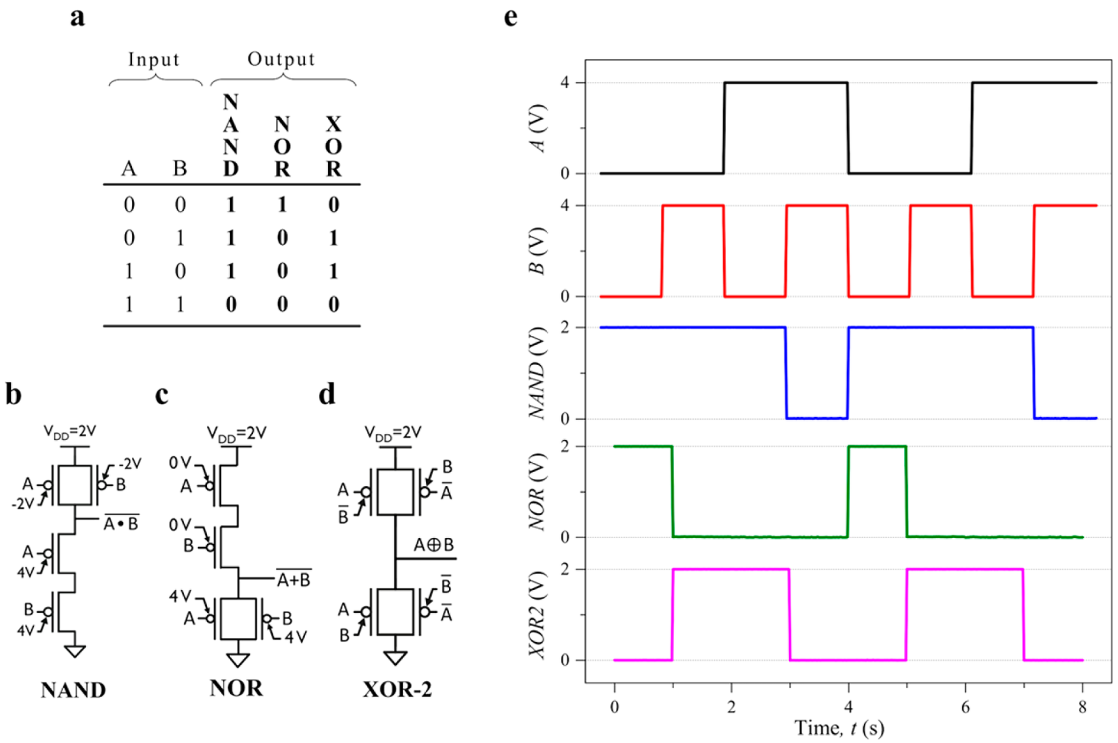


**Figure 4. Two-input logic gates. (a) Truth table of the NAND, NOR, and XOR-2 logic functions. (b–d) Circuit schematic of the logic gates describing where the logic inputs are applied and showing the fixed bias of the PG in the case of NAND and NOR gates. (e) Experimental waveforms demonstrating the operation of the NAND, NOR, and XOR-2 gates fabricated with polarity-controllable $WSe_2$ transistors.**

phenomena in the channel. Due to the scaled high-$\kappa$ oxide and the use of platinum gates, p-type operation is achieved when biasing the PG and the CG at ground (GND), which is an essential step to ensure the cascadability of the devices. Moreover, the use of scaled high-$\kappa$ $ZrO_2$ creates a high gate capacitance that translates into improved electrostatic control over the channel. We measured subthreshold slopes (SS) below 100 mV/dec over 2 and 4 decades of current for n- and p-type conduction, respectively (see Figure 2c). The minimum SS achieved for both electrons and holes of ~85 mV/dec roughly translates into an interface trap density ($D_{it}$) on the order of $2.5 \times 10^{12}$, which is in good agreement with previous literature on 2D materials[37] (see Supporting Information S3).

**Demonstration of Logic Gates.** When using polarity-controllable transistors to fabricate INV, NAND, and NOR functions, the program gates are biased at a fixed value, setting the polarity of the transistor, and the gates are arranged in a CMOS-like fashion (see Figure S2.3) with logic inputs only applied on the CG. For the case of an INV (see Figure 3a,b), proper operation of the logic gate is achieved biasing the PG at 0 and 4 V for the p- and n-type transistor, respectively, while having $V_{DD}$ = 2 V. The inverter behavior is verified (see Figure 3c), achieving high inverter gains ($d(V_{OUT})/d(V_{IN}) > 30$), as exemplified by the desirable sharp transition between the high and low state at around $V_{DD}/2$. The imbalance in the transition is caused by the different drive current in the n- and p-type



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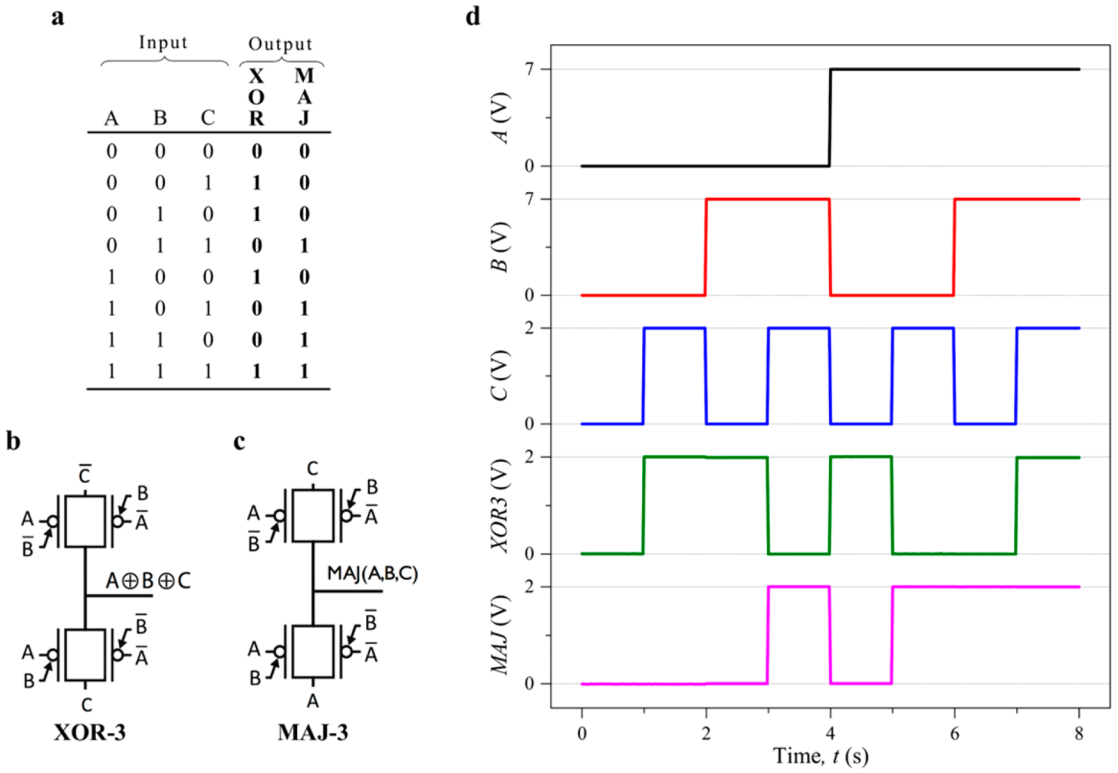


**Figure 5. Three-input logic gates. (a) Truth table of the XOR-3 and MAJ-3 logic functions. (b–d) Circuit schematic of the logic gates describing where the logic inputs are applied. (e) Experimental waveforms demonstrating the operation of the XOR-3 and MAJ-3 gates fabricated with polarity-controllable $WSe_2$ transistors. For the MAJ-3 gate, the logic input A applied at the GND terminal is kept between 0 and 2 V, and the input on the gates is kept between 0 and 7 V.**

operation mode, as mentioned in the previous section, and can be addressed by finely tuning the contacts.

Using the universal gating structure presented in Figure 1, we are able to fabricate NAND and NOR gates with a conventional CMOS-like design (see Figure 4 and Figure S2.3). The PG of the transistors are biased at a fixed voltage, whereas the logic inputs, A and B, are only applied to the CG of the transistors. We verified the functioning of the NAND and NOR gates for $V_{DD}$ = 2 V, while keeping the bias of the logic inputs between 0 and 4 V. Although for the NOR gate the PG is biased with the same voltage levels of the logic inputs, in the case of the NAND gate, in order to achieve the proper logic behavior, we apply a negative bias of −2 V to the PG of the p-type device. This is most likely caused by some residues on the channel or under the contacts that are preventing the transistor from efficiently conducting holes at $V_{PG}$ = 0 V. Moreover, flake-to-flake variations, both in terms of thickness and defect density, can also contribute to the variation in the bias that needs to be applied to the polarity gates.

At this stage, we have demonstrated how polarity-controllable 2D-$WSe_2$ transistors can be used to replicate CMOS-like logic gates. However, the real advantage in the use of polarity-controllable transistors with respect to CMOS comes only when exploiting the PG as a logic input, unlocking the enhanced switching properties of the devices. Having a logic input connected to the PG implies that the polarity of the device is no longer fixed and will change at run time according to the logic value of the signal (*e.g.*, p-type for logic "0" and n-type for logic "1"). With this configuration, only possible due to the enhanced expressive switching function of the single devices (see Figure 2), we can achieve highly compact implementation of XOR and MAJ functions with fewer transistors than what is achievable in conventional CMOS. Disregarding the inverters needed to generate the complemented inputs ($\overline{A}$ and $\overline{B}$), the XOR-2 is realized with only four polarity-controllable devices, whereas a conventional CMOS design would require eight transistors. We show the operation of the XOR-2 gate, as shown in Figure 4d,e, with all the logic inputs acting between 0 and 4 V, thus assuring the full cascadability of the gate. As shown in the circuit schematic of the XOR-2 gate (see Figure 4d), logic input B is now acting on PG and not on CG as was the case for the NAND and NOR gates. It is important to notice that in contrast to the transfer characteristics presented in Figure 2b, where the CG was only swept between 0 and 2 V, we are now operating both the CG and PG between 0 and 4 V. There is no drawback in further sweeping the CG up to 4 V as the current levels would just remain constant in either p-type OFF state or n-type ON state. By replacing the $V_{DD}$ and GND terminals with additional inputs, we are also able to demonstrate the logic operation for a highly compact four transistors XOR-3 and MAJ, as shown in Figure 5. These gates were realized on a thicker high-$\kappa$ oxide (20 nm instead of 10 nm), thus requiring a higher voltage range for the logic inputs applied on the gates (between 0 and 7 V). For the proper operation of the logic gates, the signals replacing the $V_{DD}$ and GND terminals (C, $\overline{C}$, and A, C for the XOR-3 and MAJ-3, respectively) are instead kept between 0 and 2 V. This limitation can be overcome by further scaling the gate oxide, allowing all logic inputs to have the same voltage range. XOR-3 and MAJ-3 are fundamental logic primitives that are present in virtually any arithmetic operator (consider that a


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1-bit adder can be realized by a MAJ-3 gate to generate the carry out and a XOR-3 gate to generate the sum) but are not efficiently realizable in CMOS logic. The possibility of having an efficient realization of these functions enables their use as powerful logic primitives during the logic synthesis flow, providing considerable advantages at circuit level.[50−53]

## CONCLUSIONS

Here, we have investigated the potential advantages in the use of polarity-controllable two-dimensional transistors for next-generation electronic devices, highlighting a path toward the achievement of higher computational densities in two-dimensional electronics. We have shown a complete basis for an effective standard cell library of logic gates (INV, NAND, NOR, XOR-2, XOR-3, and MAJ-3), fabricated with $WSe_2$ polarity-controllable transistors. These devices, due to the addition of the polarity gate, allowed us to exploit the electrostatic doping of the source and drain Schottky junctions to dynamically set the polarity of the transistors at run time, removing the need for any physical or chemical doping. We tested individual transistors and demonstrated polarity-controllable behavior, achieving ON/OFF ratios $>10^5$ for both polarities on the same device with subthreshold swings as low as 80 mV/dec. The enhanced switching properties of the single devices allowed us to experimentally demonstrate highly compact and expressive XOR and MAJ gates, with fewer transistors than possible in a conventional CMOS logic.

## MATERIALS AND METHODS

**PMMA Dry Transfer Process.** For the dry-transfer process, we use thick (~10 $\mu$m) spin-coated poly(methyl methacrylate) (PMMA) as transferring agent. After the flake is selected for transfer, PMMA is spin-coated on the sample and annealed at 165 °C on a hot plate. We then dice the PMMA around the flake using a microengraver, and upon release of the $WSe_2$/PMMA stack, we pick it up using a microneedle. The $WSe_2$/PMMA stack is then transferred to the target substrate and aligned with respect to the buried program gate by a manual pick-and-drop process. Adhesion of the $WSe_2$/PMMA stack is assured by 2 min hot plate annealing at 190 °C. Finally, PMMA is dissolved using dichloromethane, and the sample is cleaned with a hot acetone bath (~12 h) to ensure the absence of PMMA residues. In Figure S1, (i) $WSe_2$ has been exfoliated on the 20 nm $SiO_2$/Si substrate, (ii) and (iii) show schematically the PMMA adhesion to the flake and the PMMA release process. In (iv), the transferred flake is aligned with respect to the PG buried structures on the target substrate. The PMMA is finally dissolved after another annealing step, and (v) shows the transferred flake.

**Device Fabrication.** The $WSe_2$ flakes are exfoliated from commercially available synthetic crystal, provided by HQ-graphene, using a standard low-tack dicing tape. The flake characterization is performed with a dimension edge AFM from Bruker in tapping mode and with Raman analysis (see Figure S2.1). The fabrication process is depicted in Figure S2.2. We use a double-layer resist consisting of LOR1A and PMMA resist (solution with 3% chlorobenzene) for the patterning of the CG buried gate (i). The LOR1A is spinned for 45 s at 4500 rpm and subsequently baked on a hot plate for 5 min at 190 °C. The PMMA layer is then spinned for 45 s at 4500 and then baked on a hot plate for 5 min at 120 °C. After exposure, the PMMA resist is developed in a 1:1 solution (at 20 °C) of methyl isobutyl ketone and isopropyl alcohol for 42 s. The LOR1A is developed with a 3 s dip in OPD5262 followed by rinsing in deionized water. After the gate metal deposition (2 nm Ti/10 nm Pt), done with a commercial electron gun evaporator tool, lift-off is carried out in hot acetone (50 °C) for around 2 h. The remaining LOR1A resist is then removed in OPD5262. High-$\kappa$ $ZrO_2$ (10 nm) is deposited with atomic layer deposition at 250 °C using an AMAT Centura III−V module with TEMAZ/$H_2O$ precursor (ii), and then the PG structures are defined with the same process described for CG (ii). The PG structures are isolated from the flake with high-$\kappa$ $ZrO_2$ (10 nm), and the flake is then transferred on top of the buried structures (iii). We use a single-layer PMMA recipe for the pattering of the metal contacts, in order to avoid exposure of the 2D material to OPD5262 (LOR1A developer) and water. The source and drain contacts (2 nm Ti/50 nm Pd) are then evaporated with a commercial electron gun evaporator tool. The Ti is directly in contact with the $WSe_2$ and acts as an adhesion layer between the 2D flake and the Pd.

An annealing step is then performed at 200 °C for 12 h in a Nabetherm open-tube furnace in vacuum with a constant argon (Ar) flow of 0.5 L/h. The same design of the wiring can be used for the realization of NAND and NOR gates (iv), whereas a different wiring is needed to realize XOR-2, XOR-3, and MAJ gates. Figure S2.3 shows optical micrographs and circuit schematics for all the fabricated logic gates.

**Device Characterization.** All electrical measurements were performed at room temperature in $N_2$ environment using a Keithley 4200 semiconductor characterization system with a preamplifier probe station. The current measurements were performed with autorange setting allowing for highest accuracy (1% of reading +10 fA) on off-current measurements.

## ASSOCIATED CONTENT

### Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.8b02739.

Detailed flake transfer procedure schematic, complete fabrication process schematic, optical image and circuit of fabricated logic gates, method for the extraction of interface trap density and detailed EDX map of the device (PDF)

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### Author Contributions

G.V.R. fabricated the experimental devices, performed the measurements, and analyzed the data presented in the paper. Y.B. helped develop the flake transfer procedure. Y.B., D.L., I.P.R., F.C., P.-E.G., and G.D.M. helped interpret the experimental results. G.V.R. wrote the manuscript with contribution from all authors.

### Notes

The authors declare no competing financial interest.

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After this paper was published ASAP June 29, 2018, a correction was made to Figure S2.2 in the Supporting Information. The corrected version was reposted July 5, 2018.



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