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A 4GS/s 39.9dB SNDR 11.7mW Hybrid Voltage-Time Two-Step ADC with Feed-Forward Ring Oscillator Based TDCs

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Abstract—This paper presents a single-channel high-speed hybrid voltage-time two-step ADC. Two time-based converters (TBCs) are pipelined by a capacitive DAC (CDAC) and a residue amplifier (RA). The proposed hybrid architecture minimizes the impact of the TBCs non-linearity while maintaining a low power consumption for a high sample rate. A unipolar voltage to time converter (VTC) and a ring oscillator (RO) based time to digital converter (TDC) with feed-forward and $2\times$ interpolation is used as TBC which ensures high-speed and low-power operation. The prototype ADC is fabricated in 28nm CMOS. At 4GS/s and a Nyquist input frequency, it achieves 39.9dB SNDR and 47.8dB SFDR for a power consumption of 11.7mW. The FOM_W and FOM_S are 36.2fJ/conv-step and 152.2dB, respectively.

Index Terms—Analog to digital converter (ADC), ring oscillator, time-based ADC, time-to-digital converter (TDC), voltage-to-time converter (VTC).

I. INTRODUCTION

CMOS technology scaling results in higher switching speeds, which enables a finer resolution in the time domain. On the contrary, due to reduced supply voltages in scaled technologies, the dynamic range in the voltage domain decreases, resulting in an ever-decreasing signal-to-noise ratio (SNR). Therefore, in order to solve the design difficulties imposed by the digital driven technologies, time-based ADCs become more and more interesting [1]. Prior work has shown that time domain processing can provide a better efficiency compared with traditional voltage domain processing [2]–[6].

However, time domain conversion has its own drawbacks. To adopt to the fact that most real world signals are in the voltage domain, a VTC is needed to convert the information from the voltage domain to the time domain. The linearity of this VTC is typically limiting the performance of such a time-domain ADC [2]. Regarding the TDC, due to its flash nature, the complexity and power consumption become excessive as the resolution increases [3], [4].

To resolve these problems, this paper proposes a single-channel hybrid voltage-time two-step ADC that is both simple and low power. The proposed ADC splits the full 7-bit time domain conversion into two 4-bit pipelined steps with 1-bit redundancy. As a result, the complexity of the TDC is reduced significantly. At the same time, the linearity requirements for the VTC are relaxed, making it possible to reach high speed while maintaining a low power consumption.

The paper is organized as follows. The proposed hybrid voltage-time architecture is introduced in Section II.

Section III analyzes the detailed circuit implementations. Experimental results are presented in Section IV. Finally, Section V draws the conclusion.

II. HYBRID VOLTAGE-TIME ARCHITECTURE

Fig. 1 shows the architecture of the proposed hybrid voltage-time two-step ADC and its timing diagram. Unlike [6], the input voltage $V_{\text{inp}}-V_{\text{inn}}$ is first sampled twice through the bootstrapped switches, so the two stages are fully decoupled. The mismatch between the two sampled voltages is transferred to the CDAC residue voltage, which can be corrected by the redundancy in the digital domain afterwards. Two 4-bit TBCs are used in both the first and the second stages with 1-bit redundancy in between, resulting in a 7-bit resolution. To further increase the efficiency, the complexity of the TDC in the TBC is reduced from 4-bit to 3-bit by introducing a voltage domain comparator. This comparator operates in parallel with the VTC and produces a sign bit based on the voltage domain polarity. Since the sign bit is the MSB of the signal, the dynamic range of the TDC is halved and its conversion speed is doubled. When the first conversion finishes, the corresponding output bits are applied to the CDAC, which generates the residue voltage. Because of the flash nature of the TDC, this CDAC is thermometer coded with eight identical unit capacitors C_u of 6fF. Ideally, in order to minimize power consumption and area, one would minimize the size of C_u toward the kT/C noise and matching requirements. For example, a 100aF unit capacitor is sufficient to meet the noise and matching requirements. However, in this ADC, the size of C_u is limited by the non-linear parasitics from the S/H switches and the input gates of the RA, thanks to the double sampling scheme, the parasitics from the first stage are isolated. Due to the non-linear parasitics, the unit capacitor has to be large enough to ensure a 7-bit CDAC linearity. C_1 is chosen to be 12fF for the same reason. In contrast to the need for a successive register control logic in a SAR ADC, the proposed hybrid voltage-time architecture allows to directly connect the TBC₁ outputs to the CDAC switches with simple buffers. Thus, the critical path is shorter making this architecture more suitable for high speed operations.

The dynamic RA amplifies the residue voltage and decouples TBC₁ and the thermometer CDAC from TBC₂ to guarantee a true pipelined operation. Thanks to the 1-bit redundancy, the limited accuracy of the dynamic RA gain and

Fig. 1. Architecture of the proposed single-channel hybrid voltage-time two-step ADC, timing diagram and circuit schematic of the dynamic RA.

the mismatch of the first stage can be compensated. TBC₂ resolves the last 4 bits. A digital encoder converts the 16-bit thermometer code to a 7-bit binary output.

Compared with a 7-bit time domain converter whose complexity can be expressed as 2^7 , the complexity of this two-step ADC is reduced to 2×2^4 (4-bit in each step). Since the power consumption and the conversion time are proportional to the complexity of a time domain converter, the two 4-bit TDCs are four times better than the one with 7-bit in a single stage in terms of power and speed. A 7-bit TDC also poses more stringent requirements on matching, which further increases the power and area. As the 7-bit linearity is preserved by the CDAC, the two-step architecture reduces the linearity requirements for the VTC from 7-bit to 4-bit, which also saves a significant amount of power. Then The relaxed requirements of the TDC and VTC come at the cost of the need for the RA. Since the two stages are pipelined by the RA and the time consumed by the RA is much less than the time consumed by the VTC and TDC, only a small penalty (16%) is added to the full period. The RA operates in the voltage domain because voltage domain amplification is more accurate and a time domain residue is difficult to generate. By utilizing both the voltage domain and time domain advantages, this ADC is able to both reach high speed and low power simultaneously.

III. CIRCUIT IMPLEMENTATION

Since the two-step architecture relaxes the VTC linearity requirement, a simple current source based VTC is implemented to ensure a high speed operation. The unipolar VTC used in both stages is shown in Fig. 2. It converts positive

as well as negative differential voltages into an absolute time difference. First, the differential input voltage is stored on the capacitors C_1 at the input nodes V_p and V_n . When Φ_{VTC} goes high, the input capacitors are discharged with a current that is controlled by the biasing voltage $V_{bias_{VTC}}$. Once V_p and V_n cross the threshold voltage of the inverters, two rising edges R_p , R_n are generated, the time between which is a measure of the voltage difference between V_p and V_n . To ensure sufficient linearity, the inverter threshold voltage is designed so that M_1 and M_2 never enter the triode region. Followed by an XOR gate, the time domain information is converted into a pulse EN, of which the duration is proportional to the absolute value of $|V_p - V_n|$. To resolve the sign information, a voltage domain comparator compares the differential input voltage and produces a sign bit during the voltage to time conversion. As a result, this unipolar TDC only requires half of the dynamic range compared to a polar TDC [2]. This also saves area and power, since the comparator is smaller and consumes less power than the TDC. Unlike the SAR ADCs whose comparator metastability can happen in any of the comparison cycles, the metastability in this ADC only happens when the input is small. Moreover, since the voltage-domain comparison is in parallel with the time-domain conversion, it has more time to resolve the metastability states.

The speed of a traditional delay line based TDC is usually limited by the intrinsic inverter delay of the technology [3]. In order to break this speed limitation, cross-coupled feed-forward and $2 \times$ interpolation are used in this ADC. As shown in Fig. 3, cross-coupling inverters are inserted in between the two 5-stage ROs to create pseudo-differential outputs for the CDAC. The feed-forward is implemented by

Fig. 2. Circuit diagram of the unipolar VTC.

Fig. 3. Circuit diagram of the cross-coupled feed-forward RO TDC with 2× interpolation.

connecting the inverters two stages ahead to the opposite side. For example, n_1 is connected to p_3 and p_1 is connected to n_3 . The cross-coupled feed-forward inverters also improve the delay uniformity and thus the linearity. This feed-forward technique increases the oscillation frequency by approximately 50%. To further increase the speed, the 2× interpolator uses two inverters with their outputs shorted to produce an intermediate phase ($2i+1$ in Fig. 3) [2]. It doubles the resolution of the TDC without sacrificing the conversion speed. T_p and T_n are the differential TDC outputs. The simulated LSB for the RO based TDC is only 3.5ps ($T[2i+1]-T[2i]$) in 28nm technology. Since the TDC only operates during a small portion of the clock cycle, the full RO based TDC is power gated by the EN signal from the VTC. The EN signal enables the TDC and resets it to an initial phase before every conversion. Compared to a free-running RO, the RO in this ADC always starts from a reset phase, which eliminates the need for a cyclic output code decoder to subtract two phases.

The dynamic RA amplifies the residue from the first stage. At the same time, this dynamic RA is used as the pre-amplifier for the comparator which provides the sign bit for TBC₂. Therefore, only an additional latch is required to implement this comparator. The common-mode detector (CMD) in the dynamic RA is realized by two capacitors and a NOR gate. The two capacitors connect the differential output nodes and produce a common-mode voltage at the midpoint. This common-mode voltage is combined with the clock Φ_{amp} to turn off the dynamic amplifier.

IV. MEASUREMENT RESULTS

The prototype chip is fabricated in 28nm CMOS. A micrograph of the chip is shown in Fig. 4. The active area of

Fig. 4. Die micrograph of the proposed ADC.

Fig. 5. Measured DNL and INL.

the ADC is 0.017mm² (125μm×135μm). The measured total power consumption is 11.7mW at 1V supply and 4GS/s. The ADC power breakdown is as follows: the bootstrap switches consume 2.1mW, the voltage domain blocks, including the CDAC, comparator and residue amplifier, consume 4.4mW, the time domain blocks, including VTCs and TDCs, consume 5.2mW.

Fig. 5 shows the measured static performance. The DNL is within -0.38/+0.51LSB, and the INL is within -0.63/+0.52LSB. The mismatch introduced by the layout connections near the ends of the RO (p_4 , n_2 in Fig. 3) is shown in the INL around codes 10 and 118.

The measured output spectrum at 156.25MHz and 1.843GHz input frequencies are shown in Fig. 6. The ADC achieves 39.9dB SNDR and 47.8dB SFDR at Nyquist frequency, where the distortion is dominated by HD₃ and HD₅. The performance of the open loop RA ($\frac{g_m}{I_d}$) and the matching of the time-based circuit are both sensitive to process variations. Therefore, the gain error of the RA and the mismatch of the TDCs are calibrated to first order during the measurement, where a ramp signal fitting is applied to extract the coefficients.

The dynamic measurement results of the ADC are summarized in Fig. 7. The SNDR and SFDR stay above 42.1dB and 53.5dB respectively for input frequencies below 1GHz, leading to an FOM_W of 28.1fJ/conv-step. Above 1GHz, the SNDR and SFDR are mainly limited by the measurement setup and the quality of the differential input signal. Due to the amplitude and phase imbalance of the differential

Fig. 6. Measured output spectrum with 0dBFS signal applied at 156.25MHz and 1.843GHz respectively, sampling frequency is 4GS/s.

Fig. 7. Measured SNDR/SFDR and FOM_w versus input frequency.

signal, a severe input common-mode variation is present at high frequencies, which limits the linearity of the RA. The SNDR reduces to 39.9dB at Nyquist, leading to an FOM_w of 36.2fJ/conv-step.

Table I shows a performance summary and comparison with other single-channel ADCs of similar performance. Compared with these voltage domain and time domain ADCs, the presented ADC achieves the highest power efficiency thanks to the combination of the advantages in both the voltage and time domain techniques. Owing to the hybrid architecture, this ADC achieves the best FOM_w among all the single channel ADCs with a similar sampling rate (1GS/s–10GS/s) as can be seen in Fig. 8. Even compared with the time-interleaved ADCs [5], [10], this paper shows competitive performance while having a lower complexity and a smaller area.

V. CONCLUSION

This work introduces a simple and efficient single-channel hybrid voltage-time two-step ADC. It combines the high accuracy of the voltage domain technique and the high speed and high efficiency of the RO based TDCs. Moreover, due to the use of time domain conversion, it is robust to low voltage operation and technology scaling.

Fig. 8. Walden FOM comparison with state-of-the-art single-channel ADCs (f_{snyc} :1GHz–10GHz) presented at ISSCC and VLSI 2010-2019. Two TI ADCs with similar performance are also included.

TABLE I
COMPARISON WITH SINGLE-CHANNEL ADCs

	VLSI 2012 [7]	VLSI 2013 [8]	VLSI 2017 [4]	ISSCC 2014 [9]	This Work
Architecture	Flash	Flash	Time	Time	Voltage Time
Technology	40nm	32nm	40nm	65nm	28nm
Supply [V]	1.1	1.1	1.2	1.1	1
Resolution [b]	6	6	8	7	7
f_s [GS/s]	3	5	2	2.2	4
SNDR [dB]	33.1	30.9	40.7	37.4	39.9
Power [mW]	11.0	8.5	21	27.4	11.7
FOM_w [fJ/C]	99.3	59.4	119	210	36.2
FOM_s [dB]	144.4	145.6	150.6	143.3	152.2
DNL/INL [LSB]	NA/0.28	0.52/0.37	0.14/0.61	0.60/1.00	0.51/0.63
Area [mm^2]	0.021	0.03	0.08	0.052	0.017

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