Influence of the dielectric roughness on the performance of pentacene transistors

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The properties of the dielectric strongly influence the performance of organic thin-film transistors. In this letter, we show experimental results that quantify the influence of the roughness of the dielectric on the mobility of pentacene transistors and discuss the cause of it. We consider the movement of charge carriers out of the "roughness valleys" or across those valleys at the dielectric–semiconductor interface as the limiting step for the roughness-dependent mobility in the transistor channel. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1815042]

In the last decade, organic thin-film transistors (OTFTs) have improved rapidly. The achieved hole mobilities went up to 5 $cm^2/V\ s$ in the case of pentacene.[1] Major influences on the mobility have been the purification, deposition conditions of the organic semiconductor and the properties of the dielectric surface. Variations in the surface chemistry cause large changes in the mobility of the OTFT. In addition, several publications mention a reduction in mobility due to increased surface roughness.[2,3] In this letter, we show experimental results that quantify the influence of the roughness of the dielectric on the mobility and discuss its origin.

The challenge in investigating the effect of surface roughness on OTFTs is to generate different roughness variations of a dielectric without changing the other properties, such as surface chemistry, dielectric constant, and defect states, that can influence the growth and the charge transport of the organic semiconductor. Therefore, varying the deposition conditions of the dielectric or roughening the dielectric by ion sputter is out of question. Instead, we vary the roughness of an underlaying metal. Sputtering SiO_2 on top of this metal hardly smoothens the surface roughness. Note that there is an additional practical consequence to this observation for bottom-gate thin-film transistors, because if we use inorganic dielectrics, not only is the roughness of the dielectric important but also that of the underlying gate metal as well. In this respect, organic dielectric have the advantage of being better suited to "smoothen out" rough surfaces.

Top-contact pentacene transistors with 100 nm sputtered SiO_2 have been fabricated (Fig. 1). The gate consisted of a metal layer deposited on a Si substrate. The roughness of the gate metal is specific for the metal, the thickness of the metal, as well as the deposition recipe, and is given in Table I. It should be noted that for achieving different roughnesses of the metal layer, we randomly deposited metals under different conditions and in different deposition tools. The given values in Table I of root-mean-square (rms) roughness take only partly into account the structure of the roughness might differ, e.g., rectangular well or triangular well.

After the deposition of different gate metals with different roughnesses on different samples, all process steps that followed have been done for all samples in the same run. First, 100 nm SiO_2 was sputtered on top of the gate metals. Next, the surface of the SiO_2 was treated with an evaporated self-assembly monolayer (octadecyltrichlorosilane) followed by the deposition of 50 nm pentacene (flux ~0.25 Å/s, substrate temperature ~56 °C). As a reference, pentacene was grown on a sample of 100 nm thermal grown SiO_2 on a highly doped silicon wafer without gate metal, as well. Subsequently, 100 nm Au was evaporated through a shadow-mask to generate source–drain-contacts ($W/L = 2000\ \mu m/100\ \mu m$).

The electrical characteristics of the pentacene transistors have been measured in a N_2-glove box and the mobility was extracted from the saturation regime. The result of this experiment can be seen in Fig. 2. We have measured a gradual decrease in mobility with increasing roughness down to less than 2% of the mobility of pentacene on the smoothest surface. Additional information about the effect of the dielectric roughness on the film formation can be gained by looking at the atomic force microscope (AFM) images of the pentacene layer of the different samples (Fig. 3). Clearly, a reduction in grain size with increasing roughness can be seen. This can be attributed to a reduction of the diffusion length of the pentacene molecules, as well as a reduction of the energy barrier for nucleation during the formation of the nuclei.

There are basically three different effects, which can be found in literature, that may contribute to the lowering of the extracted mobility with increasing roughness. The first is related to an increasing amount of trap states.[4] The other two attribute the lowering of the charge-carrier mobility either to grain boundaries[5] or to surface scattering.[3,6–8] Pentacene grown on rougher substrates has a finer grain structure, hence a larger density of grain boundaries. If trap states are associated with grain boundaries, fine-grained pentacene will have

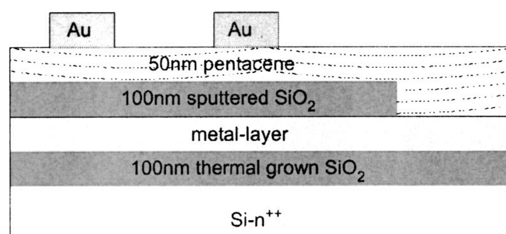

FIG. 1. Cross section of the device structure.

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TABLE I. Roughness values for 100 nm sputtered SiO_2 on different metals (all given roughness values are rms roughness values and determined for an AFM scan size of 5 $\mu m \times 5$ μm with 256 points per line).

Sample on Si substrate	rms of metal on substrate (Å)	rms of SiO_2 (Å)
Thermal SiO_2		1.7
15 nm TiW	3.4	2.4
30 nm Ni	11.8	7.6
50 nm TiW	10	10.5
200 nm TiW	28	17
100 nm TiW	66	56
150 nm TiW	105	92

a higher density of trap states. Alternatively, it may be suggested that on rougher surfaces the number of molecules in contact with the surface is larger. The molecules at the interface have shifted highest occupied molecular orbital and lowest unoccupied molecular orbital levels compared to molecules in the bulk phase, and can be responsible for a broadened density of states function. In both cases, however, we would expect a shift of the threshhold voltage V_T to more negative values with an increasing number of traps,[9] which is not the case according to Fig. 4. Furthermore, temperature-dependent measurements of two pentacene transistors with different roughnesses done by Knipp *et al.*[3] show nearly no change in activation energy between those samples but still a strongly reduced mobility on the rougher surface. We, therefore, do not favor models that attribute the apparent mobility reduction to increased trap densities.

The grain-boundary model[5] assumes that the transport through the grain boundaries is the limiting step for charge transport. The source–drain field drops over the grain boundaries and lowers the height of the barriers. If the number of boundaries increases, the same source–drain voltage drops over more grain boundaries and, therefore, the field-dependent lowering of the barrier is smaller. This effect might contribute to the roughness-dependent mobility for pentacene. It should be noted that a lowering of the mobility with increased roughness has been noticed for polymers, too,[10] where there are no grain boundaries.

Another contributor to the roughness-dependent field-effect mobility could be surface scattering. The effect of surface scattering on the mobility of a crystalline semiconductor, such as Si, GaAs, InP,[7,8] and even polycrystalline-Si

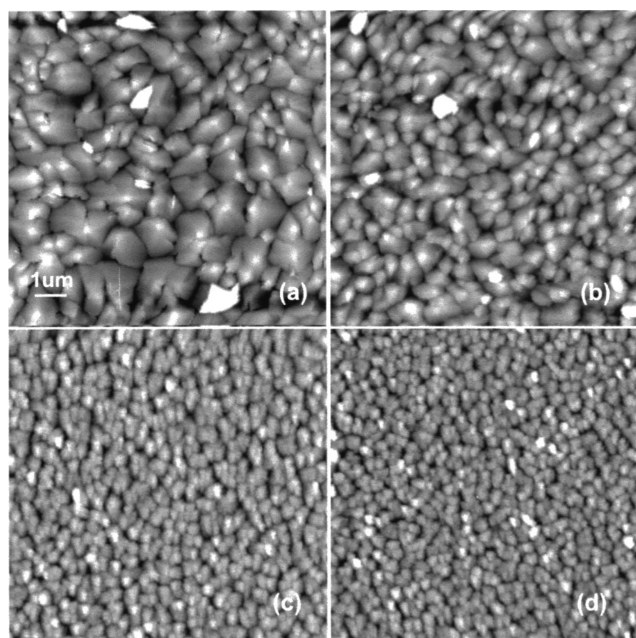

FIG. 3. Pentacene on SiO_2 surfaces with different roughness: (a) 1.7 Å, (b) 7.6 Å, (c) 54 Å, and (d) 92 Å.

(Ref. 6) has been intensively investigated, and is attributed to a scattering of the wave function of the charge carrier. However, in the case of organic semiconductors, the use of an extended wave function is not appropriate. Here, the transport is described as a movement of nearly small molecular polarons[11] with a mean-free path length of one molecular distance at room temperature. Because of this short mean-free path, the picture of drifting charges that bounce back from the roughness peaks cannot be valid.

A better explanation can be found, if we consider the holes located in roughness "valleys" at the dielectric. The source–drain field only supports drift movement along the surface and cannot support a charge movement out of the roughness valley away from the surface. In addition, in accumulation ($V_G < 0$ V), the gate field opposes any movement of charges away from the dielectric interface. The holes are "trapped" in the roughness minima and can only move out by diffusion or by drift along a local horizontal potential gradient caused by roughness variations.

In summary, we have presented results quantifying the effect of the surface roughness of the dielectric on the mobility of pentacene transistors and attributed this effect to the

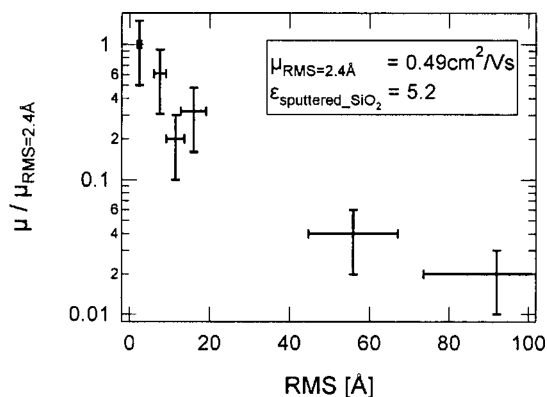

FIG. 2. Roughness vs mobility (normalized to the mobility of the smoothest surface).

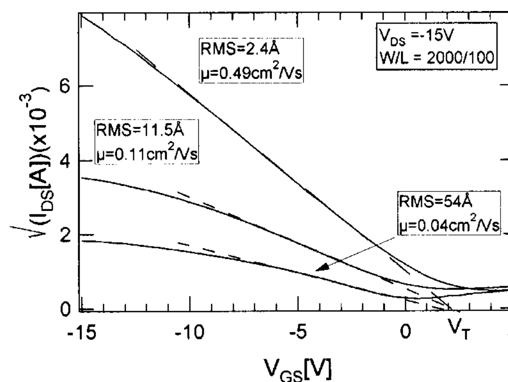

FIG. 4. Current–voltage (I_D–V_G) curve for different roughness values (W/L=2000/100, V_{DS}=−15 V).

hindering of the movement of charges by the roughness valleys. The experimental results show the significance of having a smooth dielectric as well as the importance to pay attention to the smoothness of the gate metal below.

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