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A Fully Integrated Switched-Capacitor Based AC-DC Converter for a 120 V_{RMS} Mains Interface

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Abstract—A fully integrated AC-DC power converter that faces a mains voltage of 120 V_{RMS} , 60 Hz is presented. The converter achieves an increased operating range and efficiency due to a switching capacitor which relies on the principles of charge redistribution and the memory effect. As such, the converter mimics a variable voltage division to bridge the voltage gap between the high mains and low DC-output. Customized AC-switches and a high-voltage capacitor ensure the high voltage capability. The AC-DC power converter is designed in a 0.35 μm -CMOS technology and achieves an output power of 15.16 μW at peak efficiency of 80.7 % on an active area of 9.8 mm^2 .

Index Terms—Fully integrated converter, AC-DC converter, switched capacitor, efficiency, power density

I. INTRODUCTION

POWER delivery through the AC-mains, a power source ranging from 100 to 240 V_{RMS} across our globe [1], is ideal for bunches of electronic applications. Due to the wide availability as well as the almost infinite capacity and low drop-out of the mains, it is a trustable power source for our electronic purposes. Large power converters often accompany our applications to transform the high mains voltage into a lower DC-output voltage, adjusted to the needs of the devices. Typically, these power converters are optimized for the active mode, like the heating-mode of a microwave. Unfortunately, the large efficiency drop of the AC-DC converters at low power levels (μW - to mW -range) forms a disadvantage of AC-mains powering [2]. As a result, electronic applications in standby or low power applications, like sensors, powered through these converters suffer large energy losses. Surveys state that the standby power consumption is about 5-10 % of the annual power consumption of a household [3]. A fully integrated converter optimized for the μW - and mW -range offers a solution for this problem. In addition, a monolithic converter results in a small and low cost solution which fits next to the existing converter to power the standby mode.

The main challenges of the proposed monolithic converter are situated in the voltage compatibility between the high mains input voltage and the low DC-output as well as the power density and efficiency. The first challenge is constrained by the CMOS components which typically tolerate voltages of a few volts. The density of the passive components will limit the power density of the converter.

As an alternative to the traditionally used bulky transformers, [4] uses an ESFI-SOS technology for the voltage compatibility. Unfortunately, this leads to an expensive solution. This work presents a converter implemented in a standard CMOS technology. A high voltage capacitor realized in this technology limits the voltage stress on the active components,

like in [5] and [6]. In contrast to the fixed voltage division converter in [5], the power density and efficiency are increased by a switching capacitor that mimics the effect of a variable voltage division. Compared to [6], the overall efficiency across the operating range, the load range for which the converter generates the desired voltage, is increased while the presented technique limits the output voltage independent of the load.

This paper is arranged as follows. Section II elaborates further on the challenges of monolithic high voltage conversion. The fundamental working principles of the proposed converter are discussed in section III, which is followed by a model of the converter in section IV. Section V gives more details about the implementation of the AC-DC converter facing 120 V_{RMS} , 60 Hz at transistor level. Measurement results and insights into a universal AC-DC converter are given in sections VI and VII respectively. Finally, a conclusion is drawn.

II. MONOLITHIC MAINS FACING AC-DC CONVERSION

AC-DC converters rated for mains input voltages and high loads in the W- to kW-range typically use transformers and rectifiers or a switched mode power supply combined with a high frequency transformer to bridge the gap between the mains and the voltages desired by an application [7]. Since the former components are expensive and of poor quality at the 50-60 Hz mains-frequency in a CMOS technology, integration of these techniques is not feasible. CMOS also holds another challenge for monolithic mains AC-DC converters: voltage compatibility, as integrated components often tolerate only a few volts. By adding extra circuit techniques, today's monolithic DC-DC converters tolerate input voltages up to 17 V [8]. Considering the mains of 100 to 240 V_{RMS} , it is clear that other circuit techniques are required to realize the voltage compatibility between the mains and CMOS technologies.

In order to limit the on-chip voltages, [5] implemented a capacitive voltage division. As shown in Fig. 1, the mains input voltage V_{AC} is capacitively divided by capacitors C_1 and C_2 into a lower voltage V_X . The ratio between C_1 and C_2 and the amplitude of the input voltage, determine the peak

Fig. 1: Capacitive division AC-DC voltage converter.

Fig. 2: V_X by capacitive voltage division and ideal V_X . Power is/is not transferred to the output during the green/red intervals.

voltage of V_X . C_1 holds a high voltage while only a small amount is left for C_2 and the other on-chip components.

Considering power converters, two main specifications are important. First of all, the power density, defined as the ratio between the output power P_{OUT} and the area A of the converter, should be as high as possible. Secondly, the efficiency η is kept high by limiting the power losses P_{LOSS} . In Fig. 1, P_{OUT} is mainly determined by the value of input capacitance C_1 and the conduction time of the bridge rectifier. This rectifier only transfers power to the output when V_X is larger than the DC-output voltage V_{DC} . Fig. 2 shows one period of V_X normalized to its peak value V_{MAX} for a converter operating at 60 Hz input frequency. Comparing this waveform to V_{DC} , it is clear that power can only be transferred during the green intervals. As a result, the delivered output power is limited and the output capacitor C_{OUT} should be high to restrict the output voltage ripple. The AC-DC converter in [6] increases the power density by approaching the square V_X -waveform in Fig. 2. This way, the bridge rectifier can transfer power from the mains to the output almost the whole period. Nonetheless, the efficiency is limited since the clipping of V_X introduces higher losses in the rectifier and a shunt path is needed to ensure the voltage compatibility for non-peak loads. Moreover, C_1 should be dimensioned for the fast transient, again over-stressing the rectifier with an efficiency loss as a result.

This paper presents a switched capacitor based converter for an input of 120 V_{RMS}, 60 Hz, which increases the conduction time of the rectifier compared to [5] so that the power density is boosted. The switching action ensures voltage compatibility across the whole load range. The converter aims for a peak output of 12.6 V. Additional output regulation can be achieved by an LDO for ripple reduction or by a SC DC-DC converter for lower output voltages, based on the 2-stage concept in [9], but is not needed for voltage limitation like in [6].

III. PROPOSED POWER CONVERTER AND OPERATION

A. The Fundamentals: Variable Voltage Division

Considering the aforementioned approaches, a long conduction time of the diode rectifier in the power converter is beneficial. This way, the output power increases while the ripple decreases for a fixed amount of input and output capacitance.

Fig. 3: V_X created by time dependent voltage division. Power is/is not transferred to the output during the green/red intervals.

This section presents an AC-DC converter for mains purposes which builds on the idea of a variable voltage division of the high AC-input $V_{AC}(t)$ and is conceptually illustrated in Fig. 3. When multiple voltage division factors $\alpha_1 \dots \alpha_4$ are available, the sine waves $V_1(t) \dots V_4(t)$ with amplitudes $A_1 \dots A_4$ in Fig. 3, can be generated from $V_{AC}(t)$:

$$V_i(t) = \alpha_i \cdot V_{AC}(t) = A_i \cdot \sin(\omega t), \text{ with } \alpha_i > \alpha_{i+1} \quad (1)$$

Correct combination of the different $V_i(t)$ results in the blue V_X -waveform of Fig. 3. Suppose that the on-chip voltage should be limited to V_{MAX} , V_X can follow $V_1(t)$ until V_{MAX} is reached and then gradually switches to $V_2(t)$, $V_3(t)$ and $V_4(t)$. As a result, V_X is constructed by dividing the AC-input voltage by a time dependent voltage division factor $\alpha(t)$: $V_X(t) = \alpha(t) \cdot V_{AC}(t)$. The green intervals in Fig. 3 show if the new V_X is larger than the output voltage V_{DC} . A bridge rectifier connected to this V_X will consequently conduct more power to the output compared to the fixed voltage division based AC-DC converter in [5]. In case that an infinite amount of voltage division factors is available, the blue V_X -waveform in Fig. 3 would become the square-wave in Fig. 2, so that the converter is always transferring power to the output.

B. Proposed AC-DC Converter

A resistive voltage division with a resistor bank for multiple division factors can implement previous model of ‘time dependent voltage division’ but results in a poor efficiency [8]. To increase the efficiency, a converter with capacitive division of the 120 V_{RMS} input ($V_{AC,P} - V_{AC,N}$) and one switching capacitor C_3 , shown in Fig. 4, is implemented. For a non conducting rectifier, the divided voltage $V_{XN} = (V_X - V_{AC,N})$ across the rectifier behaves as in (2) and (3) when capacitor C_3 is switched off and on respectively. $V_{OFS2}(t)$ and $V_{OFS2,3}(t)$ represent the offset voltages of the signals.

$$Off : V_{C2}(t) = V_{OFS2}(t) + \frac{C_1}{C_1 + C_2} \cdot V_{AC}(t) \quad (2)$$

$$On : V_{C2,3}(t) = V_{OFS2,3}(t) + \frac{C_1}{C_1 + C_2 + C_3} \cdot V_{AC}(t) \quad (3)$$

V_{XN} in Fig. 5 differs from V_X in Fig. 3. The reason for this distinction is situated in the 2 fundamental principles by

Fig. 4: Model of converter with variable capacitive division.

which the proposed converter operates: ‘charge redistribution’ and ‘memory effect’, as explained subsequently.

C. Charge Redistribution for AC-DC Conversion

The basic idea of ‘charge redistribution’ (CR) is illustrated in Fig. 6a for one period T of the input sine at 60 Hz. The green and blue waveforms are divided versions of the AC-input normalized to the maximum tolerable on-chip voltage V_{MAX} (4)-(6). The capacitors in Fig. 4 define the division factors of V_1 and V_2 . $V_{AC,MAX}$ is the amplitude of the input voltage.

$$V_1(t) = A_1 \cdot \sin(\omega t) = \frac{1}{V_{MAX}} \cdot \frac{C_1}{C_1 + C_2 + C_3} V_{AC}(t) \quad (4)$$

$$V_2(t) = A_2 \cdot \sin(\omega t) = \frac{1}{V_{MAX}} \cdot \frac{C_1}{C_1 + C_2} V_{AC}(t) \quad (5)$$

$$V_{MAX} = \frac{C_1}{C_1 + C_2 + C_3} V_{AC,MAX} \quad (6)$$

Starting at time $t=0$ in Fig. 6a, C_3 is disconnected and V_{XN} across the bridge rectifier follows V_2 . Once V_{MAX} is reached at t_1 , capacitor C_3 connects to C_2 so that the on-chip voltages stay limited. Here, ‘charge redistribution’ should be considered. Based on the principle of charge conservation, connecting multiple capacitors with a different voltage induces a charge transfer so that a DC-shift of the voltages on the capacitors takes place. Therefore, V_{XN} instantly evolves to the voltage V_{NEW} (7) while a voltage dip V_{DIP} (8) is visible.

$$V_{NEW} = \frac{\pm(C_1 + C_2) \cdot V_{MAX} + C_3 \cdot V_{OLD}}{C_1 + C_2 + C_3} \quad (7)$$

$$V_{DIP} = \frac{\pm C_3 \cdot V_{MAX} - C_3 \cdot V_{OLD}}{C_1 + C_2 + C_3} \quad (8)$$

Here, V_{OLD} is the voltage on C_3 before switching, which depends on the capacitor’s stored voltage at the disconnecting moment. In Fig. 6a, it is assumed that this event takes place when V_{XN} reaches 0. As a result, V_{XN} follows $V_1(t)$ from t_1 to t_2 and the offset in (2)-(3) is 0. The $\pm$ reflects the rising or falling of V_{XN} . From t_2 , V_{XN} follows V_2 until $-V_{MAX}$ is reached and CR takes place again. Considering a rectifier connected to V_{XN} , more power can be transferred to the output compared to a non-switching converter. Indeed, during the two peaks created by CR, the rectifier is on and delivers power to the load and output buffer capacitor C_{OUT} . During the dead-zones (red intervals) C_{OUT} provides the output power.

When multiple switchable capacitors are available, charge redistribution takes place multiple times each T , as shown by

Fig. 5: Signals of converter with switching capacitive division in 1 period. Green/red: conductive/non-conductive diode bridge. Blue: switching of C_3 .

the blue V_{XN} in Fig. 6b. Here, 8 division factors and as such $V_i(t)$ are created by 8 different switching capacitors. By charge redistribution, V_{XN} follows those $V_i(t)$ stepwise. Disconnection of all capacitors takes place at the 0-crossing of the input voltage. Suppose the number of switching capacitors increases to infinity, an infinite number of CR-steps takes place, leading to the red V_{XN} in Fig. 6b. As a result, a bridge rectifier connected to this V_{XN} could conduct for more than $T/2$ of the time and the output power can increase strongly.

D. Memory Effect as an Advantage

In Fig. 6b, there is still no power transfer possible in the intervals when V_{XN} follows V_1 , since V_{XN} is too low compared to the output V_{DC} and the rectifier is off. As such, a large buffer capacitor is required to bridge the idling time of the converter. This problem is solved when the memory effect of the switching capacitors is used as an advantage.

In the previous examples, the switching capacitor C_3 was supposed to turn off when the input reaches the zero-crossing. Considering the basic converter of Fig. 4, it is also possible to disconnect C_3 when a certain V_{MIN} is reached. The result is shown in Fig. 6c, where V_{MIN} is $0.5 \cdot V_{MAX}$. At t_1 , V_{XN} reaches V_{MIN} , C_3 disconnects from C_2 and it preserves the voltage of before the switching event. There is no charge transfer induced, which means that disconnecting C_3 changes the voltage division factor from the one in V_1 (4) to the one in V_2 (5), but does not create extra conduction peaks since V_{XN} does not jump back to V_2 , as was the case in Fig. 3. On the other hand, an offset is created, which explains the offsets in the final waveforms of the basic converter (2)-(3).

Despite the absence of a conduction peak at t_1 , $-V_{MAX}$ is reached faster and an extra peak appears at t_2 . Since the voltage dip at t_2 crosses the border of $-V_{MIN}$, C_3 disconnects again and another CR-event takes place at t_3 . As such, the offset of V_{XN} shifts stepwise to 0. Consequently, one capacitor with memory effect is sufficient to create the same number of conduction moments in V_{XN} as two CR-capacitors. In addition, the peak-moments are better spaced in time so that buffer capacitor C_{OUT} can be smaller, thereby increasing the maximum output power of the converter. To illustrate the advantage

Fig. 6: Illustration of the basic principles for switched capacitor based AC-DC conversion.

of the memory effect, table I shows the simulation results of the converter in Fig. 4 with following values: $C_1=10$ pF, $C_2=25$ pF, $C_3=98.2$ pF, $V_{AC,MAX}=80$ V and $V_{DC}=5$ V.

TABLE I
Memory Effect Changing the Output Power.

TEST CASE	P_{OUT}
Fixed capacitive division	P_{NOM}
Switched capacitive division, $V_{MIN} = 0$ V	$4.3 \cdot P_{NOM}$
Switched capacitive division, $V_{MIN} = 4.5$ V	$8.6 \cdot P_{NOM}$

For an infinite number of switching capacitors and the memory effect driven to the limit by $V_{MIN} \approx V_{MAX}$, V_{XN} results in the red square-wave of Fig. 6c. As the losses of the converter are not considered so far, there is an optimum for the number of switching capacitors, the ratio between the capacitors, V_{MIN} and therefore the number of extra peaks. One switching capacitor is chosen for the proposed converter, as this already gives multiple conduction peaks when V_{MIN} and the ratio between C_2 and C_3 are chosen correctly. Moreover, the area and control complexity decrease strongly compared to a converter with multiple switching capacitors. The resulting V_{XN} in Fig. 5 of the implemented converter shows 8 extra conduction peaks in T due to the explained principles. The choice of C_2 and C_3 determines the length of the non-conductive intervals [A,B] and [C,D] by the slop of $V_{C2}(t)$.

IV. CONVERTER MODELING AND DESIGN CHOICES

A. Converter Model

In order to determine the different parameters of the design in Fig. 4: C_1 , C_2 , C_3 , V_{MIN} and V_{MAX} , it is not only important to increase the conduction time as previously described, but it is also essential to evaluate the output power P_{OUT} , power losses P_{LOSS} and area of the converter to reach a high efficiency η and power density. Equations (9)-(12), which are averaged over period T of the input, define the converter's performance on condition of a constant output voltage V_{DC} .

Here, N represents the number of conduction moments in T and $I_{ON}(t)$ is the current transferred to the output when

the diode bridge is on during Δt_i . The average output current $I_{OUT,AVG}$ combines the different conduction moments. Due to the low operating frequency and μW operating range of the converter, its operation mode can be compared to the 'slow switching limit' in switched capacitor DC-DC converters [10], so that conduction losses are neglected. On the other hand, charge redistribution losses during switching contribute significantly to the converter losses (12). Finally, the diode rectifier delivers a loss contribution of $I_L \cdot V_D$ (= diode voltage drop). This loss was not considered during converter optimization, since it depends on the diode type and load current I_L and is independent of the design parameters. A transistor based rectifier avoids these losses but at the cost of driver circuits.

$$I_{ON}(t) \approx C_1 \frac{dV_{AC}(t)}{dt} \quad (9)$$

$$P_{OUT} = V_{DC} \cdot I_{OUT,AVG} = \frac{1}{T} \int_0^T V_{DC} \cdot I_{ON}(t) dt \quad (10)$$

$$= \frac{V_{DC}}{T} \sum_{i=1}^N \int_{\Delta t_i} I_{ON}(t) dt \quad (11)$$

$$P_{LOSS} = \frac{1}{T} \sum_{j=1}^{N-2} \frac{C_3(C_1 + C_2)(\pm V_{MAX} - V_{OLD,j})^2}{2 \cdot (C_1 + C_2 + C_3)} \quad (12)$$

Previous formulas hold if the load current is limited to the maximum load current the converter can deliver: $I_{L,MAX}$. During on-time, however, C_{OUT} and the load affect the slope of V_{XN} . As such, the peaks of V_{XN} created by capacitive switching become less sharp. Taking a DC-current, I_L , as load, a limitation for $I_{L,MAX}$ is calculated. For a conducting rectifier and disconnected C_3 , following expression applies to V_{XN} :

$$\frac{dV_{XN}(t)}{dt} = \frac{C_1}{C_1 + C_2 + C_{OUT}} \frac{dV_{AC}(t)}{dt} - \frac{I_L}{C_1 + C_2 + C_{OUT}} \quad (13)$$

Indeed, an increasing load I_L results in a decreased slope of V_{XN} . As a result, the proposed converter can only operate until the output current limits the rise of V_{XN} to V_{MAX} . For higher currents, the principles of 'charge redistribution' and 'memory effect' no longer hold and the output voltage will drop linearly under an increasing load current. At $I_{L,MAX}$, this means that

Fig. 7: Converter characterization curves for C_2/C_3 -ratio.

from the moment the rectifier conducts at t_{on} when the input is $V_{AC,ON}$, to the moment V_{AC} reaches its peak value at $T/4$, the integrated value of $d(V_{XN}(t))/dt$ becomes no larger than:

$$\int_{t_{on}}^{T/4} \frac{dV_{XN}(t)}{dt} dt \leq V_{MAX} - V_{DC} \quad (14)$$

Here, the diodes in the rectifier are assumed to have a negligible resistance and zero voltage drop. Integration of equation (13) for the same interval leads to:

$$\int_{t_{on}}^{T/4} \frac{dV_{XN}(t)}{dt} dt = \frac{C_1 \cdot (V_{AC,MAX} - V_{AC,ON})}{C_1 + C_2 + C_{OUT}} - \frac{I_L \cdot (T/4 - t_{on})}{C_1 + C_2 + C_{OUT}} \quad (15)$$

$$\Leftrightarrow I_L = \frac{C_1}{T/4 - t_{on}} (V_{AC,MAX} - V_{AC,ON}) - \frac{C_1 + C_2 + C_{OUT}}{T/4 - t_{on}} \int_{t_{on}}^{T/4} \frac{dV_{XN}(t)}{dt} dt \quad (16)$$

Taking (14) into account:

$$I_{L,MAX} = \frac{C_1}{T/4 - t_{on}} (V_{AC,MAX} - V_{AC,ON}) - \frac{(C_1 + C_2 + C_{OUT})(V_{MAX} - V_{DC})}{T/4 - t_{on}} \quad (17)$$

$$V_{OFS2}(t_{on}) \approx -V_{MAX} - \frac{C_1 \cdot V_{AC}(-\frac{T}{4})}{C_1 + C_2} = \frac{C_3 \cdot V_{MAX}}{C_1 + C_2} \quad (18)$$

Assuming that V_{MIN} lies close to V_{MAX} results in (18), so that t_{on} is solved by $V_{C2}(t_{on}) = V_{DC}$ (2), with $f=1/T$:

$$t_{on} = \frac{1}{2\pi f} \sin^{-1} \left(\frac{C_1 + C_2 - C_3}{C_1 + C_2 + C_3} - \frac{C_1 + C_2}{C_1} \cdot \frac{V_{MAX} - V_{DC}}{V_{AC,MAX}} \right) \quad (19)$$

$$\approx \frac{1}{2\pi f} \sin^{-1} \left(\frac{C_1 + C_2 - C_3}{C_1 + C_2 + C_3} \right) \quad (20)$$

An upper limit on $I_{L,MAX}$ is determined by neglecting the 2nd part of (17) and (19), which is correct under low ripple conditions. Although t_{on} depends on the ratio between the capacitors of the converter, it is possible to define 2 representative implementations that imply the same $I_{L,MAX}$ in (21). In the first case, C_3 is large and C_2 small, so that the slope when the rectifier turns off, is large (2). This means that non-conductive interval $[A,B]$ in Fig. 5 is bridged fast. t_{on} becomes $-T/4$ and $V_{AC,ON} = -V_{AC,MAX}$. In a more balanced

case, t_{on} is reached at 0, and $V_{AC,ON} = 0$. In other cases, t_{on} is computed by (20). Still, (21) gives good insights in the proposed design. Eq. (22) approximates the output power. Here, V_{DR} represents the voltage drop across the rectifier and the voltage loss caused by ripple on the output, which depends on C_{OUT} , I_L and the idling time of the converter.

$$I_{L,MAX} \approx 4fC_1 \cdot V_{AC,MAX} \quad (21)$$

$$P_{OUT,MAX} = V_{DC} \cdot I_{L,MAX} \approx (V_{MAX} - V_{DR}) \cdot 4fC_1 \cdot V_{AC,MAX} \quad (22)$$

B. Design Considerations

The maximum power that the proposed converter can deliver depends linearly on input capacitance C_1 , the maximum system voltage V_{MAX} and the frequency and amplitude of the input voltage. As the latter two are fixed, a large input capacitance and operating voltage are preferred. As explained subsequently, C_1 has a limited capacitance density due to the high input voltage and therefore limits the power density.

Like the efficiency of DC-DC converters benefits from a low voltage conversion step [11], so does the proposed converter by preferring a high V_{MAX} . This voltage is first of all limited by the maximum voltage the used components tolerate. Secondly, the density of the output capacitor drops with V_{MAX} . A $V_{MAX}=14$ V is chosen, which leads to a peak output of 12.6 V considering the rectifier's diode voltage drop.

For load currents smaller than $I_{L,MAX}$, the converter will operate as described in section III and (9)-(12), while the output voltage keeps regulated by V_{MAX} for the whole operating range. Based on the discussion of the 'memory effect', selecting V_{MIN} close to V_{MAX} increases the output power and decreases the voltage ripple since the non-conductive interval $[A,B]$ is shorter. The ratio between C_2 and C_3 is important for the number of conduction moments and t_{on} (20) and therefore influences the peak output power and operating efficiency, as shown in Fig. 7. Once C_1 and V_{MAX} are chosen, (6) fixes the sum C_3+C_2 . A low C_2/C_3 -ratio results in large voltage dips and an increment in the number of conduction moments N , and therefore an extension of the regulated output power range, as shown in blue in Fig. 7. Towards $I_{L,MAX}$ and so $P_{OUT,MAX}$, the CR-losses of (12) are constant or decrease slightly, as some of the switching events might disappear due to the reduced slope of V_{XN} (13). A large C_3 however, increases N such that the efficiency for a fixed load current drops, as shown by the black curves. Additionally, mismatch should be considered and so the ratio between C_2 and C_3 should not be too extreme. Based on previous trade-offs, the converter is designed with $C_1 = 50$ pF, $C_2 = 185$ pF and $C_3 = 370$ pF. For an input voltage $V_{AC,MAX} = 120\sqrt{2}$ at 60 Hz and a voltage loss towards V_{DC} of about 1 V, the theoretical maximum output load given by (17) is 1.73 μ A. Based on the trade-off between ripple reduction and power maximization, 2 nF is chosen for C_{OUT} (17).

V. CONVERTER IMPLEMENTATION

The presented converter is implemented in a 0.35 μ m-CMOS technology for an input voltage of 120 V_{RMS} , 60 Hz. This section describes the implementation details.

Fig. 10: Full system overview.

logic for driving S_{12} and S_{34} . A control loop, clocked by an external 20 kHz-clock, decides when capacitor C_3 should be connected to C_2 . The clock frequency is as low as possible to limit the losses of the drive circuit but is fast enough to decide on the result of a switching event of the capacitors. Two hysteresis comparators determine if V_X and $V_{AC,N}$ cross the boundaries of the predefined V_{MAX} - V_{MIN} interval. The resistive dividers in Fig. 10 divide V_X and $V_{AC,N}$ by six such that the inputs of the comparators fall between their supply rails. The ‘R-dividers’ are realized by series connection of six diode coupled transistors biased in subthreshold. This way, a high impedant divider is realized, which limits the power loss to a few pico-watts, while not causing a speed limitation. The capacitors filter the comparators’ kickback noise. A proper 1/6 voltage division is realized by matching of the parasitics in the divider. Based on the comparator outputs, the decoding logic decides whether $|V_{XN}|$ reaches V_{MAX} , which means that the voltage on C_2 is too high and C_3 should connect. Furthermore, the logic determines if $|V_{XN}|$ falls below V_{MIN} and decides C_3 can switch off. External DC-voltages V_H and V_{REF} set the reference and hysteresis width of the comparators and could also be realized by low power high ohmic dividers.

The controller is powered by an external 3 V-source. Considering the 2-stage approach in [9], a DC-DC converter can be added to the presented converter for regulation and to power applications at 3 or 3.3 V. This way, the controller supply can be connected to the output of the overall converter.

VI. CHIP MEASUREMENTS

The AC-DC converter with full-system overview of Fig. 10 is fabricated in a 0.35 μm -CMOS technology. The performance of the converter is measured for an input of 120 V_{RMS} , 60 Hz and is summarized in the first column of table II. The measured efficiency curve is presented in Fig. 11 and shows the converter operates from 0 to 1.6 μA at a peak output power of 15.16 μW and efficiency of 80.7%. This means that the converter not only generates the correct output for one load point, but that it operates over a wider range due to the switched capacitor

TABLE II
Comparison to State-of-the-art Monolithic AC-DC Converters

	This work	This work*	[5]	[6]	[8]**
Technology [μm]	0.35	0.35	0.13	0.35	0.35
Active area, A [mm^2]	9.8	9.8	3.5	6	7.7
P_{MAX} [μW]	15.16	14.27	1.5	6.4	$3 \cdot 10^3$
P_{MAX}/A [$\mu\text{W}/\text{mm}^2$]	1.55	1.46	0.43	1.06	390
η @ P_{MAX} [%]	80.7	84	59	70-75	2-3
V_{AVG} (V_{REG}) [V]	9.5	10.25	4	3.3	3.3
$VSOC$ [nF]	0.45	0.37	0.2	0.45	*
Max. Ripple Unreg. [%]	22.5	18.5	-	30.3	-
Max. Ripple Reg. [%]	-	-	5.76	4.54	6
P_{MAX}/C_M [W/F]	5819	5179	440	637	300

* 100 pF+50 pF SMD-capacitor, 110 V_{RMS} input

** not fully integrated, contains 10 μF SMD-capacitor

operation. The efficiency includes all converter losses as well as the DC-power consumption P_{DC} of the controller by measuring η as $P_{OUT}/(P_{IN} + P_{DC})$. Measurements confirmed the low cost realization of the controller, as it consumes less than 50 nW. Simulations show a breakdown of P_{DC} as follows: 19.21 nW for the comparators, 2.98 nW logic power, 2.02 nW is consumed by V_{EXT} and 24.44 nW by the clock buffers.

The simulated power loss breakdown in Table III confirms that the CR-losses dominate the design. The rectifier losses become more dominant at higher loads, while the operational and switch resistive losses are negligible. As discussed in section IV-B, the dominant CR-losses decrease with increased load, such that the efficiency rises in Fig. 12.

TABLE III
Power Loss Breakdown

Loss	Operational	CR	Resistive	Rectifier	Total
$I_L=300 \text{ nA}$	6.46 %	88.5 %	1.55 %	3.53 %	10.16 μW
$I_L=1.1 \mu\text{A}$	7.02 %	73.4 %	0.29 %	19.3 %	6.84 μW

Fig. 12 shows the measured voltages on nodes V_X , $V_{AC,N}$, V_{DC} and V_{XN} for a load current of 0.6 μA and an output power of 6.85 μW . The switched capacitor idea explained in section III is operational but the action is not fully symmetrical. Due to the asymmetry in the impedances at $V_{AC,P}$ (high) and $V_{AC,N}$ (low), both nodes couple unequally to the surroundings in the measurement setup. As such, the converter operates slightly asymmetrical with a lower average output power and voltage, since the asymmetry causes more ripple. Addition of a 100 pF SMD-capacitor between the negative terminal of the input source and $V_{AC,N}$ and 50 pF across C_1 , makes the circuit and the switching-operation symmetrical. The second column of table II shows the results of this adapted setup for a 110 V_{RMS} input. Because of the more symmetrical operation, the efficiency increased and a higher output voltage with lower ripple was obtained. These measurements show that the converter could be used with external components.

The performance of the fully integrated AC-DC converter (col. 1) is compared to the state-of-the-art integrated power

Fig. 11: Efficiency and output voltage vs. output power.

converters for AC-mains purposes operating at an input voltage of $120 V_{RMS}$, 60 Hz in table II. Comparison of the highlighted converters, shows that this work achieves the highest power density and as such operating range. Although this work has a larger area and little smaller $I_{L,MAX}$ than [6], it achieves the highest density thanks to the higher output voltage. In addition, the converter achieves the highest efficiency at peak output power and has equal performance based on the Voltage based Scaled Output Capacitance, $VSOC = V_{RIPPLE} \cdot C_{OUT} / V_{AVG}$. This means that all converters have a similar output ripple response for a fixed amount of output capacitance. This parameter gives a fair ripple comparison, as it takes C_{OUT} into account. Looking at the absolute ripple, this work performs worse, as there is no regulation. However, this value shows the peak % ripple, which decreases for lower loads as the outflow of stored energy on C_{OUT} depends on the load. Therefore, the average output voltage in Fig. 11 shows a gradient across the load range, which is larger than expected due to the asymmetry. An efficient SC DC-DC converter can be added to create a stable 3.3, 4.2 or 5 V output [9] or an LDO for ripple reduction of the current voltage.

The last column in table II shows an AC-DC converter, which uses an external $10 \mu F$ SMD capacitor that achieves a higher output power but lower efficiency. A fair comparison between all converters is made in the final row of the comparison table. Here, C_M includes all capacitors in the main part of the converter, including externals. Specifically, this work even as [5] and [6] produce a larger output power if all converters have the same amount C_M at their disposal. Thanks to the presented technique, this work even at a higher efficiency.

The intrinsic voltage limitation to V_{MAX} of the discussed converter holds a strong advantage to [6], shown in Fig. 11. In order to operate over a wide load range at confined intrinsic voltages, [6] sinks the unused power to ground while the AC-DC converter works in its peak power point. If this technique was used for the presented converter, the lowest efficiency curve in Fig. 11 would be measured. η' is calculated by (24), with P_{MAX} and η_{MAX} given by the values in table II. However, the switched capacitor division technique intrinsically limits the output voltage over the entire range while achieving an overall higher efficiency. Finally, Fig. 13 shows the chip micrograph of the monolithic converter that measures an active area of 9.8 mm^2 . The different capacitors are clearly visible.

$$\eta' = \frac{P_{OUT}}{P_{MAX} \cdot (1 + \eta_{MAX}^{-1}) - P_{OUT}} \quad (24)$$

Fig. 12: Measured voltage waveforms for $I_{LOAD} = 0.6 \mu A$.

VII. A UNIVERSAL AC-DC CONVERTER

A. Variable Input Voltage

The proposed power converter operates for an input voltage of $120 V_{RMS}$ at 60 Hz. Across the globe, the mains ranges from 100 to $240 V_{RMS}$ with a frequency of 50 or 60 Hz [1]. The implemented converter could be used for voltages lower than $120 V_{RMS}$ at the same V_{MAX} , as all components are rated for this voltage. Nevertheless, the efficiency and peak output power will decrease, as the converter is not working at its optimum. Namely, the V_{MAX} applied to the controller will defer from the V_{MAX} opposed by the capacitor sizes in (6), so that the too low main peak of V_{XN} cannot be used for power transfer. The efficiency of the converter rises by scaling V_{MAX} by (6), but $P_{OUT,MAX}$ still decreases quadratic with the input voltage (22). As such, another approach is needed when the proposed converter is used for different operating voltages.

Scaling of the capacitances in (6) to the applied $V_{AC,MAX}$ and V_{MAX} , demands a different implementation for each input voltage, which is economically not feasible. A more universal power converter is desired. As a first design strategy, it is proposed to keep V_{MAX} fixed at 14 V, while multiple switching capacitors make sure this 14 V is reached, depending on the input voltage. In this case, C_1 should be designed for the highest input voltage of $240 V_{RMS}$, which means that the capacitor plates in Fig. 8 should be spaced by $4 \mu m$. As a result, the capacitance density decreases by a factor 4.46. Combined with the area of an extra switching capacitor C_4 , so that (25) holds, the total converter area doubles. Nevertheless, for an input voltage of $240 V_{RMS}$, the output power doubles (22) such that the power density stays the one of table II. Consequently, the presented technique would achieve comparable results to [6] at $240 V_{RMS}$ at a higher overall efficiency, while C_1 is even over-designed relative to [5] - [6]. For optimal operation of the explained switched capacitor principles, it is possible to split C_4 into multiple capacitors. This way, the different available voltage division factors fit best for the applied input voltage.

$$V'_{MAX} = \frac{C_1}{C_1 + C_2 + C_3 + C_4} \cdot 240\sqrt{2} \quad (25)$$

Since the switching capacitors as well as the input capacitor are not used to their full potential for inputs smaller than

Fig. 13: Chip micrograph.

240 V_{RMS}, a second design approach is proposed: add an extra series division factor for input voltages higher than 120 V_{RMS} to the existing converter. By putting two C_1 capacitors in series, the component voltages stay limited to V_{MAX} while the capacitor in Fig. 8 can still be used due to the limited voltage. The power density of the converter will drop slightly but the capacitors are used efficiently for all input types. Depending on the input voltage, the added series capacitor can be put in parallel with either C_1 or the switching capacitors to increase the output power instead of leaving capacitors idling. This idea can be expanded to multiple input and switching capacitors to obtain the optimal division factor. This strategy increases the power density but demands a more complex control strategy while DC-biasing of the series capacitors is substantial.

B. mW-Output Power?

For the converter presented in this work, even as for the discussed state-of-the art fully integrated capacitive converters, the output power is limited to the μ W-range, mainly due to the low capacitance density and high impedance of the input capacitor, here C_1 . To reach the mW-range, the discussed converters could be scaled. For the presented work, up-scaling of the capacitors in the capacitive division part for an output power of 1 mW, results in a chip area of about 1.8cm x 1.8cm. This easily fits inside the existing bulky power converters to power the standby mode, as discussed in section I. A reduction of the converter area to about 1.1 cm x 1.1 cm can be achieved by soldering two external SMD-capacitors on top of the chip area that replace the on-chip C_1 and C_{OUT} , as shown in [15].

C. Influence of a Capacitive Converter on the Mains

While the diversity of electronic applications connected to the mains increases, the power quality is stressed more and more. As a result, standards like the one in [16], are introduced as a guideline to limit the influence of power systems on the mains. Typically, mains connected applications consume large amounts of reactive power, which can be compensated by ‘power factor correction’- techniques (PFC) to keep up with the power standards. As most loads have an inductive nature (motors, non-loaded transformers, ...), capacitors are often used to compensate the reactive power and let the load appear resistive. This work proposed an AC-DC power conversion technique based on capacitors, so that it even helps to correct the poor power factor created by the many existing inductive loads instead of deteriorating it.

VIII. CONCLUSION

This work showed the model and measurements of a fully integrated switched capacitor based AC-DC converter implemented in a 0.35 μ m-CMOS technology interfacing a high voltage of 120 V_{RMS}, 60 Hz. Thanks to the variable voltage division that leans on charge redistribution and the memory effect of capacitors, the conduction time of the converter is high while the voltages are confined. As a result, the presented converter achieves a better peak performance compared to the state-of-the-art monolithic power converters. Without any external component, a maximum output power of 15.16 μ W at 80.7% efficiency is achieved, while the efficiency across the whole load range is boosted. The influence of the different design parameters is shown, while the theoretical operation limit of the converter is explored. Addition of flexibility to the proposed circuit by more input and/or switching capacitors will result in an AC-DC converter for universal purposes.

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