Flip-chip joined 8X8 array of bottom - emitting 850 - nm light-emitting diodes for interconnect applications

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ABSTRACT

We present an array of GaAs-based light-emitting diodes emitting at 850 nm, which is designed to be flip-chip joined on carriers like a silicon CMOS circuit. The light-emitting diodes are grown by MBE. After processing of the array and flip-chip joining using Indium-bumps, the substrate of the LED array is removed completely. Individual light-emitting diodes reach an external quantum efficiency of 3.3% after the complete process.

1. INTRODUCTION

Light-emitting diodes compete with VCSELs as optical sources for optical interconnects. In favor of light-emitting diodes are their long lifetime, reliability, temperature stability, uncritical growth thickness and availability in large arrays. Moreover, when relatively small optical powers are sufficient, light-emitting diodes have better wall-plug efficiencies than VCSELs, because they operate without current threshold and reach efficiencies of up to 20%^{1,2}. Therefore, in applications where power consumption is critical and where modulation speed does not far exceed 1 GHz, light-emitting diodes are the appropriate light sources. Inter-chip interconnects is one of the applications where light-emitting diodes are competitive, because of the demanded large parallelism and low power consumption.

850 nm is becoming a standard wavelength for optical interconnects. This wavelength is, however, heavily absorbed in the GaAs substrate. This poses a problem for flip-chip joined light-emitting devices, since a flipped light-emitter necessarily emits through the backside. Therefore, after processing of the LED array and flip-chip joining, the substrate of the LED array has to be removed completely. The present paper shows whether and how this process affects the functioning of the LEDs.

2. LED ARRAY

Figure 1 shows the cross-section of one LED of the array. The layer structure is grown by Molecular Beam Epitaxy. The GaAs active layer is surrounded by AlGaAs cladding layers. The top cladding layer is p-type doped, the bottom cladding is n-type doped. In the top cladding layer, we foresee an $\text{Al}_{0.98}\text{Ga}_{0.02}\text{As}$ layer for lateral oxidation. The topmost layer of the LED is a heavily-doped p-type GaAs layer of 20 nm. Below the bottom cladding layer, there is an n-doped $\text{Al}_{0.05}\text{Ga}_{0.95}\text{As}$ layer of approximately 1 μm thick. This thickness is sufficient to provide a small series resistance to the LED; the Al

concentration guarantees that this layer is transparent for the light generated in the active layer. Under this layer we foresee an AlGaAs etch-stop layer.

Figure 1 also shows the processing of the LEDs. Mesas of 50 μm diameter are etched to close to the active layer. From the side of the mesas, the $\text{Al}_{0.98}\text{Ga}_{0.02}\text{As}$ layer is oxidized in wet nitrogen at 370 $^{\circ}\text{C}$ for 5 minutes³. The oxidation proceeds over a distance of about 10 μm . The open diameter of the LEDs hence is 30 μm . The cathode contact is AuGe/Ni/Au, deposited in a trench which is etched down to the n-AlGaAs contact layer and located at 28 μm from the mesa edge. It is alloyed at 380 $^{\circ}\text{C}$ for 30" in forming gas. The distance of the trench to the mesas plus the lateral oxidation distance is about 38 microns. This prevents non-radiative recombination from electrons and holes, and therefore improves the quantum efficiency at low currents. Figure 2 is a photograph of the top side of an LED, before the top contact is deposited. The oxidized aperture, the mesa and the bottom cathode plane (in a trench) can be seen. Subsequently, Ni/Au top anode contacts are evaporated on the mesas. It is not necessary to alloy these contacts, because of the high doping of the p-type top GaAs layer.

The pitch of the LEDs of the array is 150 μm . The LEDs are contacted individually by means of their anode contacts. The cathode plane is common to the array. The contacts for the cathode are mesas located at the periphery of the array. These cathode-contact mesas are identical to the LED mesas, except for the fact that an extra metal pad contacts the mesa top to the cathode plane.

The external quantum efficiency cannot be determined after processing and before flip-chip: the top side of each LED is covered by the top contact, and the substrate is not transparent.

Figure 1 Cross section of MBE-grown layer and processing.

3. FLIP-CHIP ASSEMBLY AND SUBSTRATE REMOVAL

Apart from the LEDs, a carrier is prepared on an undoped GaAs wafer coated with 200 nm of plasma SiO_2 . 200-nm thick gold pads and tracks are defined on this carrier by photolithography and lift-off. The tracks connect pads matching the anode and cathode mesas on the LED array to a set of outer contact pads for probing. The series resistance of the tracks is 150 to 300 Ohms, depending on their length. This should be reduced by depositing or plating thicker metal layers in the future.

The Indium bumps for flip-chip joining are fabricated on the anode and cathode mesas of the LED array, as shown in Fig. 3. A first resist is patterned by photolithography to have circular openings with a diameter of 40 μm on top of all mesas. Cr/Au is evaporated, but no lift-off is performed. Then, a second resist is spin-coated to a thickness of approximately 10 μm and patterned to have holes with a diameter 30 μm , concentric with the holes in the first resist. At the edge of the

wafer, this thicker resist is removed in acetone, to allow an electrical contact for the electroplating process. The wafer is then immersed in the plating bath (InCl_3/HCl),⁴ the pH of which was adjusted to 2.3. The current density during plating was 14 mA/cm^2 . Bumps with a total height of about 12 microns were obtained after 110 min plating. The bumps were reflowed in forming gas. After reflow, the bump height was about 10 micron.

To remove the oxides from the reflowed Indium bumps before the flip-chip assembly, the arrays were given a plasma treatment in SF_6 . The LED array was then flip-chip joined to the carrier at a temperature of 155°C to 180°C .

After flip-chip, the GaAs substrate was removed. First, the Indium-bumps and the carrier were protected by coating the periphery of the flip-chip-joined LED array and the carrier with varnish. Then, the flip-chip joined assembly was immersed in an $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2$ etchant, which removes the substrate and selectively stops on the AlGaAs etch-stop layer. The etch-stop layer was then stripped in $\text{HF}:\text{H}_2\text{O}$ (1:10). The varnish was removed in acetone, leaving the flip-chip assembly ready for tests and measurements.

Figure 2 Top view of an LED of the array, before the top anode contact metal is deposited. Lateral oxidation creates an effective LED diameter of about $30 \mu\text{m}$; the mesa has a diameter of $50 \mu\text{m}$; the bottom cathode contact is deposited in a trench at $28 \mu\text{m}$ from the edge of the mesa.

Figure 3 Cross-section of the LED array for Indium plating. Cr/Au metallization is used for electrical contacting of all holes to be plated. After plating, it is removed by lift-off in acetone.

4. MEASUREMENTS

Figure 4 shows the current-voltage characteristics of the LED array after Indium-plating, SF₆-plasma treatment, and flip-chip. The series resistance is determined by the series resistance of the carrier, as explained above, and will be overcome by using thicker metal on the carrier. Indium plating had no adverse effect on the ideality factor of the diode.

On Figure 5, we compare the current-voltage characteristics of an LED before and after substrate removal. The apparent decrease of the series resistance after substrate removal is attributed to the fact that we did not use exactly the same diode of the array for the measurement. The measurement allows to conclude that removal of the substrate does not increase the series resistance noticeably.

Figure 6 shows the light output characteristics of the flip-chip joined LEDs after substrate removal. Shown are, versus driving current: the light output in Watt, the absolute quantum efficiency, defined as the ratio of the optical output power (W) to the product of the current (A) and the bandgap energy (eV), and the differential quantum efficiency. The maximum quantum efficiency is 3.2%, and the maximum differential quantum efficiency is 3.3%.

Very importantly, it can be seen from Fig. 6 that the absolute quantum efficiency reaches the value of 1% for currents as small as 7 μ A. This is achieved by the effective surface passivation due to the lateral oxidation and the distance between the mesa and the trench. Achieving high efficiencies at low current levels is very important in applications such as parallel optical interconnects. Indeed, in such application, one sends on-off modulated light pulses which have to be detected and converted to electrical digital signals. The total electrical power necessary for detection of a digital light signal is typically about -40 dbm to -30 dbm. These optical power levels are achieved at currents of 35 to 250 μ A and at a driving voltage of 1.22 to 1.5 V in Fig. 6. The electrical power consumption at the light-emitter side is therefore limited to 43 μ W to 375 μ W.

Figure 4 Current-voltage characteristics of diode after Indium-bumping, reflow, SF₆-plasma treatment, and Flip-Chip joining, but before substrate removal. The series resistance is due to the resistance of the lines on the carrier.

Figure 5 Linear current-voltage characteristics before and after GaAs-substrate removal of flip-chip joined diodes. The series resistance is limited in both cases by the carrier, and no increase can be seen due to the removal of the GaAs substrate.

Figure 6 Optical characteristics of an LED of the flip-chip bonded array, after removal of the substrate. Full Line: Optical output power versus LED current. Closed Dots: Absolute external quantum efficiency. Open Dots: Differential external quantum efficiency. The maximum is 3.3%.

It should be noted that the efficiency of the LEDs could still dramatically be improved by roughening the light-outcoupling surface. Indeed, the LEDs presented in this work are thin-film devices sandwiched between a metal mirror and a semiconductor-air interface. It is sufficient to roughen this latter interface in order to generate a non-resonant cavity¹, which typically enhances the output efficiency by at least a factor of 2.⁵ Alternatively, the LED could be designed to be a microcavity², which would also strongly enhance its external quantum efficiency.

5. CONCLUSIONS

We present an array of LEDs, emitting at 850 nm, which is flip-chip joined on a carrier. The pitch of the LEDs is 150 μm , the individual LEDs have a mesa of 50 μm , and lateral oxidation further reduces this to an effective diameter of 30 μm . Flip-chip using Indium balls is used. After flip-chip, the substrate of the GaAs wafer is removed completely. After substrate removal, the maximum quantum efficiency was 3.3%. For all currents larger than 7 μA , the absolute external quantum efficiency is more than 1%. The size, density and wall-plug efficiency of the diodes at low currents allows short-distance optical interconnects with such array.

ACKNOWLEDGMENTS

The authors thank W. Van de Graaf for the MBE-growth of the samples, S. Peeters for help with the processing of the LED arrays, and M. Van De Peer for help with the flip-chip bonder. R. Windisch acknowledges the EC for his TMR grant No. ERBFMICT972046. This work was in part supported by the EC under contract No. 22641 (OIIC).

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