CMOS Receiver Array with 100 channels on 1 mm² chip area based on Self-Calibrating Self-Regenerative Sense-Amplifiers Operating at 200 Mbit/s/channel

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ABSTRACT

Parallel optical interconnects may become the communication method of choice to achieve future high bandwidth data transfer between chips or MCM's. For this purpose, an integrated CMOS detector approach is favorable at the light-reception side, so Flip-chip of detectors is no longer required. In this paper we present an integrated differential CMOS detector layout which gives a flat frequency response of 0.1A/W with a -3dB bit rate over 450Mbit/s/ch (wavelength of 860nm) in standard 0.6μ technology. The detector works following the Spatially Modulated Light detector (SML-detector) principle. Based on this SML-detector we fabricated a dense detector/receiver array consisting of 100 channels on one square mm Si area in 0.6μ standard CMOS. The detector area is 50x50μ². The detector signal is amplified and latched by a self-regenerative sense-amplifier, which is self-calibrating for increased array homogeneity and receiver yield. The power consumption per receiver channel is as low as 1.1mW and the received light power at 200Mbit/s is 25.1μW (at a BER<1e⁻¹²). Measured standard deviation on the output jitter is 96ps and the measured worst case channel to channel output delay variation is 200ps. Future CMOS technology will improve the maximum detector/receiver bit-rate as well as the attainable sensitivity.

Keywords: CMOS, detector, optical receiver

1. INTRODUCTION

Electrical interconnections between chips suffer nowadays from lack of aggregate bandwidth, electromagnetic interference (EMI), electromagnetic compatibility (EMC), ESD problems and too high power dissipation. Connecting chips with optical channels may possibly alleviate most of these problems. However, in an optical interconnect solution, the light emitters, the optical pathway and the receiver system will pose other problems.

In this paper we demonstrate that dense parallel *optical receivers*, operating at a respectable bit rate (200 Mbit/s), and at low power dissipation can already be conceived in a standard 0.6 μm CMOS technology. The optical sensitivity is for this purpose somewhat less important than for long distance interconnects. More important are however the array homogeneity, robustness and yield of the system. A requirement is also that uncoded data (including DC) can be transmitted. Coding and decoding cannot be tolerated in most digital systems since they induce extra latency. For cost and reliability reasons, we chose to work with receivers with integrated detectors being fully compatible with the standard CMOS process. The receivers are of the clocked type, allowing fast restoration to digital signal levels inside the chip. In large synchronous systems we expect to have a clock signal available everywhere. Clocked receivers dissipate only of the order of a flip-flop, much less than a traditional trans-impedance amplifier.

2. THE INTEGRATED CMOS DETECTOR

For achieving light detection with a flat frequency response, we use the Spatially Modulated Light (SML-) detector [1] shown in Fig. 1.

Figure 1. Detector cross-section

Fingers of photo-diodes are alternating open for incident light and covered with floating metal2 (reflective). All open fingers are grouped into a so-called *Immediate* (I) detector part and the covered ones into a *Deferred* (D) detector part. Incident light penetrates the substrate, 10-20 microns deep (for $\lambda = 860$ nm), whilst the available CMOS junctions are shallow. Photo-generated carriers (in the shallow zone I) arrive quasi instantaneously at the *Immediate* detector fingers. Carriers generated in zone II arrive preferentially at the *Immediate*, but also at the *Deferred* detector fingers by diffusion. Zone III carriers arrive equally at the *Immediate* and *Deferred* detector fingers. Versus time, zone I carriers arrive earliest, zone II carriers arrive a little later, and zone III carriers, if they arrive, are the slowest. Figure 2 and 3 shows respectively the measured frequency and temporal response of the two detector parts, the sum and the difference. The sum curve reflects a typical CMOS detector response exhibiting “lower frequency gain”. The difference (I-D) is the useful signal, since it is flat up to bit rates of more than 450 Mbit/s. In summary, by subtracting the *Deferred* signal from the *Immediate* signal we obtain a useful signal containing only the “fast” arriving carriers. In this way the detector bandwidth is increased to a large extent.

Figure 2. Frequency Response of the two detector parts (I and D), their sum and their difference.

Figure 3. Temporal Response of the two detector parts (I and D), their sum and their difference

The measured responsivity is 0.1 A/W in the used technology for a finger pitch of 8 μm and $\lambda = 860 \text{ nm}$. Both detector parts have a capacitance of 92 fF each (@ 3V) for an overall area of 50 x 50 μm^2 . For light with a shorter wavelength, the penetration depth is shorter and a much higher bit rate can be achieved together with improved responsivity. Besides that the detector is a fully CMOS detector, another issue to be appreciated is that we have constructed a *differential* detector, allowing *fully* differential signal processing at the sensitive start, i.e. at the detector itself. This improves power supply rejection and minimizes effects due to substrate currents. Moreover, two or more of these detectors in the same substrate exhibit (understandably) low cross talk, if the space between them is at least three times the fingers pitch. Low cross-talk is crucial for the array operation envisaged in this paper.

3. THE SELF-CALIBRATED RECEIVER

Figure 4 shows the full receiver circuit, as it is combined with the detector on a square of 100 x 100 μm^2 area, and repeated 100 times. When the clock is HIGH, nodes Q and QN are forced in an equilibrium state. When subsequently the clock goes LOW, M1..M4 go into a meta-stable phase. The current difference arriving through cascode transistors M5 and M6 determines meanwhile the switching direction. If light is incident, Q goes high and with no light incident, the threshold current $I_{\text{threshold}}$ brings Q to go Low. The latter current should be biased at about half the expected detector current. Cascode bias current I_b keeps the detector node frequencies at 125 MHz (enough for 200 Mbit/s NRZ operation). Cascode transistors M5 and M6 work somewhat amplifying (their drain nodes having much lower capacitance than the detector nodes) and they also protect the detector parts during reset from *charge kickback*. M9..M12 keep the most recent state latched, followed by two buffering inverters.

Figure 4. Receiver circuit

Different from other receiver designs is that the space for layout of the receiver cell is limited. This requires extra attention to limit the effect of the variation on transistor parameters in transistor pairs. Current sources M7 and M8 are therefore degenerated. Mismatch between Cascodes (M5-M6) results in a small detector bias mismatch, not harming the operation.

Finally for the hart of the self-regenerative sense-amplifier (M1-M4), we chose a self-calibration principle.

Figure 5. Sense-Amplifier body with self-calibration (a), and without (b).

The more conventional method is to use a set up like in Fig 5.b whereby the voltages on the switching nodes are pulled towards each other during the reset phase. When e.g. the two transistors in the PMOS pair are non-matching, the obtained equilibrium is not reached by this pulling action. After the reset transient -the clock signal still being HIGH- a current through resetting transistor M11 will remain flowing. Making the clock signal LOW will induce a *preferred switching* direction. Such a preferred switching direction can be referred to the input as an offset voltage. The self-calibration option in Fig. 5.a uses two resetting transistors (M5 and M6) in order to reset -when clk is HIGH- to the *real equilibrium*. At this real equilibrium, the voltages at the switching nodes are allowed to be different, incorporating mismatches in pairs of transistors. At the end of the reset transient, M5 and M6 do not conduct current and can as well be turned off, leaving M1..M4 in the meta stable state *without a preferred switching direction*.

Figure 6. Effect of mismatch to the input offset

The simulation of Fig. 6 shows an improvement in input referred offset between a factor 4 and 5 (for threshold voltage mismatches in the p-transistor pair M3 & M4; and M9 & M10 in Fig. 5). Due to second order effects, the improvement is not unlimited. It can be proved that the reduced sensitivity to mismatches also holds for other transistor parameters.

In summary, the transistor pairs in the sensitive part of the receiver either have reduced mismatches, or the effects from mismatches have been reduced. This is necessary for uniform array operation and DC data transmission.

4. MEASUREMENTS

4.1 Single Channel operation

A typical evaluation tool for receivers is an analog EYE-diagram. For a synchronous receiver of this type, it is however not possible to measure the eye since there is no place in the receiver where the analog signal is available. Only a direct plot of the Bit Error Rate (BER) gives proof of the good operation of the receiver. Figure 7 was measured at 200 Mbit/s with a V_{dd} of 3.4 V. The current used per receiver (at speed) is 320 μ A. To measure this, the output was disconnected, in order not to measure the high output current driving the coax. Total array current (for 100 receivers) is thus 32 mA. Per channel, 1.1 mW is dissipated.

A Pseudo Random Bit Stream (PRBS of $2^{15}-1$) was used for the evaluation of the receiver, thereby using the HP 82100 data generator/analyzer platform. Figure 7 shows the Bit Error Rate versus the light input power. For every measured point the setting of $I_{threshold}$ was optimized. As expected, best BER was obtained by biasing this current at half the photocurrent, keeping the threshold level in the middle. The cascode current I_b was fixed at 8 μ A.

Figure 7. Bit error rate plot

To reach the BER of 10^{-12} an average light input power of $25 \mu\text{W}$ (-16 dBm) was required. For inter chip communication this optical power level can easily be obtained at the receiver side. A better BER can be required, like for electrical interconnects without error correction method. More light gives a better BER but takes very long times to measure accurately.

Figure 8. Digital output Eye-diagram (@ 200 Mb/s)

An eye-diagram of the digital output is shown in Fig 8. The digital output was connected to a coax cable using a series resistance of several hundreds of ohms, allowing high frequency probing at a reduced voltage level. An on chip multiplexer allowed selection of every channel of the hundred channels. The jitter at the digital output is low enough to allow connected digital circuits on chip to use the data without any extra synchronization stage. With too little light input, meta stable failures were recognized on this digital eye-diagram.

4.2. Multiple channel operation

All 100 channels in the array operated in the same way. To get a more quantitative measure, we measured carefully the spread on the sensitivity (at BER of 10^{-11}) for 25 elements. From the other 75 receivers it was checked that the sensitivity was at least below $25.5 \mu\text{W}$ Figure 9 shows the result.

Figure 9. Spread on the sensitivity

The worst-case measured channel-to-channel output delay variation was only 200 ps, confirming that enough uniformity in timing is obtained for parallel array operation. Figure 10 shows the photograph of part of the array. The X and Y pitch is 100 μm.

5. OTHER ARRAY DESIGN CONSIDERATIONS

During the measurements, all receivers were operating in parallel with the same clock signal. However, only one light input was available. Another test has to be done with multiple random-data light inputs, to check whether electrical cross talk is low enough. From DRAM sense amplifiers it is known that operating many regenerative sense-amplifiers in parallel is a good practice, even when they are placed on a very small pitch (much less than 100 micron). Electrical cross talk between channels should thus not be a problem. If this is checked, we can state to receive at an aggregate bitrate of 20 Gbit/s/mm².

Another issue is to choose the level of the threshold current. Conventional telecom receivers generate the threshold level by low-pass filtering the photo current signal (or one of its derived signals), or by AC-detector coupling. These methods lead however to bit errors at the moment that DC-data (many consecutive ONEs or consecutive ZEROs) are transmitted. For *uncoded* communication between chips, DC-data transmission should be supported. Therefore, in array operation we propose to use (and sacrifice) at least one channel to generate this reference current. A permanent ONE or a permanent oscillating signal can be transmitted through this channel. The received photocurrent can then be used to generate the required threshold current for the other receivers in the array. Common mode fluctuations in light emitter efficiency (e.g. due to ageing), optical pathway efficiency (e.g. distance between chips), etc. will then automatically be taken into account.

Figure 10. Photograph of part of the array

6. CONCLUSIONS

In standard CMOS, optical receivers for optical interconnects between chips can be conceived operating at typical PC bus rates with footprints as small as a single bonding pad and consuming only 1.1 mW /channel. At the receiver side aggregate bit rates of 20 GBit/s per 1 mm² CMOS area become feasible already in 0.6 μ m CMOS technology. Sufficient array homogeneity in sensitivity and output delay has been demonstrated.

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