7.4 Robust Digital Design in Organic Electronics by Dual-Gate Technology

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Research towards organic RFID tags is one of the drivers of organic electronics. In recent years, 64b organic RFID tags have been shown with capacitive coupling [1] and inductive coupling at 13.56 MHz [2,3]. Recent improvements were a 128b organic transponder chip with basic anti-collision and Manchester encoding [4] and a first 4b tag in complementary organic technology [5].

As clear from above, the most widespread technology is still single- V_T p-type only, with intrinsic limitations concerning integration of larger circuits, as a result of parameter variability. The move towards an organic complementary technology [5,6] is a possible solution, but it requires the existence of robust n-type organic semiconductors, still very scarce. In this work, we present a technologically much less complex route to improve the robustness of organic circuits. It is based on p-type transistors only, equipped with a double gate [7,8,9]. One gate is used to vary the V_T , which leads straightforwardly to a dual- V_T p-type technology. Furthermore, as V_T is now not fixed by technology but controlled by a gate, the dual-gate transistor configuration allows to innovate the architecture of basic blocks as inverters. We show inverter topologies with substantially increased gain and noise margin. Finally, we demonstrate a 64b organic RFID transponder chip based on these dual-gate OTFTs for two different inverter topologies.

The organic TFT technology that is used was developed by Polymer Vision for the commercialization in rollable active matrix displays and is described elsewhere [10]. The organic insulator layers and the p-type pentacene semiconductor are processed from solution. The transistors have a typical channel length of 5 μm and an average saturation mobility of 0.15 cm^2/Vs . The top gate is coupled weaker to the channel than the bottom gate, and we therefore use it as V_T -control gate.

Two main architectures can be used for inverters and other logic gates in unipolar technologies, namely zero-vgs-load (or depletion-load) and diode-load (or enhancement-load). We investigate both architectures for a technology where both the load and drive transistors have a dual-gate. The schemes are depicted Figs. 7.4.1 and 7.4.2. The V_T -control gate is denoted with the subscript 'top'. The ratio between the drive and load transistor for the diode-load logic is 10:1, however we have found that the zero-vgs-load logic can be designed ratioless resulting in a significantly smaller chip area. Figures 7.4.1 and 7.4.2 depict contour-plots of noise margin and trip point when varying the V_T -control gate voltage of the drive and load transistor for both inverter topologies. As can be seen, noise margins can exceed 2.8V for zero-vgs-load inverters and 0.7V for diode-load inverters at $V_{DD}=20\text{V}$. The trip point can be shifted towards $V_{DD}/2$ (i.e. 10V) for both designs by appropriate V_T control.

The architecture of the inverter is optimized when connecting $V_{top,L}$ with the output node. This topology – to our knowledge never shown before – leads to increased noise margin and gain. The transfer curves of zero-vgs-load and diode-load inverters using this optimized topology are depicted in Fig. 7.4.3. The V_T -control gate of the drive transistor can be used to move the trip point towards $V_{DD}/2$. At this point, in zero-vgs-load inverters, the gain exceeds 11 and the noise margin is larger than 6V at $V_{DD}=20\text{V}$. Importantly, the typically low gain of diode-load inverters increases to 2.

In literature, circuits having an integration level larger than inverters have so far not been shown for dual-gate OTFT circuits. We made 99-stage dual-gate ring oscillators with zero-vgs-load and diode-load architectures. In Fig. 7.4.4, we show the extracted stage delays of NAND-gates and inverters, for optimized inverter topologies, and compare them to reference single-gate zero-vgs-load

gates fabricated on the same foil. The fastest family is the optimized diode-load topology, with a stage delay of 2.27 μs . The optimized zero-vgs-load topology is an order of magnitude slower ($\tau_{\text{stage}}=26\mu\text{s}$), due to the high parasitic output-capacitance. This capacitance is also present in the single-gate depletion-load architecture but the drive-transistor current is now higher, resulting in a smaller stage delay.

Next, we fabricated 64b RFID transponder chips similar to earlier designs [2], but with a clock from a 33-stage ring oscillator to prevent racing of the signal. The ratio between drive and load transistor is 10:1 leading to a chip area of 74.48 mm^2 . Figure 7.4.5 shows the output signal of the chip designed in optimized diode-load topology for $V_{DD}=20\text{V}$ and $V_{top,D}=45\text{V}$. The data rate is 4.3kb/s, more than double the fastest transponder chips shown in [4]. We verified on three different foils that some chips start operating at V_{DD} as low as 10V and all chips work at 15V.

The 64b transponder chip in optimized zero-vgs-load topology is only 45.38 mm^2 in size, thanks to this logic being ratioless. In Fig. 7.4.6, the output is shown for $V_{DD}=20\text{V}$ and $V_{top,D}=30\text{V}$. Also this transponder chip has been measured on three different foils. All measured transponder chips are operational at $V_{DD}=10\text{V}$. The data rate at $V_{DD}=20\text{V}$ is 522 b/s. These findings are fully in line with the fact that the zero-vgs topology has higher noise margin but slower stage delay than the diode-load topology. Figure 7.4.7 shows a photograph of both 64b transponder chips.

The top-gate voltage of the drive transistors are relatively high, 30 to 45V. In an organic RFID transponder, such high voltage cannot be generated by a rectifier. However, it can be generated by charge pumps, provided that the required current is limited. To verify whether that last assumption is realistic, we have operated the chips with a 1-nA current compliance for the voltage supply of the top gate of the driver transistor. All chips were fully operational after a delay to charge all top gates. This delay was about 2.09s for the diode-load configuration and only 246ms for the zero-vgs-load configuration. The difference is due to the fact that the drive transistor is 10x larger for the diode-load (ratioed) than the zero-vgs-load configuration. We conclude that charge pumps are a viable route to charge the top gates of the logic blocks of the proposed dual- V_T technology.

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Figure 7.4.1: Architecture of a dual-gate zero-vgs-load inverter (left). Contourplots of the trip point (middle) and the noise margin (right) determined from measured transfer curves of inverters when varying the top-gate voltage of the load and drive transistor and applying a supply voltage of 20V.

Figure 7.4.2: Architecture of a dual-gate diode-load inverter (left). Contour plots of the trip point (middle) and the noise margin (right) from measured transfer curves of inverters when varying the top-gate voltage of the load and drive transistor and applying a supply voltage of 20V.

Figure 7.4.3: Architecture of optimized inverter architectures in dual gate technology for (top) zero-vgs-load inverter and (bottom) diode-load inverter. Transfer curves of these inverters are plotted to the right for a supply voltage of 20V, as a function of the voltage on the V_T-control gate of the drive transistor.

Figure 7.4.4: The stage delay is plotted as a function of the V_T-control voltage of the drive transistor for optimized zero-vgs-load and diode-load inverters for a supply voltage of 20V. The stage delay of a single-gate zero-vgs-load inverter is shown for reference, also for a supply voltage of 20V.

Figure 7.4.5: The output signal of a 64b organic RFID transponder chip with optimized diode-load configuration for a supply voltage of 20V and a top-gate voltage of 45V. The corresponding data rate is 4.3kb/s.

Figure 7.4.6: The output signal of a 64b organic RFID transponder chip with optimized zero-vgs-load configuration for a supply voltage of 20V and a top-gate voltage of 30V. The corresponding data rate is 522b/s.

Figure 7.4.7: Photograph of the 64b organic RFID transponder chip designed with optimized zeroVgs-load configuration (left) and optimized diode-load configuration (right).