12.3 Memory Solutions for Flexible Thin-Film Logic: up to 8kb, >105.9kb/s LPROM and SRAM with Integrated Timing Generation Meeting the ISO NFC Standard

Florian De Roose^{1,2}, Jan Genoe^{1,2}, Auke J. Kronemeijer³, Kris Myny², Wim Dehaene^{1,2}

¹KU Leuven, Heverlee, Belgium

²imec, Heverlee, Belgium

³Holst Centre/TNO, Eindhoven, The Netherlands

Thin-film transistor (TFT) technologies have long been used predominantly for display fabrication and are attractive for large area, low cost and flexible circuit applications. Thanks to the improving performance of thin-film metal-oxide NFC tags and data processing chips on foil [1,2], fabs are considering the large-scale production of flexible logic circuits. However, these systems require a memory, but metal-oxide technology lacks reliable, large memory arrays. Today, data storage is limited to ROMs, flipflops and SRAMs. No memory array has been demonstrated with sufficient storage capacity and speed within the typical power and area budget. This paper demonstrates the first large, fast and low-power memory array in flexible metal-oxide technology, comparable to the Si Intel 4000 series in the seventies [3].

One of the most demanding TFT applications today is an NFC tag according to the ISO14443 standard. Sending NDEF messages requires at least 1kb of memory at a rate of 105.9kb/s. However, no metal-oxide-based memory of this size has been shown before. Another hot topic for thin-film circuits is computation, e.g. implementing encryption. Even the most lightweight encryption algorithms require a rewritable memory bank and a large one-time-programmable memory for storing the key. The largest rewritable memory banks shown are a 4x8b register bank [2] and a 128b SRAM [4]. The largest ROM memory is 144 bits [2]. To enable encryption on foil, larger and faster memories are needed.

The circuits in this paper use an a-IGZO ESL technology [4], a proven and reliable but slow technology. The channel length $L_{\min}$ is 15 μm (reference) or 9 μm (scaled). Figure 12.3.1 shows the performance of the diode load inverter depending on the supply. Diode load logic is fast and robust, at the cost of high power consumption [1]. To improve robustness, the backgate (BG) is used to increase the VT of the drive transistor (inset Fig. 12.3.1). The average inverter has a delay of 2.75 μs , while consuming 24.1 μW . In samples, speed correlates very closely with power, since the pull-up current determines both.

This work focuses on two types of memory: Laser Programmable ROM (LPROM) and SRAM. Figure 12.3.2 shows the architecture of all matrices. Three LPROM versions are demonstrated. The reference design uses a two-phase readout with precharge to increase speed and reduce cell size [4]. A single multi-input NOR gate is used in the decoder (DEC), increasing speed compared to [4]. To improve the readout speed, a version is designed with a sense amplifier (SA) on the bitline. A pass gate multiplexer (PGM) serves as column decoder to reduce the number of SAs and reduce total power consumption. Third, a timing generation circuit was added to the reference design to show the feasibility and performance of a completely integrated system. The SRAM arrays have 512 bits, in 8 bitlines of 64 cells. The matrix dimensions are chosen asymmetrically to match the bitline behaviour to a larger system, i.e. 64x64.

Figure 12.3.3 shows the schematics of the new blocks. The pass gate MUX consumes less power compared to a diode load implementation since no static leakage path exists. Furthermore, the delay in the MUX is reduced, because the discharge delay of the bitline is dominant with respect to the RC delay of the MUX, whereas the diode load MUX adds two gate delays. Secondly, the sense amplifier (SA) is introduced in the LPROM matrices to decrease readout time and energy. Contrary to SRAM, there are no differential signals available per cell as input of the SA. Therefore, a dummy line is added. The dummy line is like other bitlines, but the pull-down transistor is only half the size. A dummy half-sized transistor is added to match the capacitance. The bitline discharges at half the speed of a regular line, creating a matched reference for the SA. The output of the dummy line also passes through the same PGM to closely match delays.

Finally, a timing generation circuit was designed to generate the precharge (Pre) and wordline enable (WLEN) signal from a clock. Figure 12.3.3 shows the schematic of this circuit, while Fig. 12.3.5 shows the timing diagram. A dummy line is added to the matrix. The dummy line is identical to any bitline with additional load to ensure it is always slower than the other bitlines. This line operates as a reference to monitor the speed of the operation. Since it operates under the same conditions, the timing of this line matches the real bitline behaviour. First, the incoming clock signal is converted in a short Start Pulse. This signal is used to start the precharge phase by setting the precharge flipflop. A sense inverter with a high trip point, set by the BG, is added on the dummy line. When the dummy line reaches this high trip point, the precharge flipflop is reset, and the wordline flipflop is set. Therefore, the WLEN signal is activated and the dummy line discharges. When the dummy line is sufficiently discharged, a sense inverter with low trip point resets the WLEN, ending the readout cycle.

In Fig. 12.3.4, the effect of the different changes on the LPROM circuits are shown. All data is measured at 10V supply, and one die with 24 different arrays is shown in Fig. 12.3.7. Starting from the literature reference, first the size is increased to 1024 bits, which increases the delay. Additionally, an improved decoder reduces delay and power. Next, the size is again increased 8-fold, with a delay increase of only a factor 2, and a power increase of less than 4, demonstrating the effectiveness of the employed techniques. In the next step, the $L_{\min}$ is reduced from 15 μm to 9 μm , including similar scaling of wiring and parasitics. This increases readout speed by a factor 2.35, while the power increases slightly, by 7.8% to 6.1mW, due to a slight decrease of VT for shorter channel lengths. Two variants are made based on this design. Introducing the PGM and SA, speed increases by 30% and power reduces by 36%. When the integrated timing circuit is used, the delay increases by 50% compared to the ideal timing applied in the lab due to the required design margins. The energy consumption decreases by 18% because the output drivers are engaged for a shorter time.

Figure 12.3.5 shows the resulting timing for the 8kb LPROM with SA and the SRAM memory at 10V supply. The Shmoo plots show the improvement in speed when using higher supply voltages. The 8kb LPROM with SA operates at 87kb/s. The performance of the 1kb LPROM memory meets the NFC spec using NDEF messages, where the required data rate is 105.9kb/s. This memory operates at 7V at 140kb/s, with only 0.55mW power consumption. However, if 15V supply is used, the speed increases to 0.5Mb/s at 8.95mW power consumption.

Figure 12.3.6 shows a comparison with the state of the art and the Intel Si 4000 chipset of the early '70s. The SRAM memory is 4x larger than previously published metal-oxide memories, operates at 10V supply, and is >5.5x faster. The performance of LPROM also significantly improves: even though internal timing is used, the size increased from 128b to 8kb, and the supply is only 10V, the speed is increased to 44kb/s at a power of only 1.67 $\mu\text{W/b}$, a 21-fold reduction. If a sense amplifier is combined with a pass gate mux, the speed can be increased to 87kb/s. Finally, we have shown an NFC-compatible 1kb memory which operates from 7V supply at 140kb/s, using only 0.540 $\mu\text{W/b}$. Despite the large difference in mobility between pMOS (~450cm²/Vs) and metal-oxides (~10cm²/Vs), the performance of both SRAM and LPROM with similar $L_{\min}$ is very similar.

Acknowledgements:

The authors are very grateful for the received funding from the European Union's Horizon 2020 research and innovation program under grant agreement No 644331 (PING project) and No 716426 (FLICs project). F.D.R thanks the Agency for Innovation by Science and Technology in Flanders (IWT-Vlaanderen) for financial support.

References:

- [1] K. Myny, et al., "The development of flexible integrated circuits based on thin-film transistors," *Nature Electronics*, vol. 1, pp. 30-39, 2018.
- [2] K. Myny, et al., "A Thin-film microprocessor with inkjet print-programmable memory," *Scientific Reports*, vol. 4:7398, pp. 1-6, 2014.
- [3] A. Armstrong, et al., "Intel 4004 – 45th Anniversary Project", 2016. [Online]. Available: www.4004.com. [Accessed: 09-Sept.-18]
- [4] F. De Roose, et al., "A Thin-Film, a-IGZO, 128b SRAM and LPROM Matrix With Integrated Periphery on Flexible Foil," *IEEE J. of Solid-State Circuits*, vol. 52, no. 11, pp. 3095-3103, 2017.
- [5] J. Avila-Niño, et al., "Stable organic static random access memory from a roll-to-roll compatible vacuum evaporation process," *Organic Electronics*, vol. 31, pp. 77-81, 2016.

Figure 12.3.1: Performance of the 15 μ m inverter in the a-IGZO ESL technology: speed, power and variability at 10V V_{DD} . Inset: transfer curve of a TFT with VBG=0V, -1V. Butterfly diagram of 30 SRAM cells with varying scaling.

LPROM 8kbit

SRAM 512bit

Figure 12.3.2: The architecture of the different fabricated memories, demonstrated for the largest array size.

Figure 12.3.3: Schematics of the introduced components. The PGM is shown for a 4:1 configuration but is extended to a 1:16 configuration in the 8kb matrix.

Figure 12.3.4: The measured effect of different LPROM circuit changes on measured speed and power consumption at 10V supply.

Figure 12.3.5: Operating method of the timing generation block. Optimal measured timing for writing and reading the SRAM (0.5kb) and LPROM with SA (8kb) at V_{DD} =10V. Measured Shmoo plots for said circuits.

LPROM

	This work, NFC memory	This work, with SA	This work, with timing	De Roose et al., 2017 [4]	Myny et al., 2014 [2]	Intel 4001, 1971 [3]
Technology	a-IGZO 9 μ m	a-IGZO 9 μ m	a-IGZO 9 μ m	a-IGZO 9 μ m	Hybrid compl. 5 μ m	PMOS 10 μ m
L_{min}	9 μ m	9 μ m	9 μ m	9 μ m	5 μ m	10 μ m
Matrix size	1kbit	8kbit	8kbit	128bit	144bit	4kbit
Supply voltage	7V	10V	10V	15V	10V	15V
Data rate	140kbit/s	87kbit/s	44kbit/s	25kbit/s	5.2kbit/s	750kbit/s
Power per bit	0.540 μ W	1.46 μ W	1.67 μ W	35.1 μ W	N.A.	54.9 μ W
Area efficiency*	29.0%	55.4%	49.6%	4.9%	21.1%	13.7%
Chip size	2.28x2.23mm ²	5.43x3.91mm ²	5.25x4.52mm ²	1.5x2.5mm ²	8.97x6.93mm ²	4.0x2.6mm ²

SRAM

	This work	De Roose et al., 2017 [4]	Avila-Nino et al., 2016 [5]	Intel 4002, 1971 [3]
Technology	a-IGZO 9 μ m	a-IGZO 15 μ m	Organic 50 μ m	PMOS 10 μ m
L_{min}	9 μ m	15 μ m	50 μ m	10 μ m
Matrix size	512bit	128bit	16bit	320bit
Supply voltage	10V	15V	40V	15V
Data rate write	400kbit/s	72.7kbit/s	11.1kbit/s	375kbit/s
Data rate read	242kbit/s	30.8kbit/s	N.A.	375kbit/s
Power per bit	125.9 μ W	98.4 μ W	N.A.	797 μ W
Area efficiency*	23.8%	28.5%	No periphery	19.3%
Chip size	6.71x3.18mm ²	3.94x3.13mm ²	> 4x4mm ²	3.3x3.8mm ²

*Area efficiency is defined as matrix area / total area

Figure 12.3.6: Comparison Table. The circuits shown outperform thin-film state of the art in almost all specifications, and is quite comparable to the intel MCS4 platform.

Figure 12.3.7: Photograph of the die area with all memory matrices. Closeup of the matrices in the comparison table.