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From on-chip self-healing to self-adaptivity in analog/RF ICs: challenges and opportunities

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Abstract—The numerous variations that affect analog and RF circuits are becoming a limiting factor in the design of these circuits in deeply scaled CMOS technologies. An emerging idea to counteract these effects is to let the circuit compensate for these variations itself, referred to as self-healing. Over the last decade, a wide variety of off- and on-chip techniques for compensating these variations have been researched. This paper targets to give an overview of the state-of-the-art, and organize the proposed techniques in a common taxonomy. This allows to determine remaining open issues and research challenges. In particular, the SotA lacks efficient solutions for fully-integrated, short time-scale self-adaptation. The paper ends by giving an outlook towards promising research directions to enable such self-adaptation in mWatt power budgets for Internet of things applications, focusing on embedded machine-learning techniques.

I. INTRODUCTION

Circuits fabricated in deeply scaled CMOS technologies are more and more susceptible to a lot of variations, not only at manufacturing time, but also later during their lifetime. Those variations can be broadly classified in three categories: *static*, *quasi-static*, and *dynamic*. Static variations only affect the circuit once and remain constant. This is e.g. experienced due to manufacturing variations or defects. Quasi-static variations have a (slowly) varying impact on the circuit over time. Examples here are aging or stress. Dynamic variations affect the circuit with rapidly-varying impact, such as e.g. variations due to temperature changes, voltage variations, operating conditions, etc. Over the last decade, these different types of variations have increasingly started to impact analog and Radio-Frequency (RF) circuit performance, amongst others due to increased performance needs, increased device variation, and decreasing device reliability [1]. Designers have responded to this with two orthogonal strategies:

Take always more margins on the design specifications. This ensures proper circuit operation under all possible variations at run-time conditions during their complete lifetime. This however severely limits maximum achievable performance, and introduces significant power consumption overheads.

Compensate for these variations. In this approach, that is often referred to as *healing or adaptation*, variations are sensed through sensors, and on-chip tuning knobs are tuned to correct the circuit's performance accordingly. However, such analog/RF circuit healing has a high cost, as it requires to explore and measure the performances of the circuit under a wide range of variations and tuning parameters. A good amount of State of the art (SotA) publications target to improve this

Fig. 1. Overview of a circuit with healing capabilities

challenging trade-off between the quality, the cost and the speed of such healing or adaptation strategies.

This work intends to give an overview and taxonomy of SotA approaches, identify the remaining challenges and propose opportunities for future research. To this extend, the rest of this paper is organized as follows. Section II will detail our taxonomy system and make an overview of current SotA. Section III will then highlight limitations in the SotA. Finally section IV will detail possible opportunities to develop energy-efficient adaptive algorithms, specifically exploiting emerging machine-learning techniques.

II. SOTA AND TAXONOMY OF ANALOG/RF SELF-HEALING / SELF-ADAPTATION

A typical circuit with healing capabilities is illustrated in Fig.1. In this subsection, the term healing is used as a general term, referring to an additional intelligence built to heal/adapt the circuit under consideration (referred as the circuit to heal in Fig.1). The self-healing framework then aims at compensating for part of, or all the variations experienced by the circuit (i.e. static and/or quasi-static and/or dynamic), in an autonomous manner. To achieve this, the circuit to heal is equipped with several key features (see Fig.1): 1.) *sensors* to monitor all types of considered variations, 2.) *tuning knobs* to adjust circuit's performances and 3.) a core *self-healing algorithm*, which essentially decides each tuning knob setting to apply in response to measured conditions.

The self-healing algorithm may start the healing procedure with very limited a priori knowledge on the best settings to be found. An on-chip strategy then needs to be embedded, e.g. using an exhaustive search or an optimizer. In this case, we will say that the optimal healing states are characterized

Fig. 2. Overview of state of the art methodologies

on-chip. Alternatively, the circuit can know a priori which are the optimal setting to be applied for each groups of possible conditions, from a model built in an off-line characterization phase, before using the circuit in the field. The settings are then loaded in the circuit in the beginning of its lifetime as seen in the bottom of Fig.1. In this case we will say that the optimal healing states are characterized off-chip.

A. Nomenclature used for the taxonomy

In this work, we organize SotA techniques in several groups, depending on the type of variations they compensate for: static and/or quasi-static and/or dynamic, (as discussed in Section I). As such, three categories are distinguished:

- 1.) **Self-calibration**, capable of compensating for static variations only, such as manufacturing variations or defects.
- 2.) **Self-healing**, capable of compensating for static and quasi-static variations, such as aging or stress.
- 3.) **Self-adaptation**, capable of compensating for static, quasi-static and dynamic variations, such as channel impairments or dynamic operating conditions.

In addition, those techniques will orthogonally be organized regarding where the characterization of the optimal adaptation states is taking place. As introduced in the beginning of section II, we distinguish two categories:

A.) Off-chip characterization, as illustrated in Fig.3.(a), refers to the fact that the optimal calibration/healing/adaptation states are found off-line, and only executed on-chip, for instance using a Look-Up Table (LUT). The algorithm then consists in periodically (a) measuring the current conditions, (b) choosing the corresponding tuning knob setting regarding these conditions and (c) applying these settings to the circuit. In this case, the adaptive behavior of the circuit is completely modeled beforehand, which enable to execute it efficiently in hardware but impacts its versatility.

B.) On-chip characterization, as illustrated in Fig.3.(b), refers to the fact that the optimal calibration/healing/adaptation settings are found and executed on-chip, without prior model being built. In this case, the system finds its optimal tuning knob values on the fly as it measures the current conditions. Finding the best tuning setting can be done for example using an exhaustive search for small systems, but this is usually

Fig. 3. Overview of (a) off-chip characterization and (b) on-chip characterization for calibration/healing/adaptation algorithms

impracticable for larger scale systems with (significantly) more than hundreds of possible tuning combinations. Then, most SotA rely on an embedded optimizer, driven by general optimization constraints and a fitness functions to be measured. This approach is very flexible but requires more hardware resources (area, power, speed).

Note that based on this off- of on-chip characterization we always assume that the calibration, healing or adaptation process itself completely takes place on chip, i.e. the loop between sensors and tuning knobs of Fig 1 is closed on chip. How this loop is closed varies among state of the art techniques, which will be discussed more elaborately in Section II.B. Fig.2 summarizes this discussion, depicting the different works along the taxonomy introduced in Section II.A.

B. SotA on analog/RF self-calibration

Most self-healing methodologies developed in the literature are largely focused on process variations, that are becoming a show-stopper in the design of analog and RF circuits [1], [2]. Numerous self-calibration techniques have been presented, that can be classified in two categories [3], depending if they are based on *direct* performance measurements [3]–[5], or if they rely on *statistical* techniques [1], [2], [6]–[8]. Direct methodologies aim to evaluate performance targets directly while integrating a maximum of the measurement and analysis circuitry on-chip to reduce test cost. They then perform automatically several tests, such as time- or frequency-domain analysis, to evaluate circuit's performances directly. Alternatively, statistical methodologies achieve low-cost by using indirect tests, relying on the alternate test paradigm [9]. In this case, direct performance measurements are replaced by low-cost sensors measuring continuous or low-frequency characteristics. Machine learning techniques are then used to correlate the sensor values to the circuit's performances, to predict the performances solely based on the

sensor measurements. Both direct and statistical methodologies have been extended to self-calibration procedures where the best combination of tuning setting is found automatically.

a) Off-chip characterized self-calibration: concerning analog and RF circuits, the main issue associated to test is the cost. To limit this cost, the best combination of tuning knobs can be even found in a unique test iteration, using a machine learning that includes both process and tuning variations one one. This referred as *one-shot* [2], [8], [10]. A comparative of one-shot methodologies is available in [1] to calibrate a RF amplifier. Since these methodologies are performed off-line, they do not use many on-chip resources. However, the calibration can be performed only post-manufacturing.

b) On-chip characterized self-calibration: to further reduce test cost, reuse the calibration during lifetime and possibly extend it towards self-healing, the full test circuitry must be integrated on-chip, which as been achieved by both direct and statistical methodologies. As an example for a direct methodology, the method in [3] automatically runs a series of tests to evaluate the performance of a bandpass biquad filter. An on-chip optimizer is then used to find the optimal tuning settings. Results show that power can be significantly reduced, from 2.1 mW to 0.6 mW, with the same performance. However, a lot of tests are necessary and the procedure is difficult to extend for other circuits. As an example of a statistical methodology, [6] implements a on-chip neural network in the analog domain. This enables, after training, to predict a figure of merit (FoM) for a low-noise amplifier, representative of a trade-off between its main performances. After calibration, the power consumption is significantly reduced for all circuits with minimal impact on the performances. However, the strategy is limited to the prediction of one FoM and do not consider several performances explicitly.

C. Self-healing methodologies

With on-chip implementation, self-calibration techniques can be extended towards self-healing. The circuit can then run periodically and compensate for quasi-static variations. We will consider only on-chip characterized self-healing techniques since to the best of our knowledge, off-chip characterized techniques for self-healing only have not been proposed.

On-chip characterized self-healing: self-healing methodologies can be circuit-specific [11], [12], or more generally applicable [5], [13]. Focusing on generally-applicable methods, [5] and [13] propose self-healing frameworks based on on-chip optimization algorithms. The healing procedure is run periodically, thus the self-healing system can be put into sleep mode most of the time. The power consumption can be consequently kept around $2mW$ and $3mW$, resp. in [13] and [5], which is a fraction of the total power consumption of a full RF transceiver for instance.

D. Full self-adaptive methodologies

a) Off-chip characterized self-adaptation: to avoid the need of an on-chip optimizer, it is possible to pre-compute the optimal settings regarding possible groups of operating

conditions, for instance using statistical techniques. An off-line optimization phase is first carried out to build a control law, which models the relationship between optimal circuit performances and operating conditions (e.g. measured by on-chip sensors). This control law is then stored in a LUT, and subsequently used on-line by the circuit. Sensor values are measured and the corresponding settings are applied regarding the settings read in the LUT. This approach has been recently applied for Internet of Things (IoT) applications, specifically for a video sensor node aiming at human detection [14]. The full system including adaptation mechanisms consumes 4 to 7 mJ per frame, which represents 40 to 70 mW at 10 frames per second. This is around one order of magnitude less than self-healing techniques. In addition, this technique could include also process variations, following a methodology detailed in [15]. However, the best settings are pre-defined before the circuit lifetime, and are not run fully on-chip which limits the overall system flexibility.

b) On-chip characterized self-adaptation: numerous on-chip methodologies have been presented to compensate for dynamic variations only, which are not in the scope of this work. Yet, including all types of variations while characterizing the optimal states directly on-chip is still mainly an open challenge. An emerging solution recently proposed is the use of *self-learning* [7]. In this case, the circuit builds its own training data by experimenting when the system is not used, and learns itself the best adaptation settings regarding the experienced conditions. All types of variations are implicitly considered by this technique and the learning can be updated during the whole circuit lifetime. However, this technique needs a full embedded processor, limiting the applicability to applications with significant processing capabilities.

III. CURRENT LIMITATIONS OF THE STATE OF THE ART

To summarize the discussion in section II, illustrated in Fig.2, we identified three main challenges that remain in the development of resource-efficient on-chip adaptive algorithms: *Challenge 1: maintaining adaptation quality without large area cost.* As the number of variations to be considered and the complexity of the systems increase, healing and adaptation algorithms become bigger. For instance, the strategy in [13] requires $0.63mm^2$ in 32nm technology, excluding memory, which can become large for smaller sized systems. Simplifying this optimization task is crucial to integrate these adaptation strategies without sacrificing accuracy.

Challenge 2: increasing adaptation speed without large power cost. Currently, the power consumption of the healing/adaptation algorithm itself limits the amount of time that it can be used without affecting the overall circuit consumption. For instance, when activated constantly, the healing algorithms presented in [13] and [5] consume respectively 106 mW and 145 mW. This is the case because these techniques still rely on an optimizer or a complex procedure to heal the circuits.

Challenge 3: enabling on-chip characterization without power and area cost. Previous discussion revealed that there are very power and area efficient solutions available. Yet, they strongly

rely on off-chip characterization and account mostly only for (quasi-)static variations. Recent techniques try to bring more intelligence on-chip to integrate calibration on-chip and/or tackle dynamic variations. Yet, all state of the art solutions result in a significant rise in the circuit's area budget and power consumption.

By targeting the implementation of a fully on-chip characterized self-adaptive system, in an IoT node for instance, offering a large flexibility, the power and resource consumption of the algorithm should be at least lowered by an order of magnitude regarding the current SotA.

IV. EMBEDDED MACHINE-LEARNING FOR RESOURCE-EFFICIENT ON-CHIP IMPLEMENTATION

Adaptive circuits could benefit from the integration efforts made in the IoT area, with deep learning processors consuming less and less power [16]. These are:

Opportunity 1 (solving challenge 1): compact model representation. Machine-learning techniques can enable a very compact model representation of the mapping between sensors and tuning knobs. Towards this direction, Bayesian Networks (BNs) have proven their efficiency to have a compact representation of the problem and make decisions very energy-efficiently compared to classical processors [17]. In addition, hardware platform start to be developed, able to run a BN with several orders of magnitude less power than a micro-controller, e.g. consuming less than $100nW$ on given tasks [18].

Opportunity 2 (solving challenge 2): model versatility. In terms of adaptation speed, off-chip characterized methodologies have a significant advantage over on-chip characterized, since a list of optimal results are pre-computed off-line. However, embedded machine-learning algorithms could also be used with additional tasks than the required adaptation. For instance, we can think about anomaly detection, where the main adaptation algorithms could be turned on only when a significant change of the operating conditions is detected. Machine-learning have proven their efficiency adapting such hierarchical systems [19].

Opportunity 3 (solving challenge 3): inference and learning techniques. Electronic systems could also use clever inference and learning algorithms inspired from the robotics area, for instance, using reinforcement-learning techniques. In addition, BNs are also transferred to hardware using tractable models, in the form of arithmetic circuits consisting of sums and products. The inference can then be performed more easily on-chip [20].

V. CONCLUSION

This paper proposes a taxonomy for self-calibration/-healing/-adaptive analog/RF ICs, covering the full spectrum of experienced variations. Current SotA implementations have been mapped, and their limitations discussed. This allows to extract 3 challenges for resource-efficient integrated self-adaptivity: 1.) maintaining adaptation quality without large area cost, 2.) increasing adaptation speed without large power cost and 3.) enabling on-chip characterization without power and area cost. Yet, promising opportunities exist for future research, specifically based on embedded machine-learning techniques.

REFERENCES

- [1] Y. Lu, K. S. Subramani, H. Huang, N. Kupp, and Y. Makris, "A comparative study of one-shot statistical calibration methods for analog/rf ics," 2015, pp. 1–10.
- [2] M. Andraud, H. Stratigopoulos, and E. Simeu, "One-shot non-intrusive calibration against process variations for analog/RF circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 11, pp. 2022–2035, Nov 2016.
- [3] S. Lee, C. Shi, J. Wang, S. Sanabria, H. Osman, J. Hu, and E. Sanchez-Sinencio, "A built-in self-test and in situ analog circuit optimization platform," *IEEE Transactions on Circuits and Systems-I: Regular Papers*, pp. 1–14, 2018.
- [4] T. Das, A. Gopalan, C. Washburn, and P. R. Mukund, "Self-calibration of input-match in RF front-end circuitry," *IEEE Transactions on Circuits and Systems-II: Express Briefs*, vol. 52, no. 12, pp. 821–825, 2005.
- [5] E. J. Wyers, M. A. Morton, T. C. L. C. Sollner, C. T. Kelley, and P. Franzon, "A generally applicable calibration algorithm for digitally reconfigurable self-healing RFICs," *IEEE Transactions on Very Large-Scale Integration Systems*, vol. 24, no. 3, pp. 1–14, 2018.
- [6] G. Volanis, D. Maliuk, Y. Lu, K. S. Subramani, and Y. Makris, "On-die learning-based self-calibration of analog/rf ics," 2016.
- [7] D. Banerjee et al., "Self-learning RF receiver systems: Process aware real-time adaptation to channel conditions for low power operation," *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol. 64, no. 1, pp. 195–208, 2017.
- [8] D. Han, B. S. Kim, and A. Chatterjee, "DSP-Driven self-tuning of RF circuits for process-induced performance variability," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 18, no. 2, pp. 301–314, 2010.
- [9] P. N. Variyam, S. Cherubal, and A. Chatterjee, "Prediction of analog performance parameters using fast transient testing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 21, no. 3, pp. 349–361, 2002.
- [10] N. Kupp, H.-G. Stratigopoulos, Y. Makris, and P. Drineas, "On proving the efficiency of alternative RF tests," in *Proc. IEEE/ACM International Conference on Computer-Aided Design*, 2011, pp. 762–767.
- [11] C. Maxey, G. Creech, S. Raman, J. Rockway, K. Groves, T. Quach, L. Orlando, and A. Mattamana, "Mixed-signal SoCs with in situ self-healing circuitry," *IEEE Design & Test of Computers*, vol. 29, no. 6, pp. 27–39, 2012.
- [12] A. Tang et al., "A low-overhead self-healing embedded system for ensuring high yield and long-term sustainability of 60ghz 4gb/s radio-on-a-chip," in *Proc. of IEEE International Solid-State Circuits Conference*, 2012, pp. 316–317.
- [13] J. Carballido et al., "A programmable calibration/BIST engine for RF and analog blocks in socs integrated in a 32nm CMOS wifi transceiver," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 7, pp. 1669–1679, 2013.
- [14] N. Cao, S. Bin Nasser, S. Sen, and A. Raychowdhury, "Self-optimizing iot wireless video sensor node with in-situ data analytics and context-driven energy-aware real-time adaptation," *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol. 64, no. 9, pp. 2470–2480, 2017.
- [15] S. Sen, V. Natarajan, D. S., and A. Chatterjee, "Process-variation tolerant channel-adaptive virtually zero-margin low-power wireless receiver systems," *IEEE Transactions of Computer-Aided Design of Circuits and Systems*, vol. 33, no. 12, pp. 1764–1777, 2014.
- [16] B. Moons and M. Verhelst, "Energy-efficiency and accuracy of stochastic computing circuits in emerging technologies," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 4, no. 4, pp. 475–486, Dec 2014.
- [17] M. Lin, I. Lebedev, and J. Wawrzyniek, "High-throughput bayesian computing machine with reconfigurable hardware," in *Proceedings of the 18th Annual ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, ser. FPGA '10, 2010, pp. 73–82.
- [18] O. U. Khan and D. D. Wentzloff, "Hardware accelerator for probabilistic inference in 65-nm cmos," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 3, pp. 837–845, March 2016.
- [19] K. Badami et al., "Context-aware hierarchical information-sensing in a $6\mu w$ 90nm CMOS voice activity detector," in *Proc. of IEEE International Solid-State Circuits Conference*, 2015, pp. 430–432.
- [20] M. Chavira and A. Darwiche, "On probabilistic inference by weighted model counting," *Artificial Intelligence*, vol. 172, no. 6–7, pp. 772–799, 2008.