

Modelling of Coplanar Interdigital Capacitor for Microwave Microfluidic Application

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Abstract—Due to its non-invasive property, the interdigital capacitor (IDC) has been applied in dielectric liquid detection and characterization. In order to integrate the IDC sensor on a lab-on-chip, it is often required to minimize and optimize the sensor for sensitive and efficient performance. However, the conventional numerical simulation approach is quite time-consuming. Therefore, an efficient analytical method is proposed herein, leading to accurate capacitance and conductance expressions of an arbitrary multilayer-structured IDC. The model is validated with practical measurements of a series of coplanar waveguide (CPW) structure based IDCs. Additionally, an accurate characterization function, which relates the IDC capacitance and conductance to the complex permittivity of a material loaded on top of the IDC sensing area, is obtained. The characterization function shows good agreement with finite element method (FEM) simulation results, which demonstrates the capability of the IDC sensor in dielectric spectroscopy measurements of μL and even nL liquids.

Index Terms—Conformal mapping, interdigital capacitor, microwave, microfluidic, sensor.

I. INTRODUCTION

INTERDIGITAL capacitor (IDC) [1], [2], which is widely employed in telecommunication systems, has recently shown its potential in liquid detection and characterization as a non-invasive sensor in chemical and biological fields [3]–[5]. Especially, with the advances in chip materials [6] and the progress of MEMS fabrication technologies [7], IDC structure has been scaled down and integrated in microfluidic systems [5], [8], showing its numerous advantages in dramatically decreasing the amount of sample volumes and in improving the measurement throughput.

As a miniaturized sensor, it is of obvious importance to optimize its operating sensitivity. The most commonly used technique is a numerical method, such as a finite element method (FEM), to simulate the whole structure

and analyze the distribution of electromagnetic field in the structure. Though the numerical method can provide accurate and reliable information, repeating the process of structure modification, parameter setting and data processing is rather time-consuming and inefficient. Moreover, most accurate commercial numerical tools are not at an affordable price for many researchers. As a result, an inexpensive and efficient analytical technique that is capable of representing the electromagnetic field distribution in the IDC structure and characterizing the behavior and properties of the IDC sensor could be very useful.

One of the acceptable analytical methods is the conformal mapping technique (CMT). CMT has been used to explain electromagnetic field problems in coplanar structures, including transmission lines and waveguides [9]–[13] and interdigitated electrodes [2], [14]–[16]. In the case where an IDC works as a sensor, the interdigital fingers are sandwiched between multiple dielectric layers, so it is necessary to analyze the IDC with a multilayer structure. Up to now, two representative models have been reported for multilayer-structured interdigital electrodes [2], [17]. In [2], the authors demonstrated an analytical model to calculate the IDC capacitance on three-layered substrates [2]. However, when calculating the periodical section, to avoid a complicated derivation procedure, the authors mapped the semi-infinite strip 3064 instead of the rectangular area 0256 of Z-plane to the upper half of an intermediate T-plane. Then, still using the Schwarz-Christoffel transformation process to map the upper half of the T-plane onto the interior of the rectangle in W-plane is physically not correct, which may consequently result in inaccurate final analytical results. By employing conformal mapping technique and partial capacitance theory, [17] presents closed-form expressions for interdigital electrode arrays, which have similar geometry and boundary conditions to the interdigital capacitor. However, in the model of [17], the fringing effects at the electrode ends were ignored. Moreover, the ground electric wall (the virtual $V = 0$ wall) was assumed to be in the middle of two electrodes for the exterior partial capacitance analysis, which might decrease the calculation accuracy [17]. Therefore, it is significant to improve the state-of-the-art multilayer IDC model in order to provide accurate analytical theory for sensor design.

Presented here is an approach for modeling a multilayer-structured coplanar interdigital capacitor, which is aimed at providing theories for the sensor design and optimization. In the analytical procedure, Schwarz-Christoffel

Manuscript received December 03, 2018; revised February 05, 2019, accepted April 14, 2019. This work was supported in part by the KU Leuven research project C24/15/015 Microwave Microbiology ($\mu^2\text{BIO}$), in part by the project Hercules, and in part by the MTT-S 2018 Graduate Fellowship. (Corresponding author: Xiue Bao.)

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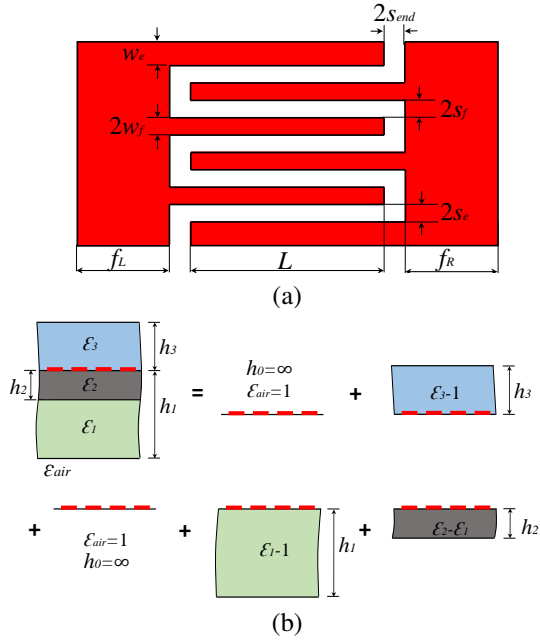


Fig. 1. Schematic of a multilayer interdigital capacitor structure showing (a) top view of the electrode plane, where six fingers are interdigitated, and (b) cross-section of the multilayer structure and the splitting process based on the partial capacitance technique.

conformal mapping (SCM) [18] and Mobius transformation technique [19] are used. Apart from that, to accurately analyze the capacitance of a multilayer structure, we introduce the partial capacitance method [12], which is also extended for analyzing multilayer conductance in this paper. Then, the analytical capacitance and conductance expressions work as the foundation for priori estimate of a coplanar waveguide (CPW) structure based IDC sensor, and provide permittivity extraction principle for dielectric material characterization.

The paper is organized as follows: Section II divides a typical multilayer IDC structure into representative unit cells, and provides theories for the subsequent modeling process. Section III physically and mathematically explains the modeling procedure of the multilayer IDC structure, which finally leads to closed-form analytical expressions for the IDC capacitance and conductance. In Section IV, the properties and optimization principles of a CPW based IDC sensor are specifically described and validated with either measurement or simulation results. A conclusion is finally drawn in the last section.

II. PHYSICAL MODEL OF THE MULTILAYER IDC

The schematic of a typical multilayer IDC structure is presented in Fig. 1, where the parameters $2w_f$, $2s_f$, w_e , $2s_e$, L , f_L , f_R , and $2s_{end}$ are separately defined as the interior finger width, the gap between interior fingers, the width of either exterior finger, the gap between an interior finger and an exterior finger, finger length, the length of the left side feeding line, the length of the right side feeding line, and the gap at the end of the fingers, respectively. The interdigital electrodes are assumed to be sandwiched between three different substrate layers (as shown in Fig. 1(b)), with the dielectric constant

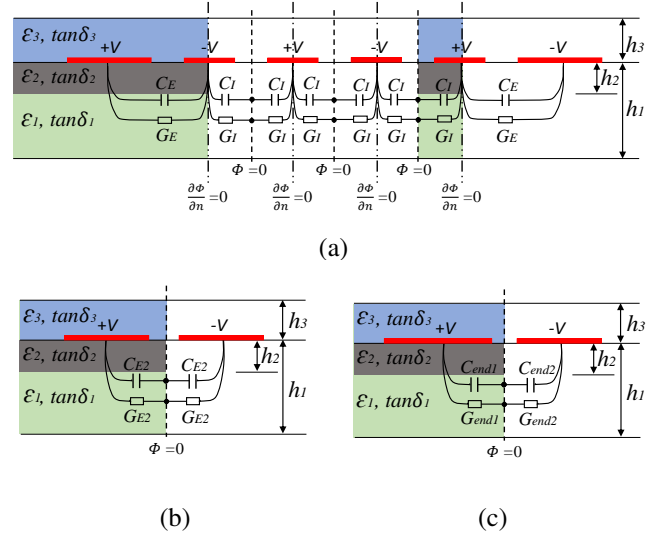


Fig. 2. Equivalent circuits of the multilayer IDC showing (a) interior and exterior unit cells for finger number $n \geq 3$, (b) exterior unit cell for finger number $n = 2$, and (c) finger end unit cell (composed of feed-part and finger-part).

(i.e., real part of relative permittivity) being ϵ_1 , ϵ_2 , and ϵ_3 , for substrate 1, substrate 2, and substrate 3, respectively. According to the partial capacitance theory [12], [13], the multilayer substrate IDC structure can be equivalent to the sum of several single-layer IDCs with the dielectric constant of the corresponding substrate being modified [2], [17]. The equivalent split partial IDCs are presented in Fig. 1(b), where “1” is the relative permittivity of air substrate (i.e., $\epsilon_{air} = 1$). Thus the total capacitance of the multilayer IDC can be expressed as

$$C_{total} = 2C_0 + (\epsilon_1 - 1)C_1 + (\epsilon_2 - \epsilon_1)C_2 + (\epsilon_3 - 1)C_3 \quad (1)$$

where C_{total} includes both the upper half plane and the lower half plane of the electrodes; C_0 , C_1 , C_2 , and C_3 are the partial capacitance of single layer IDC, with the substrate being filled with air and the substrate thickness being $h_0 = \infty$, h_1 , h_2 , and h_3 , respectively.

It should be noted that when analyzing the coplanar electrodes that are embedded in a multilayer assembly of dielectric materials using the partial capacitance method, three possible cases should be considered [20]–[22]. In the first case, there is a monotonic decrease in the dielectric constants from layer to layer when moving away from the electrode plane. In this case, magnetic walls with $\partial\Phi/\partial n = 0$ is assumed at the substrate/substrate (or substrate/air) interfaces, and then the technique called parallel partial capacitance can be adopted. Second, the dielectric constant of the substrate increases monotonically as we move away from the electrode plane. In this case, we assume that electric walls with Φ being constant exists at the interfaces and as a result, the technique called series partial capacitance is applied. The final case is that there is no monotonic behavior for the dielectric constant of the substrate layers. For simplicity and being consistent with the actual sensing application, the dielectric constant (i.e., real part of relative permittivity value) of the substrate is assumed

to be larger when the substrate layer is located closer to the electrodes, satisfying the boundary condition of the first case.

Aiming at calculating the partial capacitance C_0 , C_1 , C_2 , and C_3 in (1), we can equivalently divide the whole multilayer IDC structure into several unit cells [2], as seen in Fig. 2. The separation procedure is based on the equivalent magnetic walls (with $\partial\Phi/\partial n = 0$) and the equivalent electric walls (with $\Phi = 0$) that are generated by the currents flowing through the IDC electrodes. For finger number $n \geq 3$, there are mainly two representative unit cells: the interior periodical part and the exterior unit cell that includes one exterior and half interior electrodes, as shown in Fig. 2(a). Specially, for a two-finger ($n = 2$) IDC, there is only one type unit cell that considers an exterior electrode, as presented in Fig. 2(b). In order to accurately analyze the IDC structure, the fringing effect of the finger ends should also be taken into account. Considering the asymmetry at the two sides of the finger end gap, the fringing effect is presented by a finger-part unit cell and a feeding-part unit cell, as presented in Fig. 2(c).

In practice, when the multilayer substrates in Fig. 1 are lossy, there should also exist conductance, which is related to the dielectric loss, between the electrodes of the multilayer IDC. As shown in Fig. 2, the dielectric loss tangent of substrate 1, substrate 2, and substrate 3, is assumed to be $\tan \delta_1$, $\tan \delta_2$, and $\tan \delta_3$, respectively [23]. The “dielectric conductivity” of the substrate is related to its own real part of the relative permittivity and the dielectric loss tangent by $\sigma = \omega \varepsilon_0 \varepsilon \tan \delta$ [24], [25], where $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m is the permittivity of free space. Employing the same conformal mapping transformations as the case of partial capacitance, the partial conductance could also be illustrated [9]. The equivalent per-unit-length capacitance and equivalent per-unit-length conductance associated to the multilayer substrates are also presented in Fig. 2. In terms of the calculation for each unit cell, analyzing one half plane with one single substrate layer is enough for the complete multilayer IDC structure. Because according to partial capacitance/conductance theory, the other half plane uses the same method with only the thickness h being different. In order to enhance clearness of presentation, the subsequent analytical procedure focus on capacitance derivation, with only showing the final formulas for each partial conductance.

III. CONFORMAL MAPPING FOR IDC CALCULATION

In order to calculate the per-unit-length capacitance and conductance of the representative unit cells in Fig. 2, several CMT procedures are performed. To keep neatness and clearness, we try to use the following analytical procedure for each unit cell. First, determining the boundary condition of the unit cell for both the case when the substrate thickness is finite ($h = h_i$, $i = 1, 2, 3$) and the case when the substrate thickness is infinite ($h = h_0 = \infty$), as shown in Fig. 1(b). Second, presenting the unit in Z -plane, with the coordinates determined by the corresponding physical two-dimensional geometry parameters of the unit. Third, using Schwarz-Christoffel mapping [18] method to map the information in Z -plane to the complete upper half of a

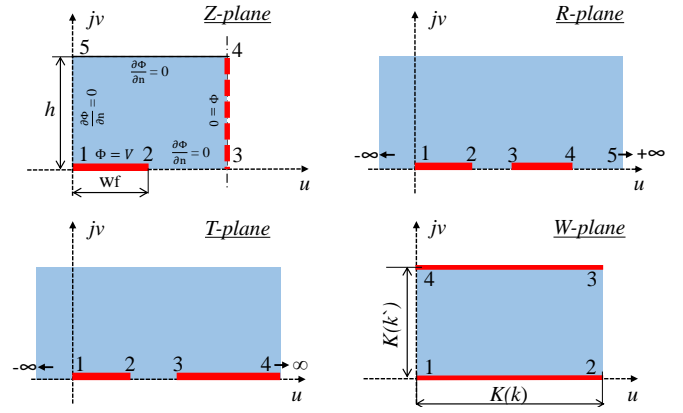


Fig. 3. Coordinates of the interior periodical unit cell with finite thickness of substrate in Z -plane, and its mapped R -plane, T -plane and W -plane.

auxiliary plane - R -plane. Forth, transforming the upper half of R -plane to the upper half of another auxiliary plane - T -plane through a Möbius transformation [19] technique, locating the equivalent electrodes in special positions of T -plane. Finally, using a second SCM method to convert the upper half of T -plane to a closed parallel plate capacitor region in W -plane, by which the capacitance is readily obtained.

A. Interior Unit C_I and G_I

1) *Finite Single Layer Calculation:* The cross-section of a single layer interior unit cell that has finite substrate thickness $h = h_i$ is presented in the Z -plane in Fig. 3. According to the physical parameters in Fig. 1(a), the key complex coordinates in Z -plane are defined as: $z_1 = 0$, $z_2 = w_f$, $z_3 = w_f + s_f$, $z_4 = (w_f + s_f) + jh_i$, and $z_5 = jh_i$. The square area 1345 in the Z -plane can be transformed to the upper half plane of the R -plane in Fig. 3, using the following SCM [18] relationship

$$z = A_1 \int^r \frac{1}{\sqrt{(r-r_1)(r-r_3)(r-r_4)(r-r_5)}} dr + A_2 \quad (2)$$

By assuming $A_1 = (r_5 - r_3)(r_1 - r_4)/2$, $A_2 = 0$, (2) can be expressed as

$$z = \int_0^\lambda \frac{d\lambda}{\sqrt{(1-\lambda^2)(1-k_{xi}^2\lambda^2)}} \quad (3)$$

$$= F(\phi, k_{xi}) \quad (4)$$

where the modulus $k_{xi} = \sqrt{\frac{(r_1-r_3)(r_5-r_4)}{(r_5-r_3)(r_1-r_4)}}$, $\lambda = \sin \phi = \sqrt{\frac{(r_5-r_3)(r-r_1)}{(r_1-r_3)(r-r_5)}}$. Consequently, the rectangular area in the Z -plane is then transformed into the upper half plane of the R -plane by the inverse function of (4) – the following Jacobi elliptic function

$$r = sn(z, k_{xi}) \quad (5)$$

by which r_1, r_2, r_3, r_4 , and r_5 are respectively corresponding with $z_1 = 0$, $z_2 = \frac{w_f}{w_f + s_f} K(k_{xi})$, $z_3 = K(k_{xi})$, $z_4 = K(k_{xi}) + jK(k'_{xi})$, and $z_5 = jK(k'_{xi})$ [26], with

$$\frac{K(k_{xi})}{K(k'_{xi})} = \frac{w_f + s_f}{h_i} \quad (6)$$

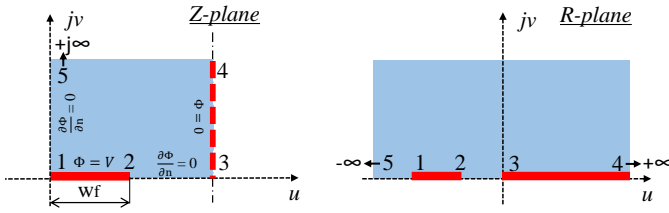


Fig. 4. Coordinates of the interior periodical unit cell with infinite thickness of substrate in Z -plane, and its mapped R -plane.

where $K(k_{xi})$ is the complete elliptic integral of the first kind, and $K(k'_{xi}) = K(\sqrt{1 - k_{xi}^2})$. The value of the modulus k_{xi} is calculated by the following formulas

$$k_{xi} = \frac{\theta_2^2(q_i)}{\theta_3^2(q_i)} \quad (7)$$

$$q_i = \exp \left[-\pi \frac{K(k'_{xi})}{K(k_{xi})} \right] \quad (8)$$

where θ_2 and θ_3 are the Jacobi theta functions that are expressed in terms of the nome q_i [27].

Next, to simplify the subsequent calculation procedure, the upper half of R -plane is transformed to the upper half of T -plane. The conformal mapping process is based on Mobius transformation [19], and the following equation is used

$$t = \frac{(r_1 - r)(r_4 - r_2)}{(r_4 - r)(r_1 - r_2)} \quad (9)$$

which maps r_1 , r_2 , and r_4 to $t_1 = 0$, $t_2 = 1$, and $t_4 = \infty$, respectively, as shown in Fig. 3.

Finally, using similar SCM transformation technique to that in (2), as

$$w = \int_0^t \frac{dt}{\sqrt{(1-t^2)(1-k_{Ii}^2 t^2)}} \quad (10)$$

the upper half of T -plane can be transformed to a rectangle in W -plane, as shown in Fig. 3. The final result of the modulus k_{Ii} is

$$k_{Ii} = \sqrt{\frac{1}{t_3}}, k'_{Ii} = \sqrt{1 - k_{Ii}^2} \quad (11)$$

2) *Infinite Single Layer Calculation*: The single layer interior unit with infinite substrate thickness ($h = h_0 = \infty$) is represented by the shadow area of the Z -plane in Fig.4. The representative coordinates in the Z -plane are $z_1 = 0$, $z_2 = w_f$, $z_3 = w_f + s_f$, $z_4 = (w_f + s_f) + j\infty$, and $z_5 = j\infty$. The first mapping transformation that converts the shadow area in the Z -plane to the upper half of R -plane is achieved by

$$z = B_1 \int^r \frac{1}{\sqrt{(r-r_1)(r-r_3)}} dr + B_2 \quad (12)$$

If z_1 and z_3 in the Z -plane are assumed to be mapped to the points $r_1 = -1$ and $r_3 = 0$ in the R -plane, as demonstrated in Fig. 4, the equation (12) is readily solved and consequently the transformation expression is obtained

$$r = \sinh^2 \left(\frac{z - B_2}{2B_1} \right) \quad (13)$$

with $B_1 = j(w_f + s_f)/\pi$, and $B_2 = w_f + s_f$. Applying the same process as the previous finite case, the upper half of the R -plane is firstly transformed to the upper half of T -plane, with $t_1 = 0$, $t_2 = 1$, and $t_4 = \infty$, respectively, which is then followed by mapping the upper half of T -plane to a rectangle in W -plane. Finally, we can obtain the expression of modulus k_{I0} , as

$$k_{I0} = \cos \left(\frac{\pi s_f}{2(w_f + s_f)} \right), k'_{I0} = \sqrt{1 - k_{I0}^2} \quad (14)$$

3) *Multilayer Calculation*: Considering the multilayer structure of the IDC, the conclusion of (1) should be used. Substituting the analytical results in (14) and (11) to (1), we can arrive at the per unit length capacitance formed by all interior unit cells

$$C_I = \varepsilon_0 \left[2 \frac{K(k_{I0})}{K(k'_{I0})} + (\varepsilon_1 - 1) \frac{K(k_{I1})}{K(k'_{I1})} + (\varepsilon_2 - \varepsilon_1) \frac{K(k_{I2})}{K(k'_{I2})} + (\varepsilon_3 - 1) \frac{K(k_{I3})}{K(k'_{I3})} \right] \quad (15)$$

As explained in the previous section, with similar analysis procedure to the interior unit capacitance, the interior per unit length conductance is readily obtained

$$G_I = \omega \varepsilon_0 \left[\varepsilon_1 \tan \delta_1 \frac{K(k_{I1})}{K(k'_{I1})} + (\varepsilon_2 \tan \delta_2 - \varepsilon_1 \tan \delta_1) \frac{K(k_{I2})}{K(k'_{I2})} + \varepsilon_3 \tan \delta_3 \frac{K(k_{I3})}{K(k'_{I3})} \right] \quad (16)$$

B. Exterior Unit C_E and G_E

1) *Finger number $n = 2$* : As explained in the previous section, there are mainly two possible occasions for the analysis of the exterior capacitance. If finger number $n = 2$, the exterior unit is expressed in Fig. 2(b). In this case, the analysis method is introduced from the conformal mapping process for coplanar stripline [9]. The complex Z -plane of the exterior unit, which has finite thickness substrate ($h = h_i$), is presented in Fig. 5(a). The coordinates of four key points in the Z -plane are $z_1 = 0$, $z_2 = s_e$, $z_3 = s_e + w_e$, $z_6 = jh_i$. Accordingly, the expression for transforming Z -plane to R -plane is

$$z = C_1 \int^r \frac{1}{\sqrt{(r-r_6)(r-r_1)}} dr + C_2 \quad (17)$$

Using the same mathematical process as in (12), z_6 and z_1 are mapped to $r_6 = -1$ and $r_1 = 0$, respectively, and consequently the transformation expression from Z -plane R -plane is

$$r = \sinh^2 \left(\frac{\pi z}{2h_i} \right) \quad (18)$$

Then, with a Mobius transformation from R -plane to T -plane, with $t_6 = 0$, $t_1 = 1$, and $t_3 = \infty$, respectively, and a SCM transformation from T -plane to W -plane, the expression of modulus k_{E2i} is obtained

$$k_{E2i} = \sqrt{\frac{\cosh^2 \left(\frac{\pi(s_e + w_e)}{2h_i} \right) - \cosh^2 \left(\frac{\pi s_e}{2h_i} \right)}{\cosh^2 \left(\frac{\pi s_e}{2h_i} \right) \cdot \sinh^2 \left(\frac{\pi(s_e + w_e)}{2h_i} \right)}} \quad (19)$$

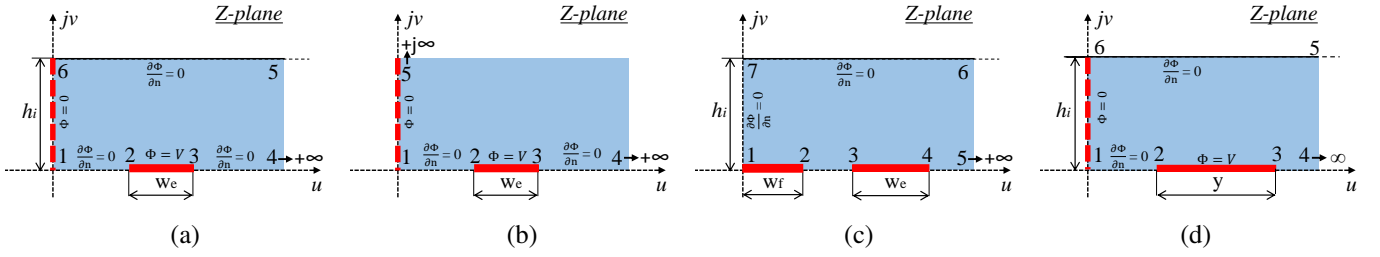


Fig. 5. The Z -plane schematics and key coordinates for (a) two-finger exterior unit cell with finite thickness of substrate, (b) two-finger exterior unit cell with infinite thickness of substrate, (c) multi-finger exterior unit cell with finite thickness of substrate, and (d) finger end unit cell with finite thickness of substrate.

When the substrate has infinite thickness ($h = h_0 = \infty$), the complex Z -plane of the single layer exterior unit is presented in Fig. 5(b). The transformation from the first quadrant of Z -plane to the upper half of R -plane is achieved by

$$r = z^2 \quad (20)$$

and then, the upper half of R -plane is transformed to the upper half of T -plane by

$$t = \frac{(r_5 - r)(r_3 - r_1)}{(r_3 - r)(r_5 - r_1)} \quad (21)$$

which is finally mapped to a rectangle of W -plane with SCM theory. Therefore, the following result is obtained

$$k_{E20} = \sqrt{1 - \frac{s_e^2}{(s_e + w_e)^2}} \quad (22)$$

Consequently, the expressions of the per unit length capacitance and the per unit length conductance for the multilayer two-finger exterior unit are

$$C_{E2} = \varepsilon_0 \left[2 \frac{K(k_{E20})}{K(k'_{E20})} + (\varepsilon_1 - 1) \frac{K(k_{E21})}{K(k'_{E21})} + (\varepsilon_2 - \varepsilon_1) \frac{K(k_{E22})}{K(k'_{E22})} + (\varepsilon_3 - 1) \frac{K(k_{E23})}{K(k'_{E23})} \right] \quad (23)$$

$$G_{E2} = \omega \varepsilon_0 \left[\varepsilon_1 \tan \delta_1 \frac{K(k_{E21})}{K(k'_{E21})} + (\varepsilon_2 \tan \delta_2 - \varepsilon_1 \tan \delta_1) \frac{K(k_{E22})}{K(k'_{E22})} + \varepsilon_3 \tan \delta_3 \frac{K(k_{E23})}{K(k'_{E23})} \right] \quad (24)$$

2) *Finger number $n \geq 3$* : In the case of finger number $n \geq 3$, the exterior unit cell presented in Fig. 2(a) is used, and the conformal mapping process for coplanar waveguide [28] is introduced into the analysis. For completeness, the schematic Z -plane of the exterior unit with finite thickness substrate ($h = h_i$) is presented in Fig. 5(c), and the transformation from Z -plane to R -plane is achieved by

$$r = \sinh^2 \left(\frac{\pi z}{2h_i} \right) \quad (25)$$

which is the same as (18). With several transformations similar to the above analysis, the resultant elliptic modulus k_{Ei} for finite thickness substrate is obtained

$$k_{Ei} = \frac{\sinh\left(\frac{\pi w_f}{2h_i}\right)}{\sinh\left(\frac{\pi(w_f + 2s_e)}{2h_i}\right)} \cdot \sqrt{\frac{1 - \sinh^2\left(\frac{\pi(w_f + 2s_e)}{2h_i}\right) / \sinh^2\left(\frac{\pi(w_f + 2s_e + w_e)}{2h_i}\right)}{1 - \sinh^2\left(\frac{\pi w_f}{2h_i}\right) / \sinh^2\left(\frac{\pi(w_f + 2s_e + w_e)}{2h_i}\right)}} \quad (26)$$

When the substrate has infinite thickness ($h = h_0 = \infty$), the transformation equation from Z -plane to R -plane is also (20), and finally we can obtain the expression of k_{E0} [2], as

$$k_{E0} = \frac{w_f}{w_f + 2s_e} \sqrt{\frac{1 - (w_f + 2s_e)^2 / (w_f + 2s_e + w_e)^2}{1 - w_f^2 / (w_f + 2s_e + w_e)^2}} \quad (27)$$

Consequently, the per unit length capacitance and the per unit length conductance for the exterior unit of multilayer multi-finger IDC ($n \geq 3$) are

$$C_E = \varepsilon_0 \left[2 \frac{K(k_{E0})}{K(k'_{E0})} + (\varepsilon_1 - 1) \frac{K(k_{E1})}{K(k'_{E1})} + (\varepsilon_2 - \varepsilon_1) \frac{K(k_{E2})}{K(k'_{E2})} + (\varepsilon_3 - 1) \frac{K(k_{E3})}{K(k'_{E3})} \right] \quad (28)$$

$$G_E = \omega \varepsilon_0 \left[\varepsilon_1 \tan \delta_1 \frac{K(k_{E1})}{K(k'_{E1})} + (\varepsilon_2 \tan \delta_1 - \varepsilon_1 \tan \delta_1) \frac{K(k_{E2})}{K(k'_{E2})} + \varepsilon_3 \tan \delta_1 \frac{K(k_{E3})}{K(k'_{E3})} \right] \quad (29)$$

F. Finger End C_{end} and G_{end}

The finger end unit cell is shown in Fig. 2(a), and accordingly, the complex Z -plane is presented in Fig. 5(d), where y represents the width of the considered electrode. Obviously, the calculation principle of C_{end} and G_{end} is the same as that of C_{E2} and G_{E2} . As a result, the corresponding expressions for the finger end unit cell are

$$k_{endi} = \sqrt{\frac{\cosh^2\left(\frac{\pi(s_{end} + y)}{2h_i}\right) - \cosh^2\left(\frac{\pi s_{end}}{2h_i}\right)}{\cosh^2\left(\frac{\pi s_{end}}{2h_i}\right) \cdot \sinh^2\left(\frac{\pi(s_{end} + y)}{2h_i}\right)}} \quad (30)$$

$$k_{end0} = \sqrt{1 - \frac{s_{end}^2}{(s_{end} + y)^2}} \quad (31)$$

$$C_{end} = \varepsilon_0 \left[2 \frac{K(k_{end0})}{K(k'_{end0})} + (\varepsilon_1 - 1) \frac{K(k_{end1})}{K(k'_{end1})} + (\varepsilon_2 - \varepsilon_1) \frac{K(k_{end2})}{K(k'_{end2})} + (\varepsilon_3 - 1) \frac{K(k_{end3})}{K(k'_{end3})} \right] \quad (32)$$

$$G_{end} = \omega \varepsilon_0 \left[\varepsilon_1 \tan \delta_1 \frac{K(k_{end1})}{K(k'_{end1})} + (\varepsilon_2 \tan \delta_2 - \varepsilon_1 \tan \delta_1) \frac{K(k_{end2})}{K(k'_{end2})} + \varepsilon_3 \tan \delta_3 \frac{K(k_{end3})}{K(k'_{end3})} \right] \quad (33)$$

where y can be replaced with f_L , $f_R + 2s_{end} + L$, $f_L + 2s_{end} + L$, and f_R , resulting in C_{endL} , C_{endfL} , C_{endfR} , and C_{endR} , respectively, and G_{endL} , G_{endfL} , G_{endfR} , and G_{endR} , respectively.

D. Calculation of Total C and G

The equivalent per unit length capacitance of the complete multilayer IDC is composed of $n - 3$ interior half-capacitance (two unit cell C_I in series), 2 exterior capacitance C_E , and n finger end capacitance (unit cell C_{endL} and C_{endfL} in series, and unit cell C_{endR} and C_{endfR} in series). Therefore, taking into account the length of the IDC electrodes, the total calculation capacitance for the case that there are odd fingers ($n \geq 3$) is

$$C = L \cdot \left[(n-3) \frac{C_I}{2} + 2C_E \right] + (w_e + \frac{n-3}{2} \cdot 2w_f) \frac{C_{endL} \cdot C_{endfL}}{C_{endL} + C_{endfL}} + (w_e + \frac{n-1}{2} \cdot 2w_f) \frac{C_{endR} \cdot C_{endfR}}{C_{endR} + C_{endfR}} \quad (34)$$

and the total IDC capacitance for the case that there are even fingers ($n > 3$) is

$$C = L \cdot \left[(n-3) \frac{C_I}{2} + 2C_E \right] + (w_e + \frac{n-2}{2} \cdot 2w_f) \left(\frac{C_{endL} \cdot C_{endfL}}{C_{endL} + C_{endfL}} + \frac{C_{endR} \cdot C_{endfR}}{C_{endR} + C_{endfR}} \right) \quad (35)$$

Specially, if there are only two fingers, the total IDC capacitance is calculated with

$$C = L \cdot \frac{C_{E2}}{2} + w_e \cdot \left(\frac{C_{endL} \cdot C_{endfL}}{C_{endL} + C_{endfL}} + \frac{C_{endR} \cdot C_{endfR}}{C_{endR} + C_{endfR}} \right) \quad (36)$$

Using similar procedure to the capacitance analysis, the calculation expressions of the corresponding total IDC conductance can be readily obtained.

IV. PROPERTIES OF CPW STRUCTURE BASED IDC SENSOR

The IDC sensor to be discussed here is based on coplanar waveguide structure. Fig. 6(a) and 6(b) schematically present a typical two-port IDC and a typical one-port IDC, respectively. The equivalent circuits at the IDC sensing area of the two-port sensor and the one-port sensor are shown in Fig. 6(c) and 6(d), respectively [4], [29]. In the two-port IDC circuit in Fig. 6(c), the equivalent shunt admittance Y_p is resulting from the substrate and the loaded material at the gaps between

the CPW signal conductor and ground planes. Apart from that, it is clear that the interdigital electrodes of both IDC sensor together with the substrate and material on both sides of the electrodes, are equivalent to a capacitance C in parallel with a conductance G . At low RF/microwave frequencies, the equivalent C and G can be calculated with the equations proposed in the previous section.

According to the functions of (34) to (36), L is linearly related to the total capacitance C . In order to validate this linearity, a series of CPW based one-port IDC structures are lithographically fabricated on a 1 mm Borofloat 33 glass wafer ($\varepsilon = 4.6$, $\tan \delta = 0.0037$ at 10 MHz and 25°C). A ~ 50 nm thick Ti followed by ~ 600 nm thick Au, forms the electrode layer. In terms of the CPW feeding part (as shown in Fig. 6(b)), the width w of the CPW signal line is 100 μm , the width g of either ground plane is 150 μm , the gap s between signal line and ground plane is 20 μm , and the feeding length is 1000 μm . Other dimension parameters that are correlated with the IDC area are presented in Table I, where the finger length of the IDCs varies from 80 μm to 1180 μm . On-wafer measurements were performed on the IDCs with a Keysight M9375A vector network analyzer (VNA), connected to a probe station, and with the microwave 40A-GSG-150C picoprobe (GGB Industries) contacting the IDC. To remove the systematic errors resulting from the cables and connections between VNA and the probe by mathematically placing the reference plane at the probe tip, at first a one-port Short-Open-Load-Thru (SOLT) calibration was carried out, which was accomplished with a commercial alumina CPW impedance standard substrate (ISS) (CS-5 calibration substrate from GGB Industries) and its associated parameters provided by the vendor [4]. Next, aiming at accurately moving the reference plane from the probe tip to the IDC area, a de-embedding process was performed by using an additional bare CPW line that has the same length and cross section with the feeding part of the IDCs [8]. The intermediate frequency bandwidth was set at 20 Hz, and the VNA power was set at -20 dBm to avoid any unwanted microwave heating effects. The room temperature during the measurements was kept at 20°C. For all measurements, the calibrated complex scattering (S-)parameters at 1601 frequency points from 300 kHz to 3 GHz on a log frequency scale were recorded.

TABLE I
DIMENSIONS OF IDCs FOR LENGTH ANALYSIS (UNITS: μm)

$2w_f$	$2s_f$	$2s_e$	w_e	$2s_{end}$	f_L	f_R	L	n
10	10	20	50	20	40	70	80-1180	15

From the calibrated S-parameters of the IDC area, the equivalent C can be readily extracted [8]. Due to the low loss property of glass wafer, G is negligible. The equivalent C values extracted from the measured IDCs with different lengths at the random chosen frequency of 300 MHz are shown in Fig. 7(a). Next, a series of CPW based one-port IDCs that have the same dimensions and substrate properties as the fabricated IDCs were designed with a numerical technique, with which we performed three-dimensional (3D) FEM simulations on these IDCs and recorded the simulated

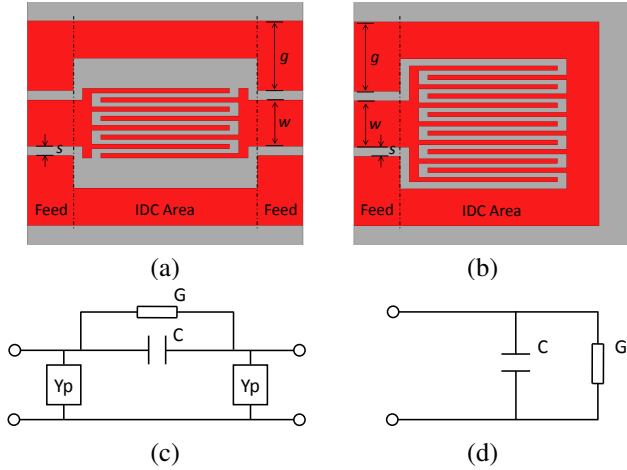


Fig. 6. The schematic coplanar waveguide (CPW) structure based IDC sensor showing: (a) top view of a two-port IDC, (b) top view of a one-port IDC, (c) equivalent electrical circuit of the two-port IDC area [29], and (d) equivalent electrical circuit of the one-port IDC area [4].

S-parameters. Dealing with the simulated results using the same procedure as for the measured S-parameters, we were able to obtain the simulated equivalent C , as shown in Fig. 7(a).

Using the function (34), where w_e is the width of the CPW ground at the IDC area, and C_{end} resulted from w_e is ignored for one-port IDC structure, we calculated the capacitance C of the IDCs with the same dimensions as the fabricated IDCs. To be consistent with the measurements, ε_1 , ε_2 , and ε_3 are 1, 4.6, and 1, respectively, with h_1 , h_2 , h_3 being ∞ , 1 mm, and ∞ , respectively. The calculated C results are also presented in Fig. 7(a). Additionally, as a reference, Fig. 7(a) also presents the calculation capacitance results with the two representative models in [2] and [17].

Similarly, observation of (34) to (36) can lead to the conclusion that C has linear relationship with n . Therefore, six other one-port IDCs were designed and fabricated on the same glass wafer mentioned above, and they were also simulated with the 3D FEM technique. The finger length L is 420 μm , finger number n ranges from 7 to 17, and accordingly w_e varies from 135 μm to 35 μm . Other dimensions are the same as that in Table I. Both the measured and the simulated capacitance results are shown in Fig. 7(b). Using the same dimensions with only n and accordingly w_e being different, we also calculated the C values based on (34) and equations in [2] and [17]. The calculated results are also presented in Fig. 7(b).

It is obvious that the measurement, simulation, and calculation results in Fig. 7(a) and 7(b) all show linear relationship between L and C , and between n and C , respectively. Clearly, compared to the results calculated with the model in [2], the calculation capacitance extracted with the proposed method shows much better agreement with both measurement and simulation results. The proposed model is mainly different from the method of [17] in the calculation of exterior cell C_E and finger end C_{end} , which is an important part of the total capacitance C when there are only a few

short fingers in the CPW based IDCs. As can be observed from Fig. 7(a) and 7(b), the proposed method provides more accurate results than the approach in [17], showing great agreement with both simulation and measurement results.

Based on the analysis in the previous section, the actual dimensions of w_f and s_f can also affect the total value of C . Ignoring the difference between the interior finger width $2w_f$ and exterior finger width w_e , we define the relationship of w_f and s_f as IDC metallization ratio η [17] with the following expression

$$\eta = \frac{w_f}{w_f + s_f} \quad (37)$$

To analyze the dependence of C on η , 13 one-port IDCs were designed and fabricated on the glass wafer and were also simulated with the 3D FEM numerical method. The finger width $2w_f$ varies from 6 μm to 30 μm , and correspondingly, $2s_f$ varies from 41 μm to 5 μm . $2s_e$, w_e , and n were designed as 80 μm , 90 μm , and 3, respectively, with other parameters the same as that in Table I. The measurement dependence and simulation dependence of IDC C on the metallization ratio η are presented in Fig. 7(c). Calculation results by (34), together with the results calculated from other available models in literature [2], [17], are also presented in Fig. 7(c). No obvious difference is observed on the calculation results with the three models, and they all show good agreement with the simulated values. Even though the measurement result is not in good coincidence with the calculation values, the same trend is observed that higher C can be obtained by increasing the metallization ratio η .

The partial capacitance equations (15), (28), and (32) indicate that the real part of the relative permittivity ε_3 of the material on top of the IDC area is linearly correlated with the total capacitance C . A similar derivation process of the IDC partial conductance expressions (16), (29), and (33) indicate that $\varepsilon_3 \tan \delta_3$ is linearly associated with G/ω . The linear properties of the IDC structures have been applied in liquid characterization [4], [29]. To further validate the linearity of the total C and G , and also to compare with other analytical models, a CPW based two-port IDC structure as shown in Fig. 6(a) is simulated here. Parameters w , g , and s of the CPW feeding part are still set to be 100 μm , 150 μm , and 20 μm , respectively. Thickness of the IDC electrodes is set at 0.6 μm , and the dielectric constant of the substrate under the IDC electrodes is 3.78. Other parameters of the two-port IDC are listed in Table II.

TABLE II
DIMENSIONS OF A TWO-PORT IDC (UNITS: μm)

$2w_f$	$2s_f$	$2s_e$	w_e	$2s_{end}$	f_L	f_R	L	n
10	10	10	10	20	40	40	460	8

A given 800 μm thick material, with the complex relative permittivity $\varepsilon^* = \varepsilon_r + j\varepsilon_i$, is assumed to be on top of the IDC area. 3D FEM simulations were separately performed on the two-port IDC with increasing ε_r from 1 to 80 while keeping ε_i fixed, and the simulated two-port S-parameters were recorded. Then, the equivalent capacitance C can be extracted at every

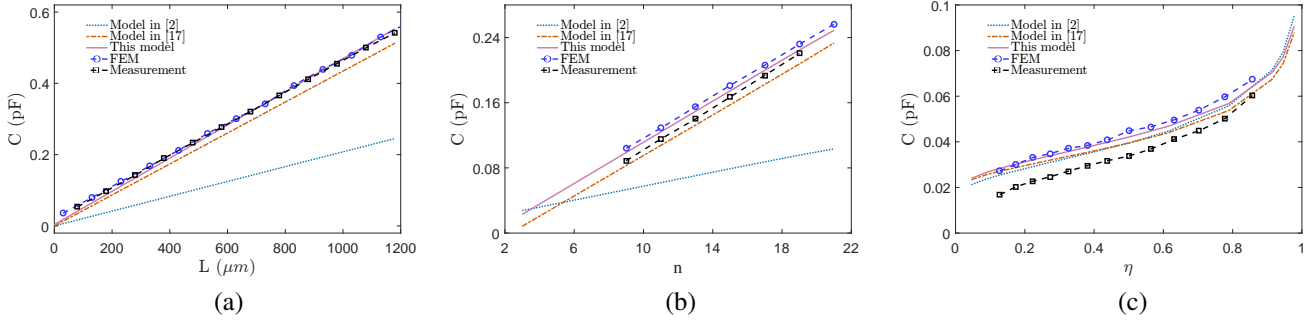


Fig. 7. Properties of a one-port CPW based IDC showing (a) C values versus finger length L , (b) C values versus finger number n , and (c) C as a function of metallization ratio η .

ε_r value [29], which is plotted in Fig. 8(a). In our experience, using different fixed ε_i has negligible effect on the plot, with the repeatability error at about 2%. Increasing ε_i from 0 to 40 while keeping ε_r constant, repeating the 3D FEM simulation and equivalent circuit calculation, we can obtain G at different ε_i settings. The relationship between G/ω and ε_i is plotted in Fig. 8(b), and the repeatability error coming from the effect of different fixed ε_r is also about 2%. Next, using the same dimensions and dielectric parameters as the settings of the above simulated two-port IDC, we calculated the capacitance and conductance with our proposed method. The calculation C and G/ω are presented in Fig. 8(a) and 8(b), respectively. The slight disagreement between simulation and calculation in Fig. 8(a) and 8(b) might partially caused by the equivalent circuit in Fig. 6(c), as it neglects the resistance and inductance [24] associated with the conductors. Nevertheless, both the simulation and calculation results verify the linear relationship between C and ε_r , and between G/ω and ε_i . The same slope for either simulation or calculation plot in Fig. 8(a) and 8(b) indicates

$$\kappa = \frac{\Delta C}{\Delta \varepsilon_r} = \frac{\Delta G}{\omega \Delta \varepsilon_i} \quad (38)$$

which is not difficult to be derived from the analysis in the previous section.

When the IDC structure is designed as a sensor, with the material under test (MUT) covered on top of the IDC electrodes, κ represents its sensitivity. Similar to the conclusion from Fig. 7(a) and 7(b), if we increase L or n , the sensitivity κ linearly increases, as shown in Fig. 8(c) and 8(d), respectively. The dependence of κ on η is presented in Fig. 8(e), which shows that higher metallization ratio results in better sensitivity of the IDC sensor. Nevertheless, in practical application, fabrication limitation should also be considered for small dimensions. As a compromise between sensor sensitivity and fabrication efficiency, η is often designed at 0.5 in microfluidic application [29].

According to the analysis in the previous section, MUT thickness h can affect the sensing results. If we keep the real part of the relative permittivity ε_r of MUT constant, the dependence of IDC capacitance on the MUT thickness variation is shown in Fig. 8(f), where λ_f is dependent on the finger width and the space between fingers, with the definition $\lambda_f = 2 \times (2w_f + 2s_f)$ [17]. According to the calculation result in Fig. 8(f), the primary conclusion can be drawn that if h

is much smaller than λ_f , the increase of h can dramatically increase the total IDC capacitance; whereas if h is larger than half λ_f , the variation of h is negligible. This is also clear from the calculation results with the two other models in Fig. 8(f). The effect of MUT thickness on the extracted IDC capacitance can also be validated with 3D FEM simulations, as shown in Fig. 8(f). Taking into account the effects of MUT relative permittivity values and metallization ratio of the IDC sensor,

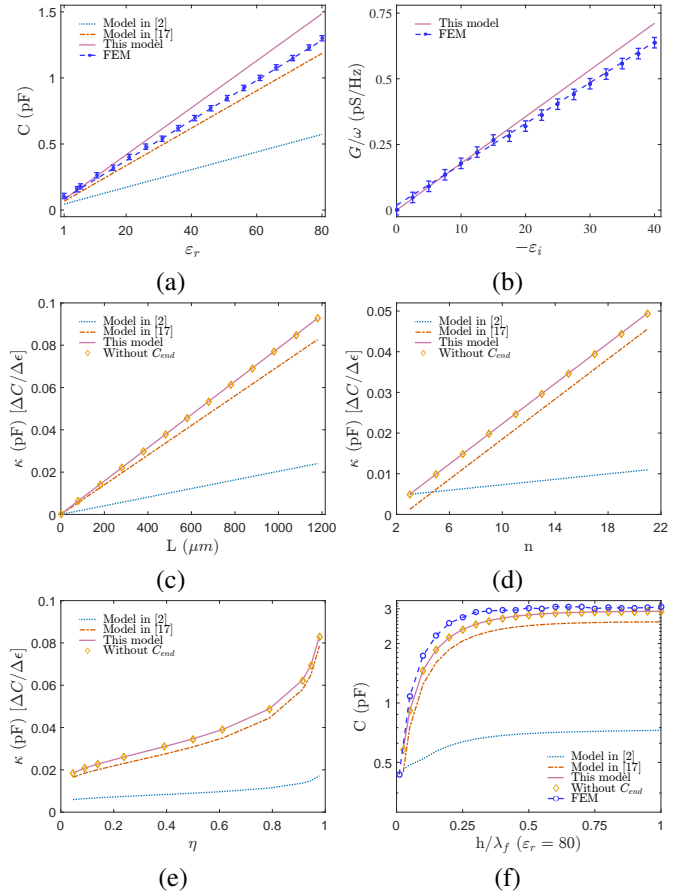


Fig. 8. Properties of the CPW structure based IDC sensor showing (a) C versus ε_r , with error caused by different fixed ε_i values, (b) G/ω versus ε_i , with error caused by different fixed ε_r values, (c) sensing sensitivity κ versus finger length L , (d) sensing sensitivity κ versus finger number n , (e) sensing sensitivity κ as a function of metallization ratio η , and (f) capacitance C due to h/λ_f variations, with MUT $\varepsilon_r = 80$.

we can reach the same conclusion. It is worth reminding that in practical applications, if the IDC device is designed on a thin layer substrate, the dielectric constant of the test fixture where the device is placed should be smaller than the substrate to guarantee the electromagnetic boundary condition.

As a reference, the calculation results analyzed with the two previous models in [2] and [17] are also presented in Fig. 8(a),(c)-(f). As expected, for the CPW based IDCs that have multiple long fingers, the improvement of our proposed model is not obvious compared with the model in [17], because the contribution of exterior units and finger end effects is relatively small. Nevertheless, the better agreement of the FEM simulation results with the calculated data using the proposed technique in Fig. 8(f) can still demonstrate the advantage of the proposed approach in accurately analyzing the IDC sensor. Compared with the model in [2], the proposed model is obviously different in calculating the interior unit, which is also the main cause of the significant disparities of the two models in both Fig. 8 and Fig. 7. Calculation results without considering the finger end effects are also separately shown in Fig. 8(c)-(f). Apparently, when the finger length is much longer than the finger width, the sensitivity contribution from finger ends is neglectable.

V. CONCLUSION

Aiming at analyzing the properties of IDCs and proposing an economical and efficient technique for IDC sensor optimization, we proposed the modeling procedure of a multilayer IDC in this paper. With reasonable electromagnetic boundary analysis, the complete IDC structure is modeled as the sum of different unit cells, and for each unit cell, the multilayer substrates are modeled as the sum of several equivalent single layer parts. Next, using conformal mapping techniques, we successfully obtain the capacitance and conductance expressions of the complete multilayer IDC.

According to the proposed model, we found that the complex permittivity of a material loaded on top of the IDC sensing area is linearly correlated with the IDC capacitance and conductance. The linearity is further validated with a three-dimensional finite element simulation method. From the proposed model, we also analyzed dependence of the IDC capacitance and the IDC operating sensitivity on the IDC sensor's geometry and dimensions. It shows that longer finger, more fingers, and higher metallization ratio at the IDC sensing area result in larger capacitance and better sensitivity.

ACKNOWLEDGMENT

The authors would like to thank Prof. G. Crupi from the Department of Biomedical and Dental Sciences and Morphofunctional Imaging, University of Messina, Messina, Italy, for insightful advice on modeling method, Leuven NanoCentre for device fabrication, and KU Leuven Central Electronic Service for technical support.

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